Space Vector Modulation Technique to Reduce Leakage Current of a Transformerless Three-Phase Four-Leg Photovoltaic System

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Abstract: Photovoltaic systems integrated to the grid have received considerable attention around the world. They can be connected to the electrical grid via galvanic isolation (transformer) or without it (transformerless). Despite making galvanic isolation, low frequency transformer increases size, cost and losses. On the other hand, transformerless PV systems increase the leakage current (common-mode current, (CMC)) through the parasitic capacitors of the PV array. Inverter topology and switching technique are the most important parameters the leakage current depends on. As there is no need to extra hardware for switching scheme modification, it's an economical method for reducing leakage current. This paper evaluates the effect of different space vector modulation techniques on leakage current for a two-level three-phase four-leg inverter used in PV system. It proposes an efficient space vector modulation method which decreases the leakage current to below the quantity specified in VDE-0126-1-1 standard. furthermore, some other characteristics of the space vector modulation schemes that have not been significantly discussed for four-leg inverter, are considered, such as, modulation index, switching actions per period, common-mode voltage (CMV), and total harmonic distortion (THD). An extend software simulation using MATLAB/Simulink is performed to verify the effectiveness of the modulation technique.

Keywords: Photovoltaic Systems, Three-phase Four-leg Inverter, Common-mode Voltage, Leakage Current.

1 Introduction

NOWADAYS, grid connected photovoltaic systems perform an important role in distributed power generation. Number of grid-connected PV systems has grown swiftly in many countries due to governmental supports. For safety reasons, most of the PV systems are connected to the grid by a transformer that isolates the PV panel from the grid. The transformer can be utilized in form of a high frequency transformer in the DC-DC boost converter or in form of a large low frequency transformer on the ac output side [1]. The low frequency transformer increases size and cost, and the high frequency transformer suffers from low efficiency and complex structure. Since the overall efficiency, cost and size are momentous factors in photovoltaic systems, it is beneficial to remove the transformer of the system [2].

PV panels are commonly manufactured from layers of glass, silicon semiconductor and backplane, the junction of these layers is covered by a grounded metallic frame [3]. The capacitors appeared between the earth and the metallic frame, are called parasitic capacitors. Furthermore, a PV inverter operates with high switching frequency which can be conducted to the dc link. Therefore, in transformer absence, the parasitic capacitors of the PV module and voltage ripple in DC bus introduce undesirable leakage current [4]. The leakage current can engender problems for safety, reliability, protection coordination and can make grid current distortion and additional losses in the system [5]. The amplitude of leakage current is mainly dependent on inverter topology and modulation techniques.

Most of the PV systems are in form of single-phase configuration [6]-[11]. In single-phase systems, the ac power in output is pulsating, and large dc capacitors are needed [12]. Thus, for improving the reliability and lifetime of the system, three-phase system is selected for this study. On the other hand, the three-phase multilevel causes considerable cost increase, so modification of modulation schemes for two-level three-phase inverter is preferred for leakage current reduction, as it does not require any additional hardware.

Space vector pulse-width modulation (SVPWM) is

one of the most well-liked and desirable pulse-width modulation schemes due to its advantageous characteristics [13]. Therefore, various SVPWM pulse-pattern-modification methods have been proposed, such as remote-state PWM (RS-PWM), active zero state PWM (AZSPWM) and near-state PWM (NSPWM) [14]-[19]. However, most of the aforementioned methods are limited to three-leg inverters. Although some new SVM methods are proposed for CMV reduction of three-phase four-leg inverters [20, 21], the impact of these methods on inverter leakage current in PV systems has not received sufficient attention. Therefore, these modulation techniques for four-leg inverters need more investigation. Fig. 1 shows a tranformerless PV system with three-phase four-leg inverter.

This paper deals with evaluating the performance of three-phase four-leg inverter under different space vector modulation techniques considering leakage current with photovoltaic energy conversion being the main application. Section II presents the theoretical analysis of the common mode model of a three-phase four-leg PV inverter. In section III classical SVPWM and discontinuous PWM (DPWM) are discussed as conventional PWM methods. Section IV introduces reduced common-mode voltage methods and the proposed method. Section V evaluates simulation results and compares performance of the methods. Finally, the conclusion is provided in section VI.

2 Common-mode Model of Three-phase Four-leg PV Inverter

2.1 PV System with Isolation Transformer

Some PV systems have an isolation transformer between the PV panels and the electrical grid. Common-mode model of such a system is shown in Fig. 2, including the parasitic capacitor of the PV array (C_{PV}) connected between ground and terminal of the PV. In this figure, the transformer winding is specified, and C_t denotes the stray capacitance between the transformer windings. The leakage current can only pass through the stray capacitance of the transformer, in this system. Since C_t has values of order of 100 pF, the leakage
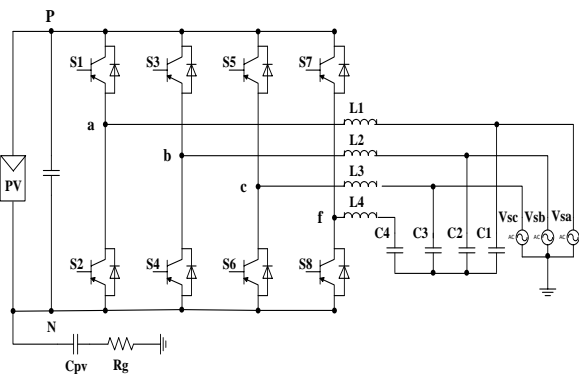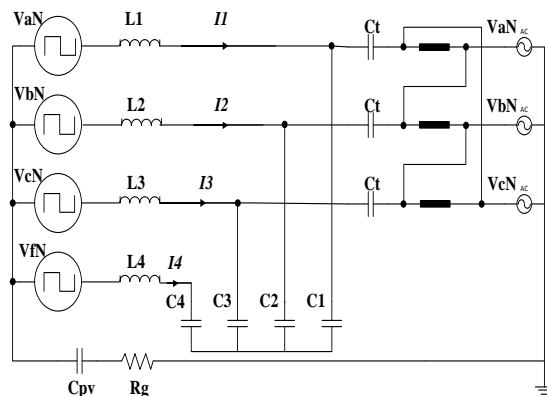

Fig. 2 Common-mode loop model of a PV system with isolation transformer.

current at frequencies lower than 50kHz will be strongly declined and, it can be removed by the EMI filter at higher frequencies [1]. Therefore, in PV systems with galvanic isolation, inverter topology and modulation technique do not affect low frequency leakage current behavior.

2.2 Transformerless PV System

The common-mode model of a transformerless PV system is presented in Fig. 3, where C_{PV} is parasitic capacitor which is influenced by many factors, such as humidity, weather condition, dust covering the PV panel, module frame and so on [22], V_{PV} is parasitic capacitor voltage, I_{CM} is leakage current, and $V_{aN}, V_{bN}, V_{cN}, V_{fN}$ are the voltages between the inverter outputs and negative terminal of the PV array.

In this case, the common-mode behavior is extremely affected by the inverter topology and PWM modulation. For a three-phase four-leg inverter, the relation between the CMV and the phase voltages can be defined as

$$V_{CM} = \frac{V_{aN} + V_{bN} + V_{cN} + V_{fN}}{4} \tag{1}$$

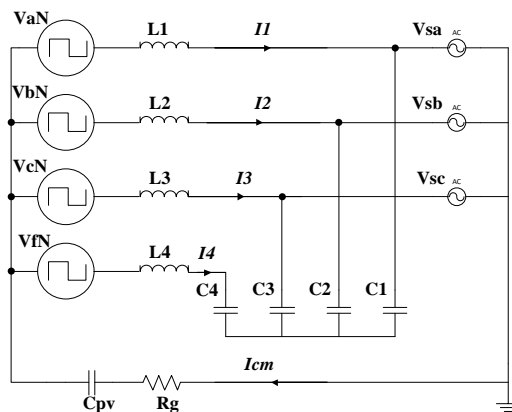Based on mathematical equations derived from Fig. 3 with Kirchhoff laws [23]:

Fig. 3 Common-mode loop model of a transformerless PV system.

Fig. 1 Transformerless grid-connected PV system.

$$V_{PV} = V_{aN} + sL_1I_1 + V_{sa} \tag{2}$$

$$V_{PV} = V_{bN} + sL_2I_2 + V_{sb} \tag{3}$$

$$V_{PV} = V_{cN} + sL_3I_3 + V_{sc} \tag{4}$$

$$V_{PV} = V_{fN} + sL_4I_4 + V_{C4} - V_{C1} + V_{sa} \tag{5}$$

$$V_{PV} = V_{fN} + sL_4I_4 + V_{C4} - V_{C2} + V_{sb} \tag{6}$$

$$V_{PV} = V_{fN} + sL_4I_4 + V_{C4} - V_{C3} + V_{sc} \tag{7}$$

$$I_1 + I_2 + I_3 + I_4 = I_{CM} \tag{8}$$

the parasitic capacitor voltage V_{PV} can be defined as follows:

$$V_{PV(s)} = \frac{4}{4 + s^2 LC_{PV}} V_{CM(s)}$$
$$+ \frac{1}{4 + s^2 LC_{PV}} \frac{3C + C_4}{3C} V_{c4(s)} \tag{9}$$

where $C_1 = C_2 = C_3 = C$, $L_1 = L_2 = L_3 = L_4 = L$ and V_{c4} is the fourth leg capacitor voltage, which can be calculated as

$$V_{c4(s)} = \frac{b_2 s^2 + b_0}{a_4 s^4 + a_2 s^2 + a_0} \left[4V_{CM(s)} - V_{od(s)} \right] \tag{10}$$

where $a_0 = -(9C + 3C_4)$, $b_0 = 12C$, $b_2 = 3LCC_{PV}$, $a_2 = -(12LCC_4 + 3LCC_{PV} + LC_4C_{PV})$, $a_4 = -3L^2CC_4C_{PV}$ and $V_{od} = V_{aN} + V_{bN} + V_{cN}$. And the leakage current is defined as follows:

$$i_{CM(t)} = -C_{PV} \frac{dV_{PV(t)}}{dt} \tag{11}$$

From (11), it can be seen that the leakage current is dependent on the parasitic capacitor (C_{PV}) and $dV_{PV(t)}/dt$. The leakage current can be repressed impressively if the voltage of V_{PV} become constant. From (9) it can be observed that V_{PV} depends on V_{CM} and the fourth-leg capacitor voltage V_{C4} which is related to V_{CM}. Thus, the principal issue is CMV. There are 16 switching states for a three-phase four-leg inverter. In Table 1, different switching states are classified to five groups based on the CMV each state produces.

3 Conventional PWM Methods

The concept of three-dimensional space vector modulation (3-D SVM) was invented by Richard Zhang and was first published in [24]. There are sixteen switching states of the inverter as mentioned in Table 1. The sixteen possible combinations are composed of fourteen active (Non-zero) and two zero (V_0 and V_{15}) vectors of voltage. In Classical SVPWM (CSVPWM) and DPWM, the hexagon created by voltage vectors, divided in six prisms and four tetrahedrons are identified in each prism. Each tetrahedron consists of three active switching vectors and two zero switching vectors. These vectors, in each tetrahedron, are the adjacent switching vectors that are used to synthesize

Table 1 switching states and corresponding CMV level.

Group	Vector	Status	VaN	VbN	VcN	VfN	CMV
group1	V0	nnnn	0	0	0	0	0
group2	V1	nnnp	0	0	0	Vdc	Vdc/4
	V2	nnpn	0	0	Vdc	0	
	V4	npnn	0	Vdc	0	0	
	V8	pnnn	Vdc	0	0	0	
group3	V3	nnpp	0	0	Vdc	Vdc	Vdc/2
	V5	npnp	0	Vdc	0	Vdc	
	V6	nppn	0	Vdc	Vdc	0	
	V9	pnnp	Vdc	0	0	Vdc	
	V10	pnpn	Vdc	0	Vdc	0	
	V12	ppnn	Vdc	Vdc	0	0	
group4	V7	nppp	0	Vdc	Vdc	Vdc	3Vdc/4
	V11	pnpp	Vdc	0	Vdc	Vdc	
	V13	ppnp	Vdc	Vdc	0	Vdc	
	V14	pppn	Vdc	Vdc	Vdc	0	
group5	V15	pppp	Vdc	Vdc	Vdc	Vdc	Vdc

the reference voltage vector.

CSVPWM utilizes equal time length for zero vectors. Fig. 4(a) shows the switching pattern and CMV level of CSVPWM, assuming that the reference vector is in the first tetrahedron of the first prism. As noted in Fig. 4(a), the CMV level changes between 0 and V_{dc} with the same frequency as of the switching. It is also shown that CSVPWM has one switching in each vector change, totaling eight switching actions in one duty cycle. Besides, discontinuous PWM (DPWM) devotes zero time length to one zero vector and full time length to the other. Using even one of the zero vectors causes high CMV for DPWM. As shown in switching pattern of DPWM in Fig. 4(b), there are eight switching actions in one duty cycle. Both CSVPWM and DPWM have modulation index of $0 \leq M \leq 1.155$ which results in high dc bus voltage utilization. Modulation index is defined as

$$M = \frac{2V_{ref}}{V_{dc}} \tag{12}$$

where V_{ref} is the amplitude of reference voltage and V_{dc} is the DC link voltage.

4 Reduced Common-Mode Voltage Methods

4.1 MSVPWM

The idea of this method has been proposed in [20]. The switching vectors of V_0 and V_{15} has the highest amplitude of CMV. In this method, in order to reduce the amplitude of CMV, zero switching states are replaced by two complementary non-zero switching vectors of V_1 and V_{14}. Since this method modifies the Classical SVPWM, it is named Modified SVPWM

(MSVPWM) in this paper. As depicted in Fig. 4(c), the level of CMV declines to between $V_{dc}/4$ and $3V_{dc}/4$. The switching pattern of this method is presented for the first tetrahedron of the first prism. It clearly shows that there are twelve switching actions in a duty cycle, which means much switching loss in comparison to CSVPWM. The dc bus utilization is high ($0 \leq M \leq 1.155$) due to using the same active vectors as CSVPWM uses for synthesizing the reference vector in each tetrahedron.

4.2 Near-State 3-D SVM

In this method, prisms and tetrahedrons are not identified, but six sections formed from half of the two adjoining prisms are introduced. Thus, different adjoining switching vectors are selected and the duration of each switching vector differs from with those of 3-D SVM [21]. NSPWM utilizes four active (non-zero) near vectors to synthesize the reference vector. In Fig. 4(d), it is assumed that the reference voltage vector is in the first defined section (between -30° and 30°). It is noted in Fig. 4(d) that one of the phases is not switched during one PWM cycle, and just six switching actions occur in one cycle, which means less switching loss in comparison to CSVPWM. It is also shown obviously that CMV has been reduced to between $V_{dc}/4$ and $3V_{dc}/4$. The only drawback of this method is linear modulation region, which is limited to $0.77 \leq M \leq 1.155$ [21].

4.3 Proposed Method (Remote State PWM (RSPWM))

This method has been proposed in [25], but for three-phase three-leg inverter in two dimensional space, not for four-leg inverter in three dimensional space. Moreover, it has been used for load neutral point voltage elimination in uninterruptable power supplies in [20], but its influence on leakage current in photovoltaic systems has not been discussed so far. As it is obvious in Table 1, the CMV level of switching states in group 3 is V_dc/2. This method uses the six switching vectors present in group 3 of Table 1, to synthesize reference vector. Utilizing these vectors makes the CMV constant, and based on (11), the leakage current can be suppressed impressively. The selected six vectors are shown in red color in 3-D space in Fig. 5 and their projection on α-β coordinate is shown in Fig. 6. The reference vector can be synthesized by the adjoining four switching vectors. The adjoining voltage vectors for each section are presented in Table 2. The dc bus voltage utilization of RSPWM is different from classical SVPWM and it can be obtained by calculations below.

A rotating reference vector on the α-β coordinate has to be supplied, so that we can obtain a balanced three-phase output voltage. The reference vector in $\alpha\beta\gamma$ coordinate can be represented by
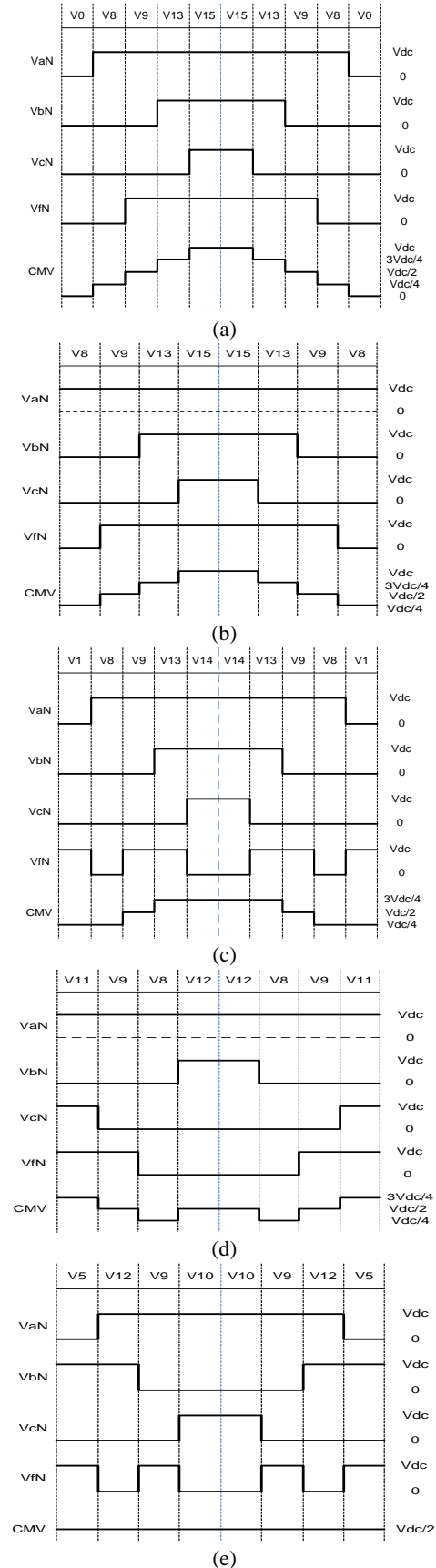

Fig. 4 Switching pattern and CMV level of a) CSVPWM, b) DPWM, c) MSVPWM, d) NSPWM, e) RSPWM.

Table 2 Adjacent vectors in each section.

Section	1	2	3
Switching vectors	V1: pnpn = V10 V2: pnnp = V9 V3: ppnn = V12 V4: npnp = V5	V1: pnnp = V9 V2: ppnn = V12 V3: npnp = V5 V4: nppn = V6	V1: ppnn = V12 V2: npnp = V5 V3: nppn = V6 V4: nnpp = V3
Section	4	5	6
Switching vectors	V1: npnp = V5 V2: nppn = V6 V3: nnpp = V3 V4: pnpn = V10	V1: nppn = V6 V2: nnpp = V3 V3: pnpn = V10 V4: pnnp = V9	V1: nnpp = V3 V2: pnpn = V10 V3: pnnp = V9 V4: ppnn = V12
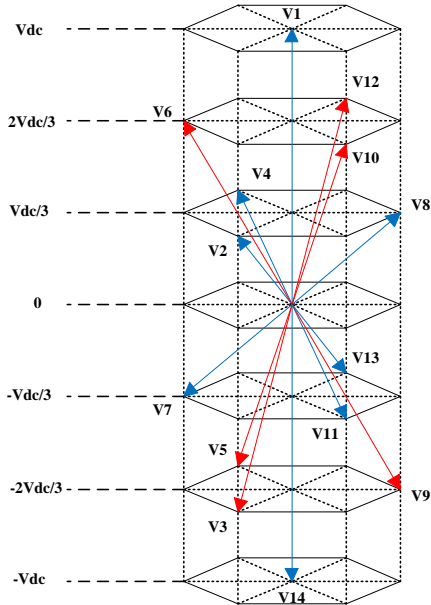
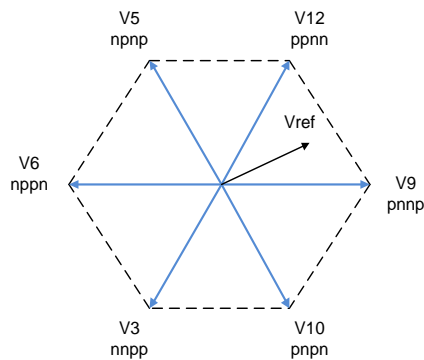**Fig. 5** Switching vectors in 3-D space.

Fig. 6 Projection of switching vectors present in group2 on α-β coordinate.

$$V_{ref} = \begin{pmatrix} V_{\alpha-ref} \\ V_{\beta-ref} \\ V_{\gamma-ref} \end{pmatrix} = \begin{pmatrix} V_{ref}\cos\omega t \\ V_{ref}\sin\omega t \\ 0 \end{pmatrix} \tag{13}$$

Since there are four vectors in each section, the reference switching vector is synthesized as

$$\vec{V}_{ref} = d_1\vec{V}_1 + d_2\vec{V}_2 + d_3\vec{V}_3 + d_4\vec{V}_4 \tag{14}$$

where d_1, d_2, d_3 and d_4 are the duration times of the applied switching vectors. It is assumed that the reference vector is in section I ($0 \leq \omega t \leq \pi/3$). Thus, switching vectors V_5, V_{12}, V_9 and V_{10} will be selected for synthesizing the reference vector,

$$\begin{bmatrix} \dfrac{1}{3} & \dfrac{2}{3} & \dfrac{1}{3} & -\dfrac{1}{3} \\ -\dfrac{1}{\sqrt{3}} & 0 & \dfrac{1}{\sqrt{3}} & \dfrac{1}{\sqrt{3}} \\ \dfrac{2}{3} & -\dfrac{2}{3} & \dfrac{2}{3} & -\dfrac{2}{3} \\ 1 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \end{bmatrix} = \begin{bmatrix} \dfrac{V_{ref}}{V_{dc}}\cos\omega t \\ \dfrac{V_{ref}}{V_{dc}}\sin\omega t \\ 0 \\ 1 \end{bmatrix} \tag{15}$$

The solution of the equations above can be obtained as

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \end{bmatrix} = \begin{bmatrix} -\dfrac{1}{2} & -\dfrac{\sqrt{3}}{2} & \dfrac{1}{4} & \dfrac{1}{2} \\ 1 & 0 & -\dfrac{1}{2} & 0 \\ \dfrac{1}{2} & \dfrac{\sqrt{3}}{2} & \dfrac{1}{2} & 0 \\ -1 & 0 & -\dfrac{1}{4} & \dfrac{1}{2} \end{bmatrix} \begin{bmatrix} \dfrac{V_{ref}}{V_{dc}}\cos\omega t \\ \dfrac{V_{ref}}{V_{dc}}\sin\omega t \\ 0 \\ 1 \end{bmatrix} \tag{16}$$

For other sections the only feature that needs to be changed is the matrix in (16). The corresponding matrixes for other sections are obtained and presented in Appendix. As the time duration of each switching vector should be more than zero, It is found out that the modulation index of RSPWM is $0 \leq M \leq 1$. Thus, the dc bus voltage utilization is reduced in comparison with CSVPWM. The switching pattern of RSPWM for the

first section is presented in Fig. 4(e). It is clear that the total switching actions in a PWM cycle is twelve, which indicates higher switching loss. Despite these shortcomings, the CMV level is constant ($V_{dc}/2$) and does not change by each vector change, which can lead to leakage current reduction without any additional hardware and cost.

5 Simulation Results

The simulations were done in MATLAB/Simulink for modulation index of 0.9. The PV array was simulated with a dc voltage source of 120V and the other parameters of simulated system are listed in Table 3. It is worth mentioning that the PV system under test is a grid connected system, thus the inductive load can be interpreted as the reactive power. Consequently, it should be noted that all of these results are performed with both active and reactive power injection. The results in Fig. 7(a) to 7(e) show the line to line voltage of five modulation techniques. It is obvious that the line to line voltage is unipolar for CSVPWM, DPWM and MSVPWM, while it is bipolar for NSPWM and RSPWM. The THD of CSVPWM, DPWM, MSVPWM, NSPWM and RSPWM is 75.79%, 76.27%, 75.79%, 103.07% and 102.15%, respectively. However, after the output filter, the voltage will be sinusoidal. Fig. 8(a) and 8(b) depicts the grid current for CSVPWM and RSPWM, respectively. The THD of grid current for CSVPWM is 2.61%, while it is 0.59% for RSPWM. As it is clear, more leakage current in CSVPWM creates more grid current distortion. Thus, by mitigating the leakage current, it is possible to reduce harmonic distortion of the grid current. The grid current THD for other methods is presented in Fig. 9.

Fig. 10(a) to 10(e) show the results of the parasitic capacitor voltage and the leakage current. In agreement with theoretical analysis, the parasitic capacitor voltage is time-varying with high amplitude for CSVPWM and DPWM. The RMS value of the leakage current is high for CSVPWM and DPWM, 853mA and 774mA, respectively. In MSVPWM, the frequency of CMV is lower than in CSVPWM and DPWM. The CMV amplitude also decreases and changes between $V_{dc}/4$ and $3V_{dc}/4$. Thus, the RMS value of parasitic capacitor voltage and leakage current become 66.44V and

Table 3 Parameters of the three-phase four-leg system.

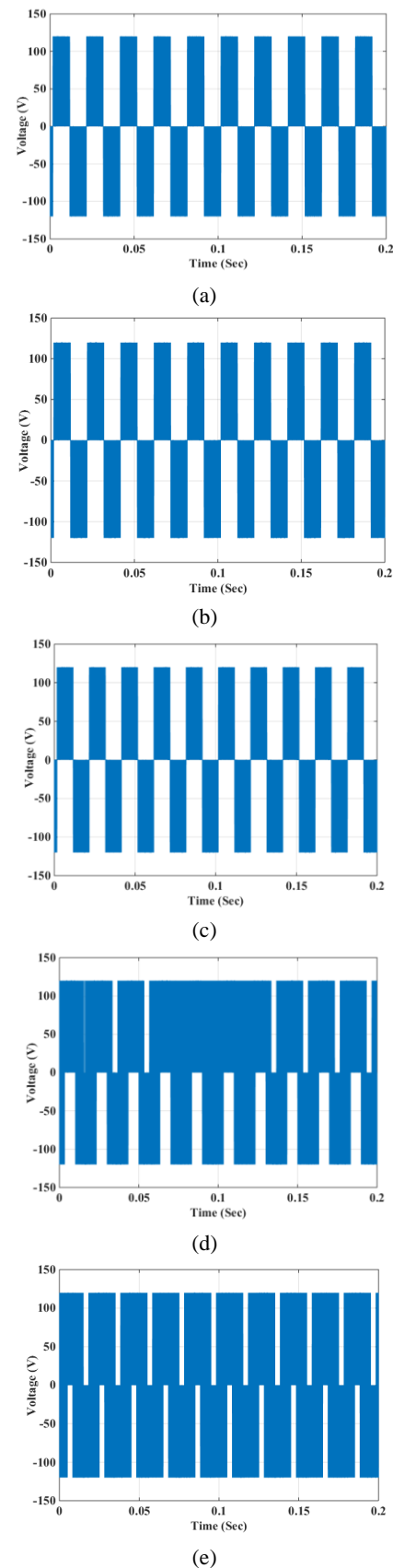| Parameters	Values
DC voltage source (PV)	120 v
Filter inductor (L)	5 mH
Filter capacitor (C)	10 μF
Switching frequency (f)	10 KHz
Parasitic capacitor (Cpv)	300 nF
Ground resistance (Rg)	15 Ω
Grid voltage (Vs)	30 v (peak)

(a)

(b)

(c)

(d)

(e)

Fig. 7 Line-line voltage of a) CSVPWM, b) DPWM, c) MSVPWM, d)NSPWM, e) RSPWM.
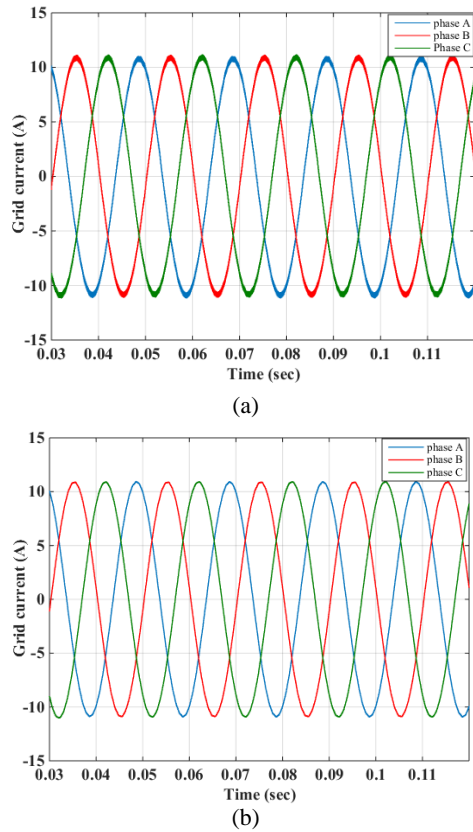
Fig. 8 Grid currents of the PV inverter a) CSVPWM and b) RSPWM.
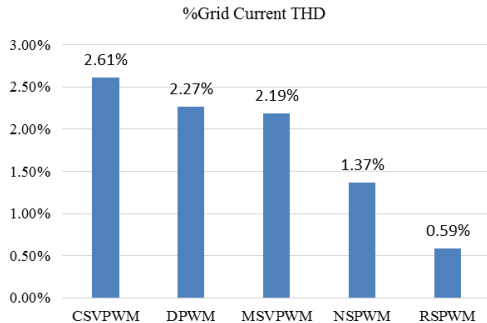

%Grid Current THD

Fig. 9 Harmonic distortion of grid current under different switching methods up to order of 40.

499mA, which are less than of CSVPWM. For NSPWM, although the amplitude of CMV is reduced, it is still time-varying with switching frequency. Therefore, it has almost high value of RMS leakage current, 351mA. By using RSPWM method, The CMV remains constant without any high frequency components. Therefore, the leakage current can be significantly reduced to 118mA, which is almost one seventh of the leakage current amplitude in CSVPWM method. In addition, the maximum value of the leakage current is 276mA which is below 300mA specified in VDE-0126-1-1 standard. The results and comparison of five space vector modulation techniques are shown in Table 4. In this table, some other characteristics are considered as following: switching actions per period, linear modulation region, RMS value of the parasitic

capacitor voltage, total harmonic distortion, and common mode voltage.

Switching loss is a main source of loss and inefficiency in power converters. Switching loss has relevancy with instantaneous power loss in semiconductor devices during turn-on and turn-off time. Thus, the number of switching actions (turn-on and turn-off) in a duty cycle could be important for a PWM scheme. In Table 4 among the five methods, NSPWM and DPWM have the least number of switching actions, equivalent with the least switching loss. It is essential that a PWM scheme being able to operate in its full modulation rang. Especially in applications like variable speed drives which have to sustain constant ratio of voltage to frequency. Moreover, in distributed power generation applications linear range limitation could be a defect when a voltage dip occurs [33]. As it is presented in Table 4, CSVPWM, MSVPWM and DPWM have the modulation index of 0-1.155, meaning that they are able to operate in full modulation region. CSVPWM has the lowest output voltage THD. In the other hand, RSPWM produces the least harmonic content in grid current. Also, when considering the leakage current, RSPWM shows the best performance.

6 Conclusion

This paper has investigated the effect of space vector modulation techniques on leakage current for a two-level three-phase four-leg inverter used in PV system as the main objective. A modulation technique named RSPWM is proposed in which the CMV stays constant. Thus, the maximum leakage current has considerably decreased to below 300mA, as specified in the standard VDE-0126-1-1. In addition, some other characteristics of these modulation techniques have been evaluated which can lead to appropriate method selection proportionate to application purpose. As the results have shown, DPWM and NSPWM have the least switching loss. CSVPWM, DPWM and MSVPWM can operate in full linear modulation range. Also among all the methods, CSVPWM and MSVPWM have the lowest output voltage THD. Furthermore, the harmonic content of grid current is the least for RSPWM.

Table 4 Switching states and corresponding CMV level.

|	CSVPWM	DPWM	MSVPWM	NSPWM	RSPWM
Rms Leakage Current	853 (mA)	774 (mA)	499 (mA)	351 (mA)	118 (mA)
Rms Parasitice Capacitor Voltage	76.51 (V)	85.28 (V)	66.44 (V)	63.2 (V)	60.25 (V)
Maximum leakage current	1.366 (A)	1.425 (A)	0.855 (A)	0.886 (A)	0.276 (A)
CM Voltage	Variable (0-Vdc)	Variable (Vdc/4-Vdc)	Variable (Vdc/4-3 Vdc/4)	Variable (Vdc/4-3 Vdc/4)	Constant (Vdc/2)
Switchings per cycle	8	6	12	6	12
Modulation index (Mi)	0 – 1.155	0 – 1.155	0 – 1.155	0.77 – 1.155	0 – 1
Voltage THD	75.79 %	76.27 %	75.79 %	103.07 %	102.15 %
Grid current THD	2.61%	2.27%	2.19%	1.37%	0.59%
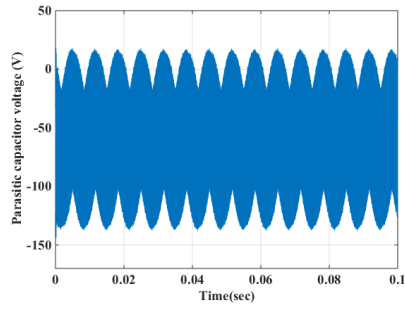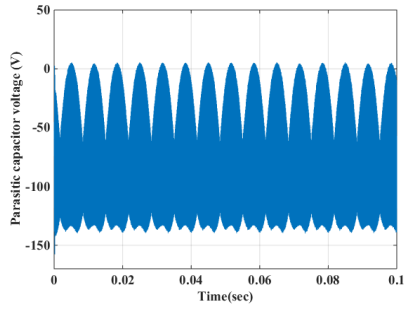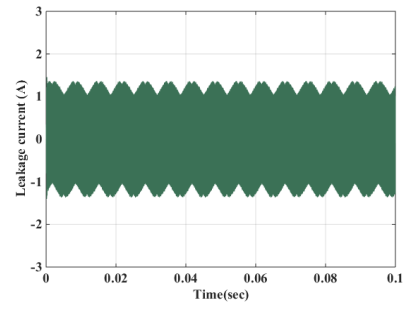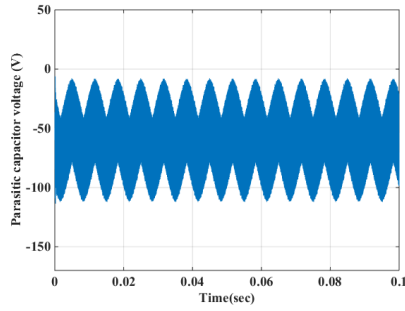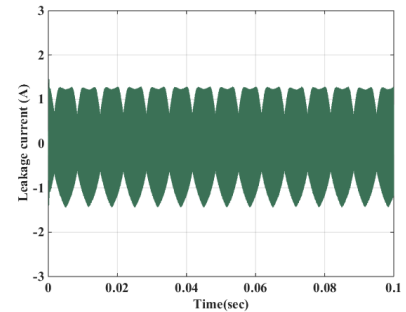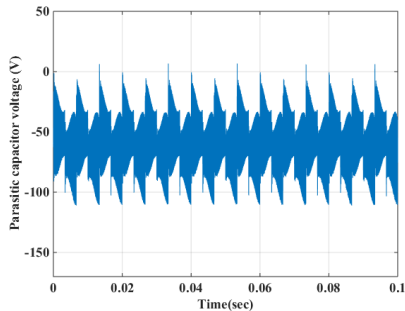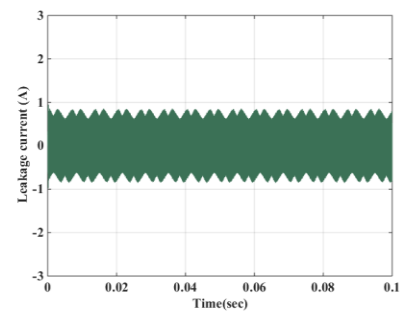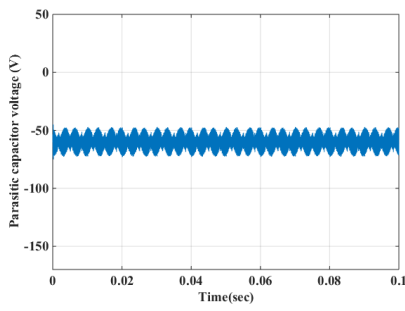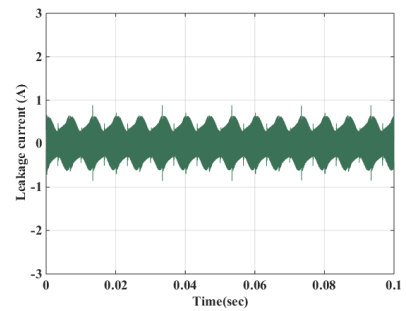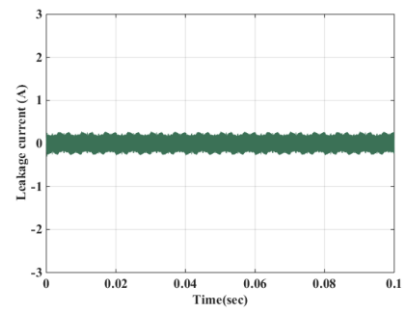
Fig. 10 Parasitic capacitor voltage and leakage current of a) CSVPWM, b) DPWM, c) MSVPWM, d) NSPWM. e) RSPWM.

Appendix Matrix for switching vector duty ratio computation in RSPWM scheme

Section	1	2	3	4	5	6
Matrix of duration of each switching vector	$\begin{bmatrix} -1 & 0 & -\frac{1}{4} & \frac{1}{2} \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{2} & 0 \\ 1 & 0 & -\frac{1}{2} & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{4} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{4} & \frac{1}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{2} & 0 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{4} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{4} & \frac{1}{2} \\ -1 & 0 & \frac{1}{2} & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ 1 & 0 & \frac{1}{4} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & \frac{1}{4} & \frac{1}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ -1 & 0 & \frac{1}{2} & 0 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{4} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{2} & \frac{\sqrt{3}}{2} & -\frac{1}{4} & \frac{1}{2} \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2} & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{4} & \frac{1}{2} \end{bmatrix}$	$\begin{bmatrix} -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{4} & \frac{1}{2} \\ 1 & 0 & -\frac{1}{2} & 0 \\ \frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{2} & 0 \\ -1 & 0 & -\frac{1}{4} & \frac{1}{2} \end{bmatrix}$

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