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Generalized Switched-Inductor Based Buck-Boost Z-H Converter

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Abstract: In this paper, a generalized buck-boost Z-H converter based on switched inductors is proposed. This structure consists of a set of series connected switched-inductor cells. The voltage conversion ratio of the proposed structure is adjusted by changing the number of cells and the duty cycle. Like the conventional Z-H converter, the shoot-through switching state and the diode before LC network are eliminated. The proposed converter can provide high voltage gain in low duty cycles. Considering different values for duty cycle, the proposed structure works in two operating zones. In the first operating zone, it works as a buck-boost converter and in the second operating zone, it works as a boost converter. In this paper, a complete analysis of the proposed converter is presented. In order to confirm the accuracy of mathematic calculations, the simulations results by using PSCAD/EMTDC software are given.

Keywords: Z-Source Converter, Z-H Buck-Boost Converter, Switched-Inductor Cell.

1 Introduction

IN the recent years, the use of modern power electronic converters has been increased and the voltage boosting converters have gained a special importance. Among the voltage boosting converters, studies on a buck-boost converter, known as Z-source converter, have been rapidly developed [1, 2]. This converter has a special impedance (LC) network, which consists of one diode, two inductors and two capacitors in X-shaped structure. This converter has two operating states as shoot-through (ST) and non-shoot-through (non-ST) states. One of the main features of the Z-source converter is that it can be utilized in buck and boost modes with a wide range of output voltages. This structure is more robust and has lower sensitivity to electromagnetic interference.

The Z-source converter, while offering multiple advantages, has some problems such as high voltage stress across capacitors, high inrush current, high costs and etc. In addition, there is a diode or a switch before LC network, which causes the converter to tolerate the high voltage occurring during the ST switching state. Due to the non-continuous current, this diode causes an undesired performance during non-ST switching state. Besides, this diode prevents flowing of reverse current and therefore application of Z-source converter is limited to the cases in which, there are no need to reverse flow of energy to the source [1, 3, 4].

In the literature, new structures and control methods have been presented to address the problems of the Z-source converter. Some of them are algorithms for controlling dc and ac output voltage [5], constant boost control to minimize current ripple of inductor [6] and modeling and control of quazi-Z-Source network for distributed generation applications [7]. Some structures have been presented in [8-12], in which, the main concept is addition of diodes, capacitors and inductors. The Z-source converter, in practice, has been utilized in fuel cell systems [13], motor drives [14], high frequency half-bridge inverters for electrochemistry applications [15, 16], distributed generation [17], photovoltaic systems [18] and electric vehicles [19]. In [4, 20, 21], in order to resolve the problems of the front-end diode in conventional Z-source converters, the Z-H structure, which makes use of the Z-source converter, has been presented. One of the main features of the Z-H converter is that it can be used for dc-dc, ac-dc, dc-ac

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and ac-ac conversions without any change in its structure. The Z-H converter is similar to the voltage source converter, where, there is no ST switching state. A combination of inductors and diodes, known as switched-inductor cell, has been presented in [9, 12, 22, 23]. The switched-inductor cell increases the boosting factor of the converter.

In this paper, a new structure is proposed, which consists of an impedance network similar to Z-source converter, an H-bridge switching circuit similar to Z-H converter and a series of mirrored switched inductor cells. The proposed structure can work in both buck and boost operating modes. In the proposed topology, the voltage conversion ratio can be adjusted by changing the number of switched inductor cells; the diode before LC network is eliminated; due to Z-H structutre there is no ST switching state; and due to the symmetric switched-inductor cells, the proposed converter can be easily developed for ac-ac applications. One main difference between ac-ac converter of Z-H type and Z-source type is that the output voltage of Z-H type has sinusoidal waveform and this resolves the need for additional filter. The performance of the proposed buck-boost converter in dc-dc conversion, with detailed analysis of the equations of voltages, currents and voltage gain, for cells, is presented. Finally, in order to check the accurate performance of the proposed converter, the simulation results of two-cell converter are illustrated in PSCAD/EMTDC software.

2 Proposed Converter

Fig. 1 shows the structure of the proposed converter. This converter consists of four bidirectional switches, two capacitors, two inductors and $2N$ switched-inductor cells where each cell has one inductor and three diodes. As shown in Fig. 1, equal number of cells are arranged in the upper and lower parts of the converter and are connected to input and output dc buses. The inductors L_{n+1} and L'_{n+1} are not the components of the the cells. The generalized structure is obtained by adding new cells to two main inductors. The switched-inductor cells have a number of inductors that in the first operating mode (T_0) are connected in parallel and are charged and in the second operating mode (T_1) are connected in series and are discharged. The proposed converter has two operating zones as $D=[0,\ \frac{1}{N+2})$ and $D=(\frac{1}{N+2},\ 1]$ (D is duty cyle). In $D=[0,\ \frac{1}{N+2})$ the converter works in buck-

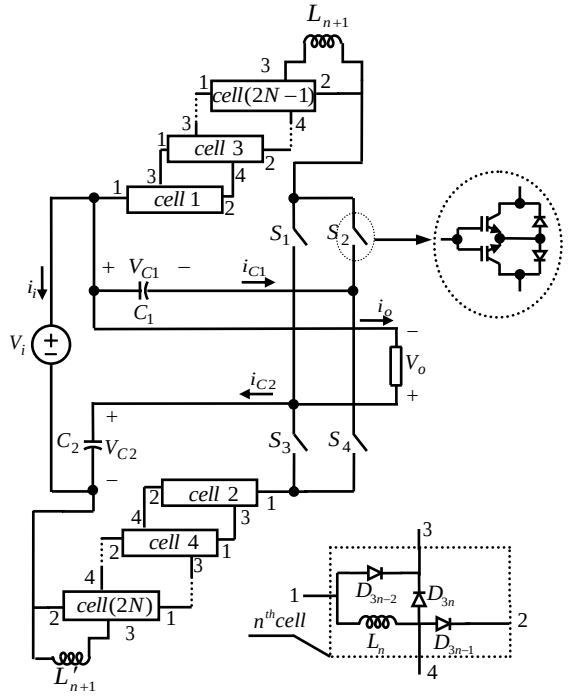


Fig. 1 Poroposed converter.

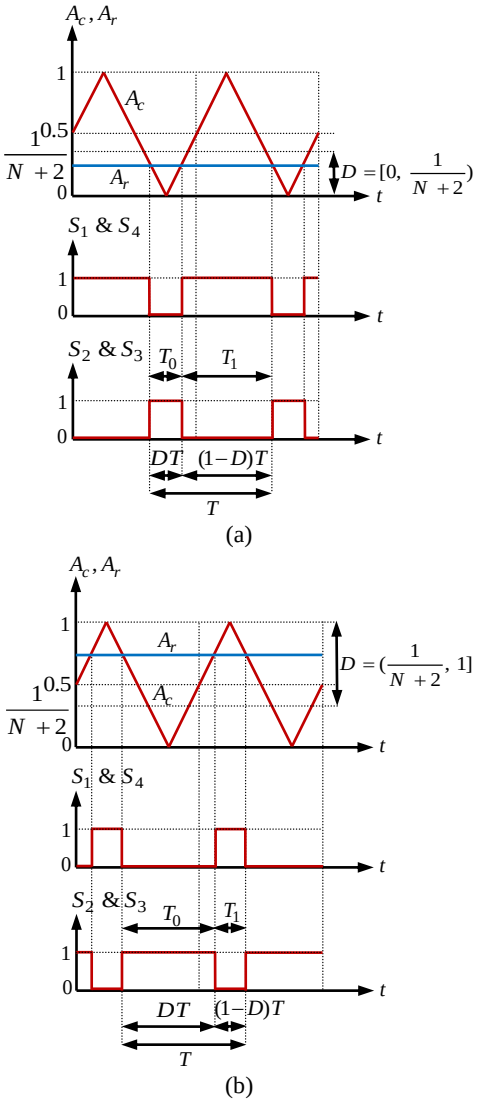


Fig. 2 Control signals for two operating zones; (a) $D=[0,\ \frac{1}{N+2})$; (b) $D=(\frac{1}{N+2},\ 1]$.

boost operation and in $D=(\frac{1}{N+2},\ 1]$ it works in boost operation. The proposed converter can be utilized in dc-dc, ac-dc, dc-ac and ac-ac conversions. In the following, the operation of the converter in dc-dc conversion is presented.

Considering Fig. 2, when the switch S_1 is turned on, the switch S_3 is turned off and vice versa. This is the same for the switches S_2 and S_4. The control signals of these switches (S_1-S_3 or S_2-S_4) are complementary. The switches S_1 and S_4 are turned on and off simultaneously. The same condition is valid for switches S_2 and S_3. Fig. 2 shows the control signals for both operating zones. As shown in Fig. 2, the duty cycle of switches S_2 and S_3 is D.

The proposed Z-H converter in the first operating zone, $D=[0,\ \frac{1}{N+2})$, has two operating modes where in the time interval T_0 (S_2 and S_3 are turned on), the inductors L_n, L_{n+1}, L'_n and L'_{n+1} are charged and in the time interval T_1 (S_1 and S_4 are turned on), the inductors L_n, L_{n+1}, L'_n and L'_{n+1} are discharged. Accordingly, in the second operating zone, $D=(\frac{1}{N+2},\ 1]$, the converter has two operating modes where in the time interval T_0 (S_2 and S_3 are turned on), the inductors L_n, L_{n+1}, L'_n and L'_{n+1} are discharged and in the time interval T_1 (S_1 and S_4 are turned on), the inductors L_n, L_{n+1}, L'_n and L'_{n+1} are charged. The equivalent circuits of the proposed converter, in both the operating zones are shown in Fig. 3.

First Operating Mode (Time Interval T_0)

The equivalent circuit of this mode is illustrated in Fig. 3(a). In this operating mode, the switches S_2 and S_3 and the diodes D_{3n-1}, D_{3n-2}, D'_{3n-1} and D'_{3n-2} are on and the switches S_1 and S_4 and the diodes D_{3n} and D'_{3n} are off. Therefore, $n+1$ number of inductors are conncted in parallel. In this operating mode, when $D=[0,\ \frac{1}{\gamma_{TL}+2})$, the inductors L_n and L_{n+1} are charged by the capacitors C_1 and C_2, respectively; and when $D=(\frac{1}{\gamma_{TL}+2},\ 1]$, the inductors L'_n and L'_{n+1} are discharged by the capacitors C_1 and C_2, respectively. Assuming that the values of L_n, L_{n+1}, L'_n and L'_{n+1} are equal, and the capacitors C_1 and C_2 have equal values

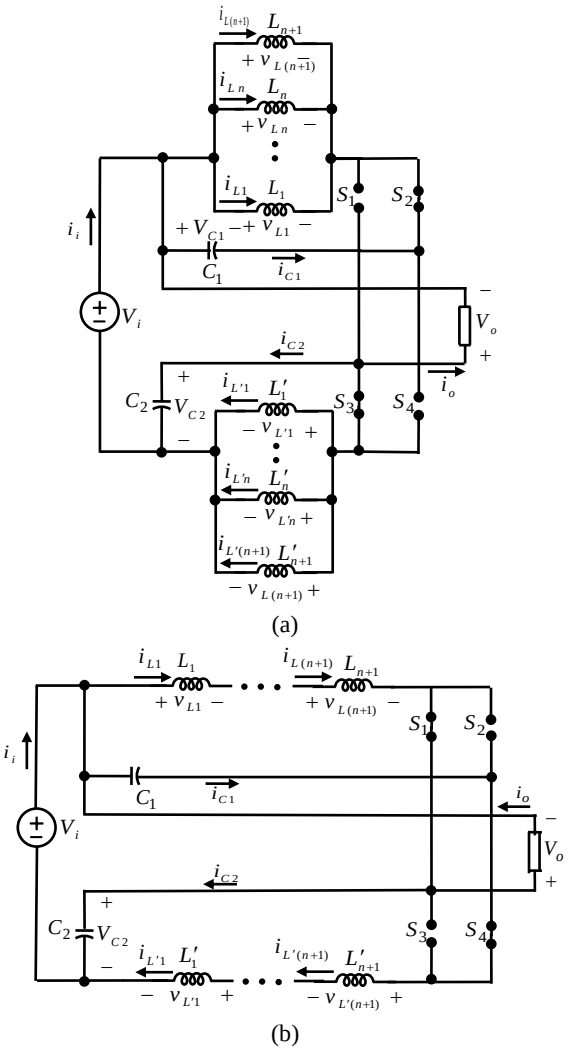


Fig. 3 Equivalent circuits of the proposed converter; (a) in time interval T_0; (b) in time interval T_1.

($C_1=C_2=C$), the following equations can be obtained:

$$V_{C1}=V_{C2}=V_C \quad (1)$$

$$v_{Ln}=v_{L'n}=v_{L(n+1)}=v_{L'(n+1)}=v_L \quad (2)$$

$$v_{D(3n-1)}=v_{D(3n-2)}=v_{D'(3n-1)}=v_{D'(3n-2)}=v_D \quad (3)$$

$$v_{D3n}=v_{D'3n}=v_{D'} \quad (4)$$

where, V_C, v_L, v_D and $v_{D'}$ are the voltages across the capacitors (C_1 and C_2), the inductors (L_n, L_{n+1}, L'_n and L'_{n+1}), the diodes (D_{3n-1}, D_{3n-2}, D'_{3n-1} and D'_{3n-2}) and the diodes (D_{3n} and D'_{3n}), respectively.

Second Operating Mode (Time Interval T_1)

Fig. 3(b) shows the equivalent circuit of the converter in the second operating mode. In this operating mode,

the switches S_1 and S_4 and the diodes D_{3n} and D'_{3n} are on and the switches S_2 and S_3 and the diodes D_{3n-1}, D_{3n-2}, D'_{3n-1} and D'_{3n-2} are off. So, in the upper switched-inductor cell, the inductors L_n and L_{n+1} and in the lower switched-inductor cell, the inductors L'_n and L'_{n+1} will be in series. In this operating mode, in the first operating zone, the inductors L_n and L_{n+1} are discharged by the capacitor C_2 and source V_i, and the inductors L'_n and L'_{n+1} are discharged by capacitor C_1 and the source V_i, whereas in the second operating zone, $D=(\frac{1}{N+2},\ 1]$, the inductors L_n and L_{n+1} are charged by the capacitor C_2 and source V_i, and the inductors L'_n and L'_{n+1} are charged by capacitor C_1 and the source V_i.

A. Extraction the Equations of Voltage Gain and Voltage across Componentes

The average values of voltage across capacitors (V_C) and output voltage (V_o) in both the operating zones are calculated as:

$$V_C=\frac{1-D}{1-(N+2)D}V_i>0 \quad for \quad D=[0,\ \frac{1}{N+2})$$
$$=\frac{1-D}{1-(N+2)D}V_i<0 \quad for \quad D=(\frac{1}{N+2},\ 1] \qquad (5)$$

$$V_o=\frac{(N+1)D}{1-(N+2)D}V_i>0 \quad for \quad D=[0,\ \frac{1}{N+2})$$
$$=\frac{(N+1)D}{1-(N+2)D}V_i<0 \quad for \quad D=(\frac{1}{N+2},\ 1] \qquad (6)$$

where, $D=T_0/T$ is the duty cycle of switches S_2 and S_3.

Considering (6), the buck-boost factor (B) of the converter can be defined as:

$$B=\frac{V_o}{V_i}=\frac{(N+1)D}{1-(N+2)D}$$
$$for \quad D=[0,\ \frac{1}{N+2}) \ \&\ D=(\frac{1}{N+2},\ 1] \qquad (7)$$

According to the above equation, in the first operating zone, the voltage gain has the values of $0\le B\le 1$ (as buck) and $1\le B\le\sim+\infty$ (as boost) and in the second operating zone, the voltage gain has the values of $\sim-\infty<B\le-1$ (as boost).

As presented in (7), the voltage gain (B) is more dependent to duty cycle (D) in comparison to the number of the switched-inductor cells (N). The proposed converter can provide high voltage gain in low duty cycles. Also, this can be seen in Fig. 4. In the first operating zone, D is limited as $D<1/(N+2)$, which is derived by setting the denominator of (7) to be greather than zero. By increasing N, the boundary of D will be adjusted and therefore D will be more controllable. However, by increasing N, the sensitivity of the voltage gain to D will be increased. So, it is suggested to use small number of switched-inductor cells.

Considering (1) to (7), the proportion of the voltage stress across capacitors to the input voltage and the voltage gain with respect to the duty cycle under different number of switched-inductor cells for two buck-boost and boost operating zones, are illustrated in Fig. 4. From Fig. 4 it can be observed that:

- ✓ The duty cycle is divided into two operating zones, as $D=[0,\ \frac{1}{N+2})$ and $D=(\frac{1}{N+2},\ 1]$, where in the first operating zone, the output voltage is positive and in the second one, the output voltage is negative.
- ✓ In $D=[0,\ \frac{1}{N+2})$ operation zone, the proposed converter acts as buck-boost (buck in $0\le D\le\frac{1}{2N+3}$ and boost in $\frac{1}{2N+3}\le D<\frac{1}{N+2}$.

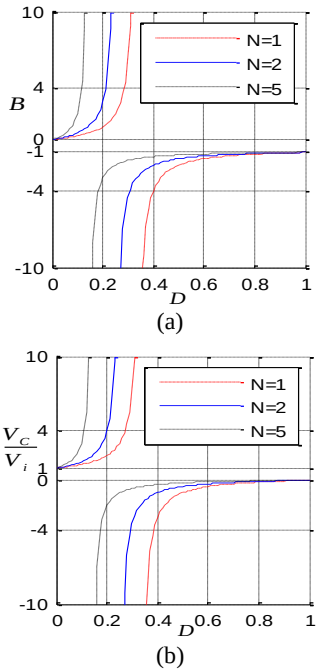


Fig. 4 (a) Variations of voltage stress across capacitors to input voltage; (b) Variations of boost (buck) factor, with respect to duty cycle.

- ✓ The proposed converter operates as a boost converter in the second operating zone.
- ✓ The voltage stresses across capacitors are different in two operating zones.
- ✓ The minimum value of voltage stress, in the second operating zone, is zero. So, in this operating zone, the voltage stress across capacitors is lower.
- ✓ The number of switched-indctor cells can be increased to the point that the stability ranges are not violated.

The voltages across inductors and diodes in the time intervals T_0 and T_1 can be obtained as:

$$v_{L,T0} = V_{D',T0} = \frac{1-D}{1-(N+2)D} V_i > 0 \; for \; D = [0, \frac{1}{N+2}) = \frac{1-D}{1-(N+2)D} V_i < 0 \; for \; D = (\frac{1}{N+2}, 1] \quad (8)$$

$$v_{L,T1} = -\frac{D}{1-(N+2)D} V_i > 0 \; for \; D = [0, \frac{1}{N+2}) = -\frac{D}{1-(N+2)D} V_i < 0 \; for \; D = (\frac{1}{N+2}, 1] \quad (9)$$

$$V_{D,T0} = V_{D',T1} = 0 \quad (10)$$

$$V_{D,T1} = \frac{D}{1-(N+2)D} V_i > 0 \; for \; D = [0, \frac{1}{N+2}) = \frac{D}{1-(N+2)D} V_i < 0 \; for \; D = (\frac{1}{N+2}, 1] \quad (11)$$

B. Extraction of Equations of Currents

First Operating Mode (Time Interval T_0)

Assuming that the output load is pure resistive, the instantaneous current flowing through the load will be equal to the average current flowing through the load ($I_{o,av}$), in both the operating zones and in both the time intervals T_0 and T_1. Therefore, this results that

$$i_{o,T0} = i_{o,T1} = I_{o,av} = \frac{V_o}{R} \quad (12)$$

Considering Fig. 3(a), the instantaneous current flowing through the inductors L_{n+1} and L'_{n+1}, in the time interval T_0 can be obtained as:

$$i_{L(n+1),T0} = \frac{V_C}{L_{n+1}} t + I_{1,L(n+1)} \quad (13)$$

$$i_{L'(n+1),T0} = \frac{V_C}{L'_{n+1}} t + I_{1,L'(n+1)} \quad (14)$$

where $I_{1,L(n+1)}$ and $I_{1,L'(n+1)}$ are initial values of currents flowing through the inductors L_{n+1} and L'_{n+1}, in the time interval T_0.

By replacing $t = T_0 = DT$ in (13) and (14), the maximum current flowing through inductors L_{n+1} and L'_{n+1} ($I_{2,L(n+1)}, I_{2,L'(n+1)}$), at the end of time interval T_0, can be obtained as follows:

$$i_{L(n+1),T0}\Big|_{t=T0=DT} = I_{2,L(n+1)} = \frac{V_C}{L_{n+1}} DT + I_{1,L(n+1)} \quad (15)$$

$$i_{L'(n+1),T0}\Big|_{t=T0=DT} = I_{2,L'(n+1)} = \frac{V_C}{L'_{n+1}} DT + I_{1,L'(n+1)} \quad (16)$$

Considering (12) to (14) and applying KCL in Fig. 3(a), the instantaneous currents through the capacitors C_1 and C_2 at the end of the time interval T_0 are calculated as follows:

$$i_{C1,T0} = \frac{-(N+1)V_C}{L_{n+1}} t - (N+1) I_{1,L(n+1)} \quad (17)$$

$$i_{C2,T0} = \frac{-(N+1)V_C}{L'_{n+1}} t - (N+1) I_{1,L'(n+1)} - \frac{V_o}{R} \quad (18)$$

Second Operating Mode (Time Interval T_1)

In the second operating mode, the currents of inductors L_{n+1} and L'_{n+1} are given by

$$i_{L(n+1),T1} = \frac{V_i - V_C}{(N+1)L_{n+1}} t + I_{2,L(n+1)} \quad (19)$$

$$i_{L'(n+1),T1} = \frac{V_i - V_C}{(N+1)L'_{n+1}} t + I_{2,L'(n+1)} \quad (20)$$

By applying KCL in Fig. 3(b) and considering (12), (19) and (20), the instantaneous currents through the capacitors C_1 and C_2 at the end of the time interval T_1 are obtained as follows:

$$i_{C1,T1} = \frac{V_i - V_C}{(N+1)L'_{n+1}} t + I_{2,L'(n+1)} \quad (21)$$

$$i_{C2,T1} = \frac{V_i - V_C}{(N+1)L_{n+1}} t + I_{2,L(n+1)} - \frac{V_o}{R} \quad (22)$$

$$i_{i,T1} = \frac{V_i - V_C}{(N+1)} \left(\frac{1}{L_{n+1}} + \frac{1}{L'_{n+1}} \right) t + I_{2,L(n+1)} + I_{2,L'(n+1)} - \frac{V_o}{R} \quad (23)$$

According to the current balance law, the average value of currents through capacitors over the switching period equals to zero. So, considering (17), (18), (21) and (22), we have:

$$\frac{1}{T}\int_0^T i_{C1}dt = \int_0^{T_0}\left(\frac{-(N+1)V_C}{L_{n+1}}t-(N+1)I_{1,L(n+1)}\right)dt + \int_0^{T_1}\left(\frac{V_i-V_C}{(N+1)L'_{n+1}}t+I_{2,L'(n+1)}\right)dt = 0 \quad (24)$$

$$\frac{1}{T}\int_0^T i_{C2}dt = \int_0^{T_0}\left(\frac{-(N+1)V_C}{L'_{n+1}}t-(N+1)I_{1,L'(n+1)}-\frac{V_o}{R}\right)dt + \int_0^{T_1}\left(\frac{V_i-V_C}{(N+1)L_{n+1}}t+I_{2,L(n+1)}-\frac{V_o}{R}\right)dt = 0 \quad (25)$$

By simplifying the above equations, replacing V_C from (5) and considering $L_{n+1}=L'_{n+1}$, the maximum current flowing through the inductor L'_{n+1} is obtained as:

$$I_{2,L'(n+1)} = \frac{D(1+ND)V_i}{2L_{n+1}f\,[1-(N+2)D]} + \frac{(N+1)DI_{1,L(n+1)}}{(1-D)} \quad (26)$$

Considering V_C from (5) and replacing $I_{2,L'(n+1)}$ from (26) in (24), we have:

$$I_{1,L(n+1)} = \frac{(1-D)DV_i}{[1-(N+2)D)]}\left(\frac{(N+1)}{R[1-(N+2)D)](1+ND)}-\frac{1}{2L_{n+1}f}\right) \quad (27)$$

Replacing $I_{1,L(n+1)}$ from (27) in (15), (16) and (26) and considering $L_{n+1}=L'_{n+1}$, the following results are obtained:

$$I_{2,L(n+1)} = \frac{(1-D)DV_i}{[1-(N+2)D)]}\left(\frac{(N+1)}{R[1-(N+2)D)](1+ND)}+\frac{1}{2L_{n+1}f}\right) \quad (28)$$

$$I_{2,L'(n+1)} = \frac{DV_i}{[1-(N+2)D)]}\left(\frac{(N+1)^2D}{R[1-(N+2)D)](1+ND)}+\frac{1-D}{2L'_{n+1}f}\right) \quad (29)$$

$$I_{1,L'(n+1)} = \frac{DV_i}{[1-(N+2)D)]}\left(\frac{(N+1)^2D}{R[1-(N+2)D)](1+ND)}-\frac{1-D}{2L'_{n+1}f}\right) \quad (30)$$

The current ripple of inductor is obtained from the difference of its maximum and minimum values. So, considering (27) to (30), the current ripple of inductors is calculated as follows:

$$I_{PP,L(n+1)} = I_{2,L(n+1)} - I_{1,L(n+1)} = \frac{(1-D)DV_i}{L_{n+1}f\,[1-(N+2)D)]} \quad (31)$$

$$I_{PP,L'(n+1)} = I_{2,L'(n+1)} - I_{1,L'(n+1)} = \frac{(1-D)DV_i}{L'_{n+1}f\,[1-(N+2)D)]} \quad (32)$$

where $I_{PP,L(n+1)}$ and $I_{PP,L'(n+1)}$ are the current ripple of inductors L_{n+1} and L'_{n+1}, respectively.

Considering (31) and (32), it can be observed that $I_{PP,L(n+1)}=I_{PP,L'(n+1)}$, in other words, although the instantaneous current of inductors L_{n+1} and L'_{n+1} are not equal but their current ripples are equal.

The average value of inductor current ($I_{L,av}$) can be defined as:

$$I_{L,av} = \frac{I_1+I_2}{2} \quad (33)$$

Considering (27) to (30) and (33), the average value of inductors current ($I_{L(n+1),av}$, $I_{L'(n+1),av}$) can be calculated as follows:

$$I_{L(n+1),av} = \frac{(1-D)DV_i}{[1-(N+2)D)]}\left(\frac{(N+1)}{R[1-(N+2)D)](1+ND)}\right) \quad (34)$$

$$I_{L'(n+1),av} = \frac{DV_i}{[1-(N+2)D)]}\left(\frac{(N+1)^2D}{R[1-(N+2)D)](1+ND)}\right) \quad (35)$$

Considering i_{C1} and i_{C2} from (21) and (22), the voltage ripple of capacitors can be obtained as follows:

$$V_{PP,C1} = \frac{1}{C_1}\int_0^{T_1} i_{C1}dt = \frac{1}{C_1}\left(\frac{(V_i-V_C)(1-D)^2}{2(N+1)L'_{n+1}f^2}+\frac{I_{2,L'(n+1)}(1-D)}{f}\right) \quad (36)$$

$$V_{PP,C2} = \frac{1}{C_2}\int_0^{T_1} i_{C2}dt = \frac{1}{C_2}\left(\frac{(V_i-V_C)(1-D)^2}{2(N+1)L_{n+1}f^2}+\frac{I_{2,L(n+1)}(1-D)}{f}-\frac{V_o(1-D)}{Rf}\right) \quad (37)$$

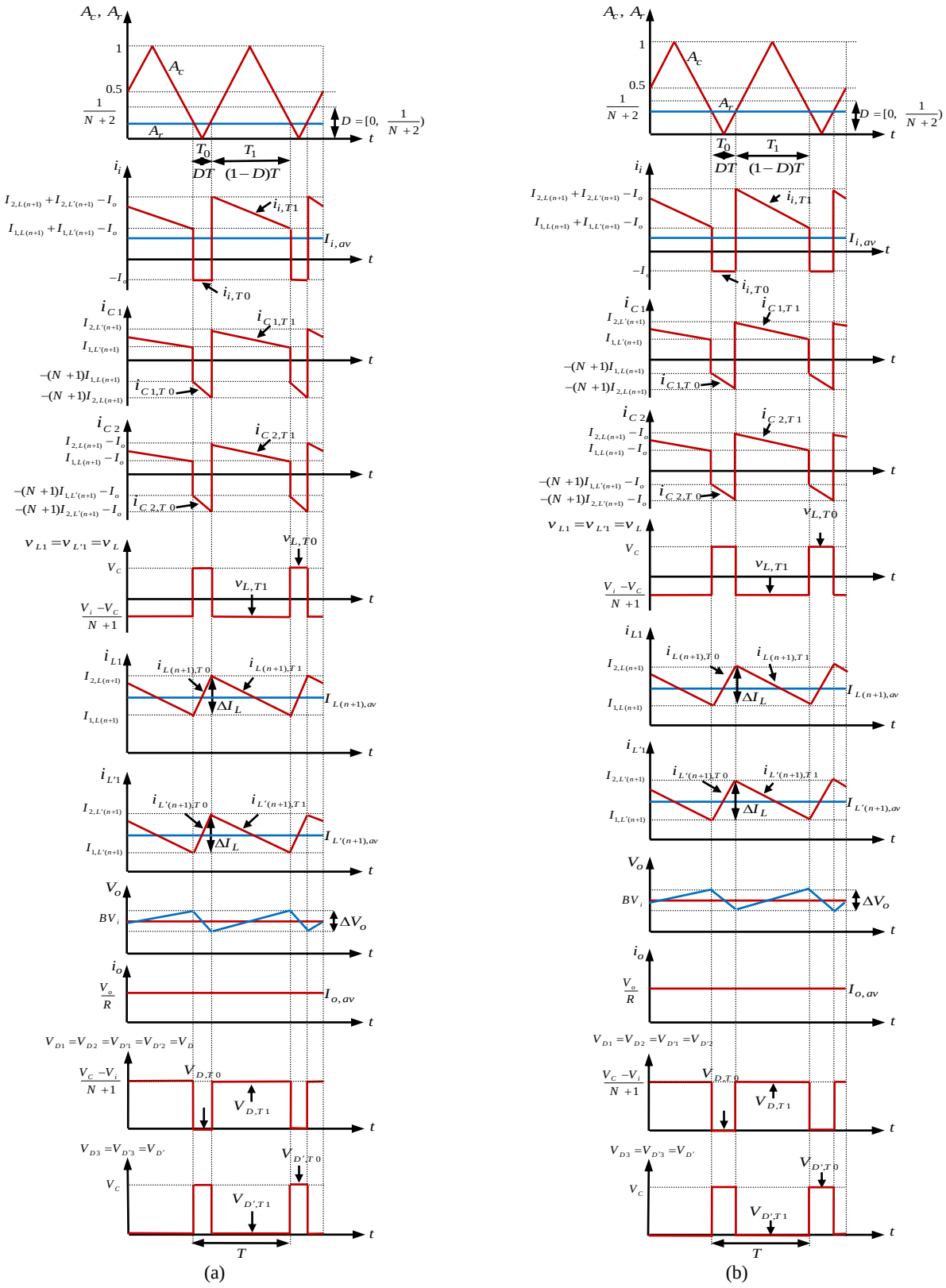


Fig. 5 Voltage and current waveforms in the first operating zone where $D=[0,\frac{1}{N+2})$; (a) buck; (b) boost.

By replacing V_C , $I_{2,L(n+1)}$ and $I_{2,L'(n+1)}$ from (5), (28) and (29) in (36) and (37), then simplifying them, we have:

$$V_{PP,C1} = \frac{(N+1)^2 D^2 (1-D) V_i}{RC_1 f\,[1-(N+2)D)]^2 (1+ND)} \quad (38)$$

$$V_{PP,C2} = \frac{(N+1)D^2 (1-D)[1+(N+2)ND]V_i}{RC_2 f\,[1-(N+2)D)]^2 (1+ND)} \quad (39)$$

According to extracted equations, the voltage and current waveforms of the proposed converter in the first operating zone for buck and boost operation modes are shown in Figs. 5(a) and 5(b), respectively.

3 Designing of Values of L and C

Ripples of capacitor voltage and inductor current affect the stability of the converters. To properly design the values of C_1 and C_2, the allowable voltage ripple X_C% may be used, which is defined as follows [24]:

$$x_{C1}\% = x_{C2}\% = x_C\% = \frac{V_{PP,C}}{V_C} \quad (40)$$

By substituting the values of V_C , $V_{PP,C1}$ and $.V_{PP,C2}$. from (5), (38) and (39) into (40), the rated value of C_1 and C_2 are calculated as follows:

$$C_1 = \frac{(N+1)^2 D^2}{Rf\,[1-(N+2)D)](1+ND)x_{C1}\%} \quad (41)$$

$$C_2 = \frac{(N+1)D^2[1+(N+2)ND]}{Rf\,[1-(N+2)D)](1+ND)x_{C_2}\%} \quad (42)$$

To properly design the values of L_{n+1} and L'_{n+1}, the allowable current ripples $x_{L(n+1)}$% and $x_{L'(n+1)}$% may be used, which are defined as follow:

$$x_{L(n+1)}\% = \frac{I_{PP,L(n+1)}}{I_{L(n+1),av}} \quad (43)$$

$$x_{L'(n+1)}\% = \frac{I_{PP,L'(n+1)}}{I_{L'(n+1),av}} \quad (44)$$

By substituting the values of $I_{PP,L(n+1)}$ and $I_{L(n+1),av}$ from (31) and (34) into (43), and by replacing the values of $I_{PP,L'(n+1)}$ and $I_{L'(n+1),av}$ from (32) and (35) into (44), the rated values of L_1 and L_2, are calculated as follow:

$$L_{n+1} = \frac{\left(1-(N+2)D\right)(1+ND)R_L}{(N+1)f\ x_{L(n+1)}\%} \quad (45)$$

Table 1 Comparison of characteristics for variety of the buck and boost converters.

Converter	Voltage Gain (V_o/V_i)	Stress voltage across the capacitors (V_C)	Advantages	Disadvantages	Some features
The conventional Z-source Converter	$\frac{1}{1-2D}$	$\frac{1-D}{1-2D}$	- Having two operating zones - Step-down and step-up capability - Using in all of conversions	- Needing one switch (or diode) before the LC network - Diode prevents the reverse current.	Diode creates an unpleasant operation mode in during the non-ST switching state.
The conventional Z-H boost converter	$\frac{1}{1-2D}$	$\frac{1-D}{1-2D}$	- Having two operating zones - Elimination of diode before the LC network - Using in all of conversions without any change in its topology	-Needing four bidirectional switches in all of conversions	It has only step-up capability.
The conventional Z-H buck converter	$1-2D$	D	- Having two operating zones - Elimination of diode before the LC network - Using in all of conversions without any change in its topology	- Needing four unidirectional switches in dc/dc, dc/ac and ac/dc conversions - Needing four bidirectional switches in ac/ac conversions	It has only step-down capability.
The Z-H buck-boost converter [21]	$\frac{D}{1-2D}$	$\frac{1-D}{1-2D}$	- Having two operating zones - Elimination of diode before the LC network - Step-down and step-up capability - Using in dc/dc, dc/ac and ac/ac conversions without any change in its topology	Needing four bidirectional switches	In this converter, in the denominator of the voltage gain, the factor of the duty cycle is 2. So, the converter will have the maximum voltage gain when duty cycle is close to half.
The proposed buck-boost Z-H converter	$\frac{(N+1)D}{1-(N+2)D}$	$\frac{1-D}{1-(N+2)D}$	- Having two operating zones - Elimination diode before the LC network - Can provide high voltage gain in low duty cycles. - Using in dc/dc, dc/ac and ac/ac conversions without any change in its topology	Needing four bidirectional switches	In $D=[0, \frac{1}{N+2})$ this converter works in buck-boost operation and in $D=(\frac{1}{N+2}, 1]$ it works in boost operation.

$$L'_{n+1} = \frac{(1-(N+2)D)(1+ND)(1-D)R_L}{D(N+1)^2 f\, x_{L'(n+1)}\%} \quad (46)$$

4 Comparison of the Proposed and Some of the Similar Converters

The proposed converter has multiple advantages. It can produce lower or higher voltage than the input voltage; due to the existence of LC network, the reliability of the converter is increased; it can be applied for dc-dc, dc-ac and ac-dc conversions without any change in its structure; moreover, it eliminates ST switching state due to Z-source LC network.

A comparison between conventional Z-source inverter, conventional Z-H buck and boost converters, the Z-H buck-boost converter [21] and the proposed buck-boost Z-H converter are shown in Table 1.

Although the proposed converter has higher number of the passive and active elements in comparison to some of the presented converters, it provides multiple advantages.

In conventional Z-source inverters, number of the switches is higher than the proposed converter. Also, the conventional Z-source inverter has a front-end diode that it adds to the losses of the inverter. Therefore, in similar conditions, according to [21], power loss of the conventional Z-source inverter is higher than the power loss of the proposed converter and this shows the higher efficiency of the proposed switched-inductor based Z-H buck-boost converter.

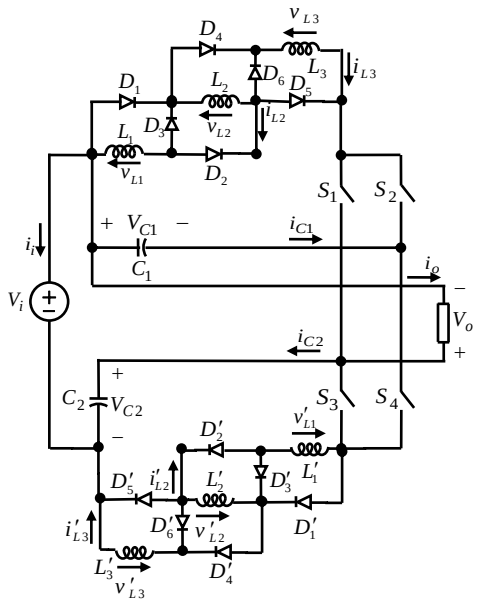


Fig. 6 Proposed converter in two-cell switched inductor structure.

Table 2 Values of utilized parameters in the simulation

f_s	Output load (R_L)	LC network $C_1 = C_2$	LC network $L_1 = L_2$	V_i	Duty Cycle	
$25kHz$	5Ω	$50\mu F$	$500\mu H$	$20V$	$D = 0.1$	Buck
	200Ω				$D = 0.2$	Boost

5 Simulation Results

In order to evaluate the operation accuracy of the proposed converter, the simulation results in PSCAD/EMTDC software are presented. The proposed converter in two-cell switched inductor structure is shown in Fig. 6. Table 2 gives the values of the utilized parameters in the simulation. Fig. 7 illustrates the simulation results in the first operating zone for buck operation by assuming $B = 0.5$, $D = 0.1$ and $N = 2$ and for boost operation by assuming $B = 3$, $D = 0.2$ and $N = 2$.

5.1 Calculation of the Values of the Capacitors and Inductors

Based on the explanations in section III, the values of capacitors and inductors can be obtained as follow:

For $D = 0.1$, $N = 2$, $I_{PP,L(n+1)} = I_{PP,L'(n+1)} = 0.24A$, $V_C = 30V$, $V_{PP,C1} = 0.6V$ and $V_{PP,C2} = 0.36V$ the values of inductors and capacitors can be calculated as follow:

From (40), the allowable voltage ripples $x_{C1}\%$ and $x_{C2}\%$ are given by:

$$x_{C1}\% = \frac{V_{PP,C1}}{V_C} = \frac{0.6}{30} = 0.02$$

$$x_{C2}\% = \frac{V_{PP,C2}}{V_C} = \frac{0.36}{30} = 0.012$$

From (41) and (42), the rated value of the capacitances C_1 and C_2 is equal to:

$$C_1 = \frac{(N+1)^2 D^2}{Rf\,[1-(N+2)D)](1+ND)x_{C1}\%} = 50\mu F$$

$$C_2 = \frac{(N+1)D^2[1+(N+2)ND]}{Rf\,[1-(N+2)D)](1+ND)x_{C_2}\%} = 50\mu F$$

From (43) and (44), the allowable current ripples $x_{L(n+1)}\%$ and $x_{L'(n+1)}\%$ are given by:

$$x_{L(n+1)}\% = \frac{I_{PP,L(n+1)}}{I_{L(n+1),av}} = 0.096$$

$$x_{L'(n+1)}\% = \frac{I_{PP,L'(n+1)}}{I_{L'(n+1),av}} = 0.28$$

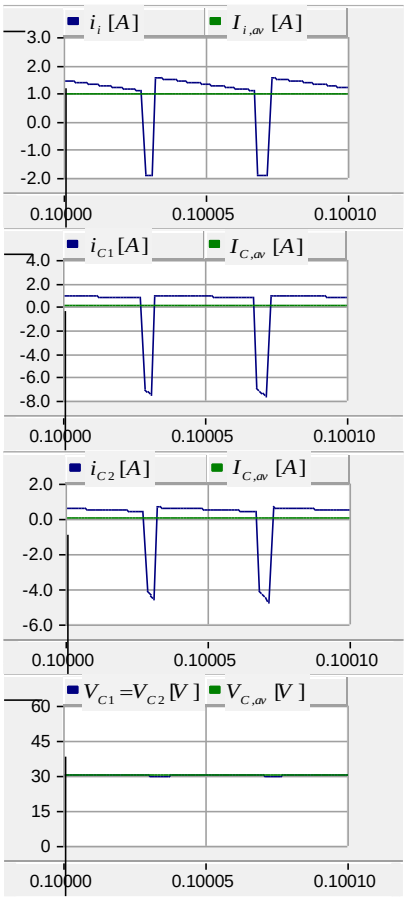
From (45) and (46), the rated values of the inductances L_1 and L_2 are equal to:

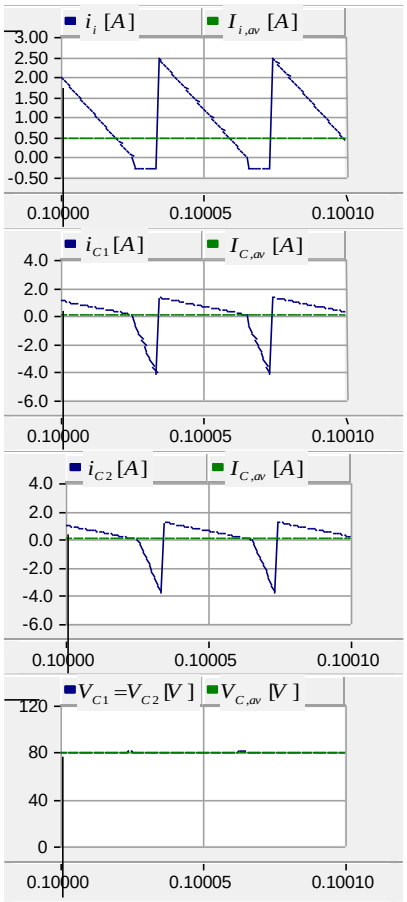
$$L_{n+1}=\frac{\left(1-(N+2)D\right)(1+ND)R_L}{(N+1)f\ x_{L(n+1)}\%}=500\mu H$$

$$L'_{n+1}=\frac{\left(1-(N+2)D\right)(1+ND)(1-D)R_L}{D(N+1)^2 f\ x_{L'(n+1)}\%}=500\mu H$$

5.2 Calculation of Voltages and Currents Values

The following results are obtained considering $B=0.5$, $D=0.1$ and $N=2$. From (6) and (12), the output voltage and current of the converter in the time intervals T_0 and T_1 are as $V_o=10V$ and $i_o=2A$, respectively. Considering (5), the average voltage across capacitors C_1 and C_2 in both the time intervals is $V_C=30V$. From (8) to (11), the values of the voltages across inductors and diodes, in the time intervals T_0 and T_1 are obtained as $v_{L,T0}=V_{D',T0}=30V$, $v_{L,T1}=-3.3V$, $V_{D,T0}=V_{D',T1}=0$ and $V_{D,T1}=3.3V$. From (27)-(30), the current values of the inductors L_3 and L'_3 at the end of the time intervals T_0 and T_1 are as $I_{1,L3}=2.38$, $I_{2,L3}=2.62$, $I_{2,L'3}=0.95$ and $I_{1,L'3}=0.71$, respectively. By replacing $t=T_0=DT$ in (17) and (18), the instantaneous currents through the capacitors C_1 and C_2 at the end of the time interval T_0 are obtained as $i_{C1,T0}=-7.86$ and $i_{C2,T0}=-4.85$. By replacing $t=T_1=(1-D)T$ in (21)-(23), the instantaneous currents through the capacitors C_1 and C_2 at the end of the time interval T_1 are obtained as $i_{C1,T1}=0.71$, $i_{C2,T1}=0.38$ and $i_{i,T1}=1.09$. According to (31) and (32), the value of current ripples of the inductors is obtained as $I_{PP,L3}=I_{PP,L'3}=0.24A$. Considering (34) and (35), the average value of inductors current are obtained as $I_{L3,av}=2.5A$ and $I_{L'3,av}=0.83A$. From (38) and (39), the voltage ripple of capacitors C_1 and C_2 are obtained as $V_{PP,C1}=0.6V$ and $V_{PP,C2}=0.36V$, respectively. The results obtained from the simulations confirm the accuracy of the theoretical calculations and correspond to the waveforms illustrated in Fig. 5(a). The above calculations are for the buck operation and in the same way; they can be repeated for the boost operation.





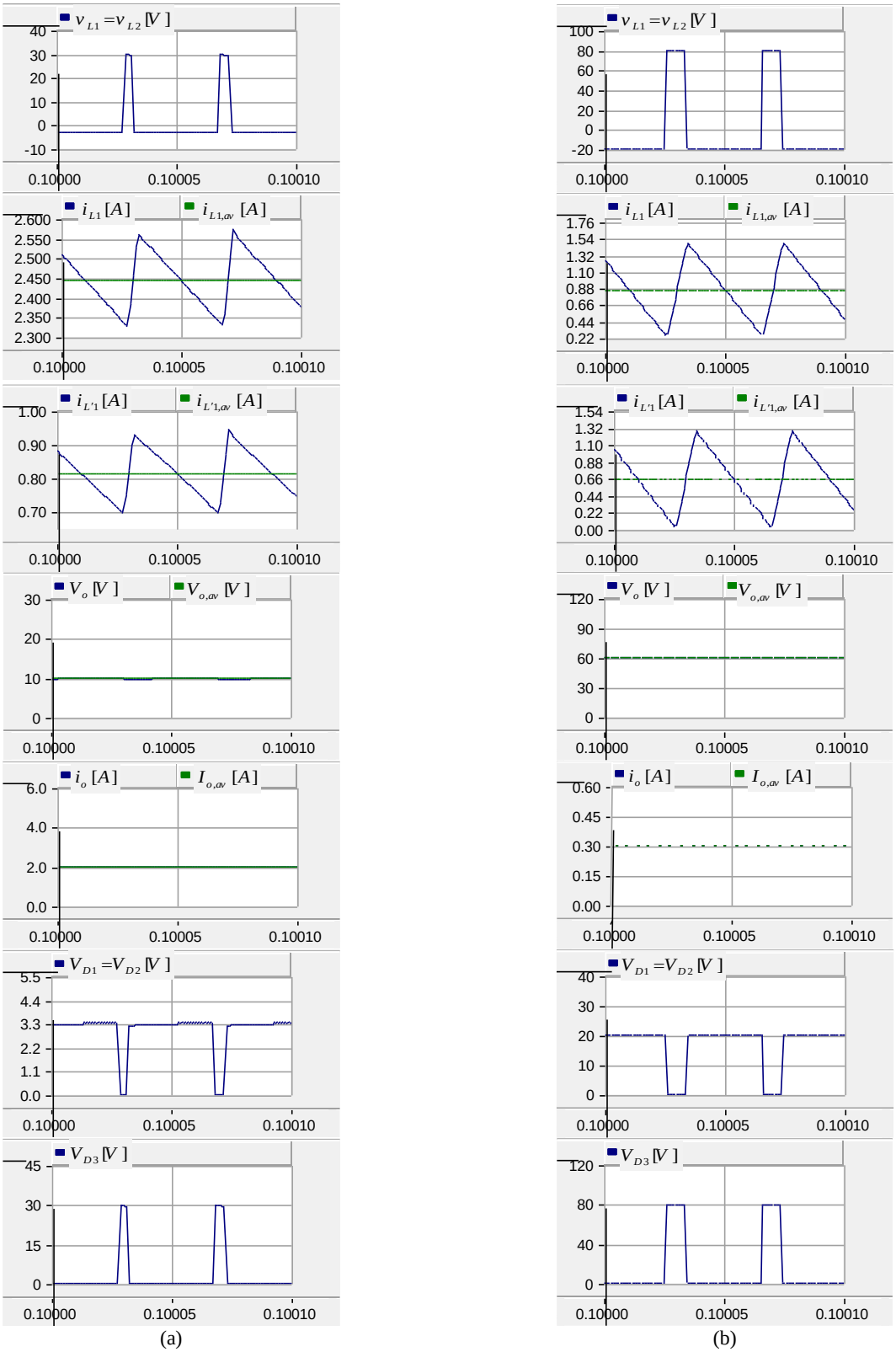


Fig. 7 Simulation results of the proposed converter in the first operating zone as $D=[0,\ \frac{1}{N+2})$; (a) buck operation for $B=0.5$, $D=0.1$ and $N=2$; (b) boost operation for $B=3$, $D=0.2$ and $N=2$.

6 Conclusion

In this paper, a generalized Z-H buck-boost converter with switched inductor cells was proposed. The operation principles were given and voltage and current equations of all the components were presented. It was shown that the proposed structure can work in both buck and boost operating modes; the voltage gain can be increased by adjusting the duty cycle and changing the number of switched inductor cells; due to the elimination of the diode before LC network the reverse flow of energy is possible; and due to Z-H structutre, there is no ST switching state and there is no need for additional filter. The current and voltage ripple equations of the components of the proposed structure were obtained. Also, the optimum values of the inductors and the capacitors were given. In order to confirm the accuracy of the calculations, the simulation results were performed and presented for $N = 2$ cells. It was observed that the simulation results were in accordance with the mathematical calculations.

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