Realization of Novel Cascadable Current-Mode All-pass Sections

A. Kumar* and B. Chaturvedi*(C.A.)

Abstract: This paper introduces four new resistorless circuits of first-order current-mode all-pass filter (CMAPF) based on dual-X current conveyor transconductance amplifier (DXCCTA). All the four circuits use a single DXCCTA and a capacitor for their realization. The main features of the proposed CMAPFs are: use of minimum active and passive components, resistorless realization, electronically adjustable pole frequency, easily cascadable, good sensitivity performance with respect to active and passive elements, low total harmonic distortion of output current (0.74%) and good operating frequency range (39.2 MHz). The non-ideal analysis of the proposed circuits has also been explored. Moreover, two applications of the proposed first-order CMAPF in terms of second order CMAPF and current-mode quadrature oscillator are also presented. HSPICE simulations have been carried out with 0.18 µm CMOS process parameters to validate the proposed circuits.

Keywords: All-pass Filter, Quadrature Oscillator, Electronic Tuning, Cascadable, DXCCTA.

1 Introduction

The wide range of applications of all-pass filters (APFs) have made them important cell for communication systems. Their main applications include phase shifters while maintaining amplitude to be constant, generation of quadrature signals or multiphase signals [1] and design of high-Q band-pass circuits. Both the voltage-mode as well as current-mode first-order APFs based on numerous high performance active elements are presented in the literature [2-23]. However, current-mode circuits have gained significant attention because they have increased bandwidth, simple structures of circuits, widespread dynamic range and low power consumption [24]. Therefore, designers have shown interest to develop the first order current-mode all-pass filter (CMAPFs) while focusing on reducing the number of active and passive elements, resistor less realization, ease of cascadability, electronic tunability of pole frequency etc.

The circuits of APFs presented in [2,4-9,11-16,18,19] have the advantage of cascadability and do not have any component matching restrictions. Additionally the circuits presented in [2-5,7,9,12,14,15,17,18,20,21,23] are based on single active element and circuits presented in [2,3,9-16,19] have the property of electronic tuning. However, these APFs suffer from one or more of the following weaknesses; no resistorless realization [4-7,9,17,18,20-23], no electronic tuning [4-8,17-18,20-23], use of more than one passive components [4-7,9,17,18,20-23] and lower pole frequency [2-23].

In this paper four novel circuits of CMAPF that comprise single dual-X current conveyor transconductance amplifier (DXCCTA) [25] and a capacitor are proposed. Thus, no external resistor is required for their realization. The input impedance of the proposed CMAPFs is low and output impedance is high. Therefore, the proposed circuits can be easily cascadable. Moreover, the pole frequency is electronically tunable. The sensitivity performance of the proposed circuits is also found good. Furthermore, the presented CMAPFs exhibit low total harmonic distortion (THD) for the output current. A comparison of the presented CMAPFs with few of the previously presented CMAPFs has shown favorable performance.
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Two applications in terms of second order CMAPF and current-mode quadrature oscillator (CM-QO) are also given. HSPICE simulation results using 0.18 µm are depicted to examine the performance of the presented circuits.

2 DXCCTA Basics

DXCCTA [25] combines the feature of both DXCCII [26] and OTA. The symbol and CMOS implementation of DXCCTA are shown in Fig. 1(a) and (b), respectively. In CMOS implementation of DXCCTA, the MOS transistors, M1-M30 form the input stage, DXCCII and MOS transistors, M21-M32 form the output stage, OTA. The current mirror formed by M14 and M15 forces the drain currents of M1 and M2 to be equal. Thus, voltage of X+ terminal becomes equal to voltage of Y terminal. The transistors M1-M5, M16-M18 form the inverting voltage follower which causes the voltage at terminal, Y to be followed in inverting manner by voltage at terminal, X-. Moreover, the gate voltages of M12 and M13 are equal which causes the current at terminal, X+ to be followed by current at terminal, Z+.

Similarly the current of terminal, X- is transferred to the terminal, Z-. In OTA stage, the MOS transistors, M21-M22, M25-M26 form a single input balanced output differential amplifier. The current mirrors formed by MOS transistors M24-M25, M26-M27 and M31-M32 cause the output of differential amplifier to appear at terminal, O+. The MOS transistors, M33, M35-M36 form an inverter thus, current at O- terminal flows in opposite direction of current at O- terminal. The following hybrid matrix gives the port relationships of DXCCTA

Table 1 Comparison of the proposed CMAPF with few of the already existing APFs.

<table>
<thead>
<tr>
<th>Ref. No.</th>
<th>ABB used</th>
<th>ABB count</th>
<th>Passive components count</th>
<th>Resistorless realization</th>
<th>Cascadable</th>
<th>Component matching constraints</th>
<th>Electronic tunability</th>
<th>CMOS technology (µm)</th>
<th>Operational frequency (MHz)</th>
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<tr>
<td>2</td>
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<td>Yes</td>
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<td>0.18</td>
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<td>Yes</td>
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<td>39.2</td>
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</table>

The transconductance, $g_m$ in Eq. (1) depends on the bias current $I_B$ and it is expressed as

$$g_m = \frac{k_n I_B}{C_{OX} (W/L)}$$

where $k_n = \mu_n C_{OX} (W/L)$ is the physical parameter of MOS transistors. It is well known that physical parameter, $k_n$ is temperature dependent [27] thus, the transconductance, $g_m$ is also temperature dependent and its value decreases with increase in temperature.

### 3 Proposed First-order Current-mode All-pass Filters

The newly proposed first-order current-mode all-pass filters, CMAPF-I, CMAPF-II, CMAPF-III and CMAPF-IV are shown in Fig. 2(a), (b), (c) and (d), respectively. The CMAPF-I and CMAPF-III employ one DXCCTA and one capacitor only whereas, CMAPF-II and CMAPF-IV employ one multiple output DXCCTA along with a single capacitor. It is to be mentioned that in case of CMAPF-III and CMAPF-IV the voltage of Z+ terminal ($V_{Z+}$) is transferred in terms of current to the O+ and O- terminals instead of voltage of Z-terminal ($V_Z$). Therefore, a little change in CMOS implementation (terminal Z+ is connected to the gate of $M_{21}$ instead of terminal Z-) is needed in case of CMAPF-III and CMAPF-IV. Using the port relationships of DXCCTA-IV, all the proposed CMAPFs are analyzed and transfer function obtained after analysis is given as follows:

$$I_{out} = \frac{s - g_{m}}{C}, \quad I_{in} = \frac{s + g_{m}}{C}$$

The pole frequency, $\omega_0$ and frequency dependent phase angle, $\phi(\omega)$ are given as

$$\omega_0 = \frac{g_m}{C} = \sqrt{k_n I_B}$$

$$\phi(\omega) = \pi - 2 \tan^{-1}\left(\frac{\alpha C}{g_{m}}\right)$$

It is to be noted from Eq. (3) that electronic adjustment of $\omega_0$ is possible by means of bias current $I_B$. Furthermore, the input impedance of all CMAPFs is low and output impedance of all CMAPFs is high. Thus all the proposed CMAPFs are easily cascadable.

### 3.1 Non-Ideal Analysis

The following equation gives the port relationships for the non-ideal model of DXCCTA

$$V_{X+} = \beta V_y, \quad V_{X-} = -\beta V_y,$$

$$I_{Z+} = \alpha_1 J_{X+}, \quad I_{Z-} = \alpha_2 J_{X-},$$

$$I_{O+} = \gamma_1 g_m V_{Z+}, \quad I_{O-} = -\gamma_2 g_m V_{Z-}$$

![Fig. 1 a) Symbol of DXCCTA, b) CMOS implementation of DXCCTA [25].](image1)

![Fig. 2 Proposed first-order current-mode all-pass filter circuits: a) CMAPF-I, b) CMAPF-II, c) CMAPF-III and d) CMAPF-IV.](image2)
where, $\beta_1$, $\beta_2$ and $\alpha_1$, $\alpha_2$ are the voltage transfer gains ($Y$ to $X+$, and $Y$ to $X-$) and current transfer gains ($X+$ to $Z+$, and $X-$ to $Z-$), respectively. The $\gamma_1$ and $\gamma_2$ are the transconductance inaccuracies from $Z$ to $O+$ terminal and from $Z$ to $O-$ terminal, respectively. It is to be further mentioned that in case of CMAPF-III and CMAPF-IV, the expressions of $I_{\text{out}}$ and $I_{\text{in}}$ are given as follows:

$$I_{\text{out}} = \gamma_1 g_m V_{Z+} \quad \text{and} \quad I_{\text{in}} = -\gamma_2 g_m V_{Z-}. \quad (6)$$

Considering the non-ideal port relationships given in Eq. (5) and (6), the all four CMAPFs are reanalyzed and provide the following transfer functions

CMAPF-I: $$\frac{I_{\text{out}}}{I_w} = \alpha_1 \alpha_2 \left[ \frac{s - \gamma_1 g_m}{\alpha_1 C} \right] \left[ \frac{s + \gamma_2 g_m}{s + \gamma_2 g_m} \right] \quad (7)$$

CMAPF-II: $$\frac{I_{\text{out}}}{I_w} = \alpha_2 (2\alpha_1 - 1) \left[ \frac{s - \gamma_1 g_m}{(2\alpha_1 - 1)C} \right] \left[ \frac{s + \gamma_2 g_m}{s + \gamma_2 g_m} \right] \quad (8)$$

CMAPF-III: $$\frac{I_{\text{out}}}{I_w} = \alpha_1 \alpha_2 \left[ \frac{s - \gamma_1 g_m}{\alpha_1 C} \right] \left[ \frac{s + \gamma_2 g_m}{s + \gamma_2 g_m} \right] \quad (9)$$

CMAPF-IV: $$\frac{I_{\text{out}}}{I_w} = \alpha_1 (2\alpha_2 - 1) \left[ \frac{s - \gamma_1 g_m}{(2\alpha_2 - 1)C} \right] \left[ \frac{s + \gamma_2 g_m}{s + \gamma_2 g_m} \right] \quad (10)$$

Equations (7) to (10) provide the following pole frequency

$$\omega_0 = \frac{\gamma_1 g_m}{C} \quad (11)$$

The sensitivities of $\omega_0$ with respect to active components and capacitor are given as

$$S_{\gamma_1}^{\omega_0} = S_{g_m}^{\omega_0} = 1 \quad , \quad S_{C}^{\omega_0} = -1 \quad \text{and} \quad S_{\alpha_1,\alpha_2}^{\omega_0} = 0 \quad (12)$$

Equation (12) reveals that none of the sensitivity is in excess of unity in magnitude. Therefore, the proposed CMAPFs enjoy good sensitivity performance.

4 Simulation Results

HSPICE simulation results using 0.18 µm CMOS process parameters have been carried out to validate the proposed circuits of CMAPF. The W/L ratios of MOS transistors are given in Table 2. The minimum length of transistors is selected (just double of the technology used) keeping in view the practical aspects of integration. The supply voltages of ± 1.25 V are used and biasing voltage used is $V_{BB} = 0.42$ V. The proposed filter is designed for 39.78 MHz frequency. The bias current is fixed to $I_B = 26$ µA for which value of $g_m$ is 0.5 mS. The value of capacitor used is $C = 2$ pF. Fig. 3 shows the simulated phase response along with the magnitude response. A 90° phase shift occurs at pole frequency of $f_0 = 39.2$ MHz (1.47% error) which is very close to the theoretically designed pole frequency. The transient responses of input and output at pole frequency are shown in Fig. 4(a) and their simulated frequency spectrums are depicted in Fig. 4(b). The Lissajous pattern shown in Fig. 4(c) confirms the quadrature relationship between input and output. The output waveform at pole frequency shows a total harmonic distortion (THD) of 0.74%. Additionally, the variation of THD (%) with the amplitude of input current is plotted in Fig. 5. It is to be noted from the Fig. 5 that for an amplitude range up to 50 µA, the THD is not higher than 2%.

Furthermore, the phase responses of output current for different values of bias current ($I_B = 20, 25, 30$ µA) are shown in Fig. 6. The pole frequency varying against the bias current $I_B$ is plotted in Fig. 7. The bias current is varied from 10 µA to 40 µA with 5 µA step size and a frequency range of 14 MHz to 56.1 MHz is achieved for this range of bias current. Next, the performance of the proposed circuit is tested for temperature variation. The input and output waveforms at different temperatures (25°C, 50°C, 75°C and 100°C) are shown in Fig. 8. The plot of variations of pole frequency and THD against the temperature is also shown in Fig. 9. As discussed in Section 2, the transconductance, $g_m$ decreases with increase in temperature therefore, the pole frequency also decreases with increase in temperature since pole frequency is directly proportional to $g_m$ as to be seen from Eq. (3). Fig. 9 shows that pole frequency decreases from 39.2 MHz to 33 MHz as temperature is increased from 25°C to 100°C. Moreover, THD of the output current varies from 0.74% to 0.92% when temperature is varied from 25°C to 100°C. It is to be observed that THD is less than 1% for a wide range of temperature variation.

<table>
<thead>
<tr>
<th>MOS Transistors</th>
<th>W(µm)/L(µm)</th>
</tr>
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<tbody>
<tr>
<td>M1, M2</td>
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</tr>
<tr>
<td>M3, M4, M5, M24, M25</td>
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<tr>
<td>M14, M15</td>
<td>1.34/0.36</td>
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<td>M16, M17, M18</td>
<td>2.40/0.36</td>
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<td>M21, M22</td>
<td>3.60/0.36</td>
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<td>M27, M28, M31, M32</td>
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</table>
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Fig. 3 Phase response and magnitude response.

Fig. 4 a) Transient responses of input and output at pole frequency, b) Frequency spectrums and c) Lissajous pattern at pole frequency.

Fig. 5 THD variation against input current $I_{in}$.

Fig. 6 Phase responses at different bias currents.

Fig. 7 Pole frequency variation against bias current, $I_B$.

Fig. 8 Input and output waveforms at different temperatures (25°C, 50°C, 75°C and 100°C).

Fig. 9 Pole frequency and THD variations against temperature.
5 Applications of the Proposed CMAPFs

5.1 Second Order CMAPF

To verify the property of cascadability of the proposed first order CMAPF-I, a second order CMAPF is realized by cascading the two first order CMAPF-I as shown in Fig. 10. The circuit employs two DXCCTA and two capacitors. The transfer function obtained from the analysis of circuit is given as

\[
\frac{I_{out}}{I_{in}} = \left( \frac{sC_1 - g_{m1}}{sC_1 + g_{m1}} \right) \left( \frac{sC_2 - g_{m2}}{sC_2 + g_{m2}} \right)
\]

(13)

The pole frequency and phase angle obtained from Eq. (13) are given as

\[
\omega_0 = \left( \frac{g_{m1} C_1}{C_2} \right)^{\frac{1}{2}}
\]

(14)

\[
\phi(\omega) = -2\tan^{-1} \left( \frac{\omega C_1}{g_{m1}} \right) - 2\tan^{-1} \left( \frac{\omega C_2}{g_{m2}} \right)
\]

(15)

It is clear from Eq. (15) that a second order all-pass filter provides a phase shift of 0º to -360º when frequency is varied from 0 to ∞.

The circuit of second order CMAPF is designed for a pole frequency of 39.7 MHz. The bias currents used are \( I_{B1} = I_{B2} = 26 \mu A \) for which \( g_m = 0.5 \) mS. Two capacitors used are \( C_1 = C_2 = 2 \) pF. Fig. 11 shows the simulated magnitude response and phase response. It is to be clearly seen from the Fig. 12(a) that input and output have a phase difference of 180º at the pole frequency.

Fig. 10 Circuit of the proposed second order CMAPF.

Fig. 11 Simulated phase and magnitude responses.

5.2 Current-Mode Quadrature Oscillator

A common technique to realize an oscillator circuit is to use an APF together with an integrator. The proposed current-mode quadrature oscillator (CM-QO) is also realized using CMAPF-I and an integrator formed with the help of DXCCTA. Fig. 13 shows the circuit of CM-QO. The characteristic equation obtained from the analysis of the circuit can be found as

\[
s^2 + \frac{\omega_0^2}{RC_2} - \frac{2g_m RC_2 C_1}{RC_2} + \frac{g_m}{RC_2} = 0
\]

(16)

The oscillation frequency \( f_0 \) and condition of oscillation (CO) from Eq. (16) are found as

\[
f_0 = \frac{1}{2\pi} \sqrt{\frac{g_m}{RC_1 C_2}}
\]

(17)

CO: \( g_m RC_2 \leq C_1 \)

(18)

For equal value of capacitors the CO in Eq. (18) becomes as

CO: \( g_m R \leq 1 \)

(19)

The quadrature current outputs \( I_1 \) and \( I_2 \) are related as

\[
I_1 = j \omega RC_1 I_2
\]

(20)

Equation (20) confirms the quadrature relationship between the two current outputs. 

The proposed CM-QO is designed for an oscillation...
Furthermore, the proposed CMAPF circuits are expected to find applications in single side band suppressed carrier modulation (SSB-SC) circuits and in phase equalizers. The proposed CM-QO can also be expected useful in many applications such as single side band generation, quadrature mixers, selective voltmeters etc. in the areas of communication and measurement systems.

References


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B. Chaturvedi received B. Tech. degree in Electronics and Communication Engineering and M. Tech. degree in Electronics Engineering, with specialization in Electronic Circuits and System Design. He has completed his Ph.D. in Electronics Engineering from Department of Electronics Engineering of Aligarh Muslim University, Aligarh, India. He is currently working as Assistant Professor in the Department of Electronics and Communication Engineering of Jaypee Institute of Information Technology, Noida, India. His research interests include Analog Signal Processing, Circuits and Systems. He has published more than 40 research papers in reputed international journals and conferences and also authored one book chapter.