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Switched-Capacitor Dynamic Threshold PMOS (SC-DTPMOS) Transistor for High Speed Sub-threshold Applications

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Abstract: This work studies the effects of dynamic threshold design techniques on the speed and power of digital circuits. A new dynamic threshold transistor structure has been proposed to improve performances of digital circuits. The proposed switched-capacitor dynamic threshold PMOS (SC-DTPMOS) scheme employs a capacitor along with an NMOS switch in order to effectively reduce the threshold voltage of a PMOS transistor. The proposed structure improves the propagation delay of a circuit and is much suitable for those circuits with high switching factor. Post layout simulation results using TSMC 180 nm CMOS technology at 0.2V supply voltage shows 45% improvement in delay as well as 25% less power consumption at the cost of only 53% more occupied area.

Keywords: Low Power, High Speed, Sub-threshold, Body Biasing, Dynamic Threshold.

1 Introduction

OVER the past four decades, the size of transistors has continuously been reduced to increase the device speed and density on a given chip and the die yield during manufacturing [1]. With the increasing demand for portable applications, low power, low energy VLSI design has been growing very rapidly over the recent years [2]. The most effective way to reduce energy dissipation is through reducing the supply voltage and this agrees with the continuing scaling down of the transistor size. Therefore, continuous reduction in the threshold voltage of the transistor, which ensures high drive current and hence performance improvements, is inevitable [1].

From another point of view, threshold voltage cannot be scaled down with the same rate due to the standby power considerations in static circuits and avoidance of failure in dynamic circuits [3,4]. As a result, there is a tradeoff between the standby power dissipation and the speed of a digital circuit.

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With the above mentioned discussion on scaling down of the supply voltage, the sub-threshold operation, where the supply voltage is lower than the threshold voltage, becomes a logical result [5,6]. In sub-threshold region, the speed of a transistor decreases due to its lower drive current. As a result, the delay of a circuit increases in the sub-threshold region. Several attempts have been done to overcome this problem [3,7-8]. Body biasing technique [9] is among the best ways to improve the performance of analog and digital circuits in sub-threshold region [10-12]. This technique benefits from the dependency of the threshold voltage of a MOS transistor to its source-to-bulk voltage. The threshold voltage of a PMOS transistor is related to the voltage of its body by the following equation:

$$V_{TH} = V_{TH0} - \gamma\left(\sqrt{|-2\varphi_F|} - \sqrt{|-2\varphi_F + V_{BS}|}\right) \quad (1)$$

Where $2\varphi_F$ is the surface potential, V_{BS} is body-to-source voltage and V_{TH0} is the threshold voltage for zero body-to-source voltage.

From Eq. (1), if the voltage of the body of a PMOS transistor is connected to a voltage lower than the voltage of its source, the threshold voltage of the transistor will be reduced. Conversely, if the bulk-to-source voltage becomes positive, the threshold voltage will be increased. Using this effect, one can increase the threshold voltage when a transistor is off to save power.

In addition, the threshold voltage can be decreased to improve drive capability while a transistor is on.

In order to take advantage of the superior effects of body biasing technique, some structures have been proposed to use the same idea in bulk CMOS technology [3,13-15]. Dynamic threshold-voltage MOSFET (DTMOS) [3] is implemented by connecting the gate of a MOSFET to its substrate to achieve the desired performance, which was shown to outperform the conventional CMOS logic in the sub-threshold region. In [14] a new structure is introduced which uses an auxiliary NMOS transistor to connect the gate of a PMOS transistor to its body. In this way the switching activity of the body of PMOS transistor and hence delay and power consumption will be reduced. The authors in [15] have been proposed a new scheme in which the well of a PMOS transistor is connected to the output of the gate instead of using each gate's input as in [3]. Using this approach, the switching activity of the body of PMOS transistor is decreased and as a result, more power will be saved.

Here, a new dynamic body biasing structures has been proposed to improve performances of digital circuits. The proposed structure takes advantage from switched capacitor structures as well as DTMOS scheme and successfully reduces the threshold voltage of a PMOS transistor while it is in an on-state. The proposed SC-DTPMOS circuit is suitable for the circuits which the probability of the output voltage switching is high.

To evaluate the proposed technique and compare the results with others, a simple NOT gate has been designed and simulated with Cadence Spectre using TSMC 0.180µm CMOS technology.

The rest of this paper is organized as follows. A review of previous works is given in Section 2. In Section 3 the proposed technique is introduced. Post layout simulation results and comparison with previous works are shown in Section 4. Eventually, Section 5 concludes this work.

2 Review

In this section, some dynamic body biasing structures, including DTPMOS, NCB-DTPMOS and Gate-Level Body Biasing are briefly described.

2.1 DTPMOS Technique

As shown in Fig. 1, this structure relies on the connection between the gate and the well of PMOS transistors to reduce the threshold voltage during the on-state and maintain a high threshold voltage in the off-state. The low threshold voltage in the on-state leads to a significant reduction in delay at a low voltage supply [2].

Compared to conventional CMOS structure where the body of PMOS transistor connects to its source, DTPMOS results in a higher PMOS current drive and consequently a higher speed operation at a very low voltage. This is mainly due to a larger inversion charge and a lower effective normal field in the channel. The lower effective normal field leads to higher mobility and consequently higher current drive [3].

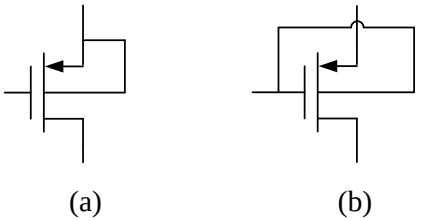

Fig. 1 a) Conventional structure and b) DTPMOS scheme [2].

2.2 DTPMOS Technique

Fig. 2(a) shows the conventional DTPMOS operation, where the gate of each PMOS transistor is connected to its well to achieve the desired performance. Fig. 2(b) shows the NMOS-Controlled DTPMOS (NCB-DTPMOS) operation.

In this scheme, the gate of the PMOS transistor is not connected directly to its well; instead an NMOS transistor is employed. The gate of the NMOS is tied to the PMOS source, while the source and drain of the NMOS are connected to the PMOS gate and well. Note that the common NMOS substrate is connected to common ground all over the circuit. The NMOS acts as a switch between the PMOS gate and well. If the PMOS network is not forming a continuous path between the supply and this PMOS transistor, the output node will not be brought high; this note is indeed applicable to any PMOS transistor in the PMOS network. In this case; and if the input at the gate of the PMOS transistor is high, the potential of the PMOS transistor well will not increase and the threshold voltage of the PMOS transistor will not be reduced. In other words, the leakage current will not increase and energy will be saved. This means that the NMOS transistor reduces the switching rate of the PMOS's n-well and as a result more energy is saved. In the conventional DTPMOS scheme; Fig. 2(a), the n-well of the PMOS transistor will keep switching conditionally; depending on the input on the gate, although it is sometimes will not affect the logic level at the output and it is only a waste of energy [14].

This scheme is applied to all PMOS transistors in the PMOS network. The only PMOS transistor that will be excluded from this scheme is the one whose source is directly connected to the voltage supply [14]. Therefore, if the PMOS network in a circuit includes only one series transistor (as in NAND), this structure does not outperform DTPMOS. In this case, DTPMOS shows superior performance in terms of area and speed since in NCB-DTPMOS scheme a transistor is added to the circuit which increases the area and the overall input capacitance.

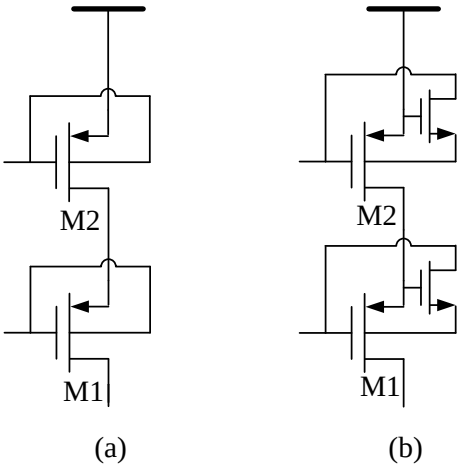

Fig. 2 a) DTPMOS technique [2] and b) NCB-DTPMOS technique [14].

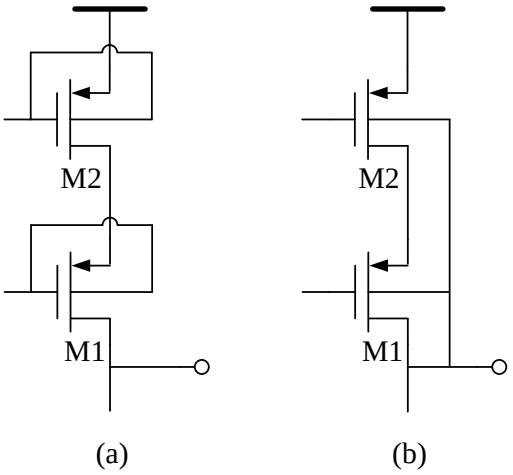

Fig. 3 a) DTPMOS structure [2] and b) Gate Level Body Biasing scheme [15].

2.3 Gate-Level Body Biasing Technique

As shown in Fig. 3, this structure relies on the connection between the well of PMOS transistors and the gate's output instead of its input as in DTPMOS. In the conventional DTPMOS technique, PMOS transistors' bodies are biased individually by their respective inputs so that each transistor may have a high or low sub-threshold leakage current, independent of the gate's status. Consequently, a gate may experience a high current even though it may not be needed due to individual PMOS transistors' states. Moreover, such signal currents introduce glitches in the output signal waveform which further increase circuit's power consumption. In the proposed technique, a biasing signal is used which is generated on the gate level by the gate itself so the need of a dedicated circuit to generate the bias signal is eliminated and the used biasing signal will not vary from a transistor to a transistor within the same gate. The output of the gate will be used to bias all the PMOS transistors in the gate [15].

The proposed circuit will work best if the circuit has a large activity factor since this way it will continuously save more power than DTPMOS scheme. While if it had a low activity factor then it would still outperform the DTPMOS in terms of speed but it will suffer from some high currents and hence its power consumption will increase during circuit idle durations [15].

3 Proposed Technique

In the previous section, some body biasing techniques were reviewed. DTPMOS suffers from high body switching factor and power consumption. The problem of NCB-DTPMOS is its weak performance while the PMOS network has only one series transistor. The drawback of Gate-level body biasing is its power dissipation. Here, a new dynamic body biasing structure is introduced and illustrated in detail. This scheme outperforms the previous works in terms of propagation delay and power consumption.

Equation (1) showed the dependency of the threshold voltage to the bulk-to-source voltage of a PMOS transistor. Considering Eq. (1), higher bulk-to-source voltage results in a higher threshold voltage. Conversely, lower bulk-to-source voltage causes the threshold voltage to become lower. As a result, if a negative bulk voltage can be generated while the transistor is in the on-state, the threshold voltage can become as low as possible and the drive capability of the circuit will be higher. This results in a faster circuit and the propagation delay will be lower.

Fig. 4(a) shows the DTPMOS structure. The main idea of the proposed structure is depicted in Fig. 4(b). The circuit looks like DTPMOS structure; however, the difference is that a voltage source is connected between the gate and the bulk. In DTPMOS structure, the voltage of the body and the gate are the same. So, when the PMOS transistor is on, the gate voltage is zero, the body potential is zero, too and the body-to-source voltage will be $-V_{DD}$. However, in the proposed structure the body potential (V_B) is as follows:

$$V_B = V_G - V_0 \tag{2}$$

Where V_G is the gate voltage and V_0 is the value of the voltage source which is placed between the gate and the body. When the PMOS transistor is on, the gate potential is zero. Using Eq. (2), the body voltage will be $-V_0$. As a result, the body-to-source voltage become $-V_0$-V_{DD} which is less than DTPMOS structure. So, the threshold voltage becomes less in comparison with DTPMOS structure when the transistor is on. This results in a higher drive current and the propagation delay will be lower.

The main obstacle of the proposed idea is the implementation of a floating voltage source. This is accomplished using a capacitor (C) as shown in Fig. 5(a). Also, a switch (S) is placed to charge the

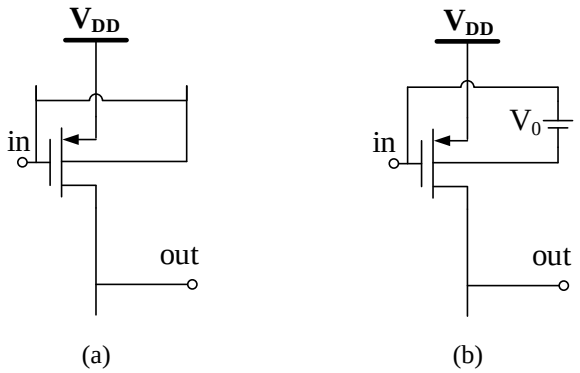

Fig. 4 a) DTPMOS structure and b) The proposed idea.

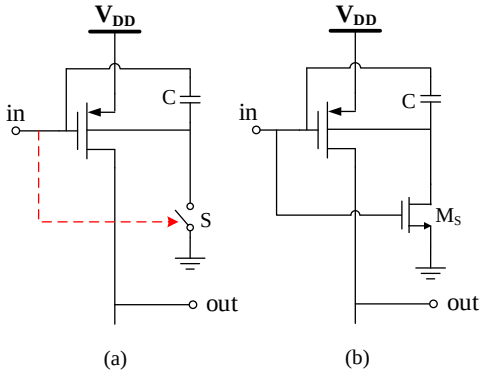

Fig. 5 a) Implementation of floating voltage source and b) implementation of switch S.

capacitor to a desired value. When the input is in a high-state (V_{in}=V_{DD}), the PMOS transistor is off. In this case, switch S becomes on and connects the body to the ground. So, the capacitor will be charged to V_{DD}. When the input goes to a low-state (V_{in}=0), switch S turns off. According to Eq. (2), the body potential becomes – V_{DD} and the threshold voltage becomes lower. It should be mentioned that the capacitor does not provide a constant negative voltage (– V_{DD}) for the biasing of the body of the pmos transistor while the pmos transistor is on (like what is actually a voltage source do). The capacitor improves the propagation delay times of the circuit by changing the body potential at the transitions from low-to-high or high-to-low states.

An NMOS transistor (M_S) is used to implement switch S. The overall proposed Switched-Capacitor DTPMOS (SC-DTPMOS) structure is demonstrated in Fig. 5(b).

The SC-DTPMOS structure suffers from some drawbacks. When the PMOS transistor is off, the input must be in a high state. As a result, switch S is on and the body potential becomes zero. In DTPMOS scheme, the body potential is V_{DD} when the transistor is off. This leads to a higher standby power dissipation in the proposed SC-DTPMOS structure compared to DTPMOS technique. However, due to higher drive current, the transition time of the output voltage is less than DTPMOS structure. As a result, the short-circuit current in the proposed structure decreases. This causes the dynamic power consumption to be decreased. The proposed structure shows better performance if the switching factor of the gate is high. In this case, dynamic power dominates standby power and results in less power consumption in the proposed structure. Conversely, for the circuits with low switching factor, the DTPMOS structure outperforms SC-DTPMOS scheme. Finally, the SC-DTPMOS structure is proposed for the applications where the propagation delay is a major concern and the switching factor of the circuit is high.

4 Simulation Results

To evaluate the effectiveness of the proposed structure, a simple NOT gate is designed using the proposed SC-DTPMOS structure as shown in Fig. 6(a). Circuit parameters are given in Table 1. V_{DD} is assumed to be 0.2V in order to evaluate the structures in low-voltage and sub-threshold applications. The size of the auxiliary transistor (M_S) is chosen to be minimum size. Also the value of capacitor (C) is chosen to be as small as possible. The reason is that as the proposed structure has an extra capacitor and an extra transistor in comparison with DTPMOS technique, the area of the proposed structure is bigger than DTPMOS scheme. In order to minimize the area, these two components should be minimum size. Furthermore, the capacitor (C) changes the input capacitance seen at the gate of the PMOS transistor. The value of C is chosen to be minimum in order to minimize the input capacitance of the gate. This capacitor is implemented by NMOSCAP technology to save more area. It should be mentioned that the minimal size NMOS transistor acting as a switch is prone to the transient current of capacitor switching and may be damaged. Whenever it is a concern, its size should be chosen bigger than minimum size.

To evaluate the proposed structure and compare the results with other body biasing structures, similar NOT gates are designed using conventional, NCB-DTPMOS, Gate-Level body biasing and DTPMOS techniques which are shown in Fig. 6(b)-6(e), respectively. The circuit parameters for these structures are according to Table 1. In order to have a fair comparison, RC parasitics of the circuit layout should be taken into account. Hence, circuit layouts for the proposed structure as well as other schemes have been carefully designd using Virtuso layout editor. Post layout simulations have been done with Candence Assura using TSMC 180nm CMOS technology.

A 200 kHz periodic pulse is applied to the circuits. Post layout simulation result for the output voltage of the mentioned structures are shown in Fig. 7. It can be seen that SC-DTPMOS structure outperforms other scheme in terms of propagation delay and speed. Both high-to-low and low-to-high propagation delay times are improved in the proposed SC-DTPMOS scheme.

Table 1 Circuit parameters of the proposed SC-DTPMOS structure.

Parameter	Symbol	Value
Supply voltage	V_{DD}	0.2V
Size of M_n	$(W/L)_{Mn}$	1um/180nm
Size of M_p	$(W/L)_{Mp}$	2um/180nm
Size of M_S	$(W/L)_{Ms}$	1um/180nm
Capacitor	C	1.5 fF

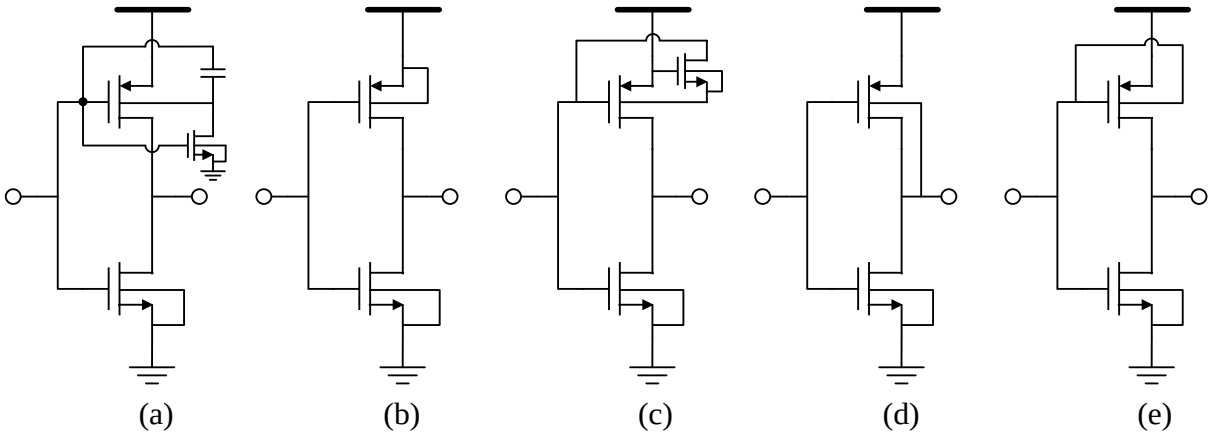

Fig. 6 A simple NOT gate using a) proposed SC-DTPMOS structure, b) conventional structure (no dynamic threshold design), c) NCB-DTPMOS structure, d) Gate-level body biasing structure and e) DTPMOS structure.

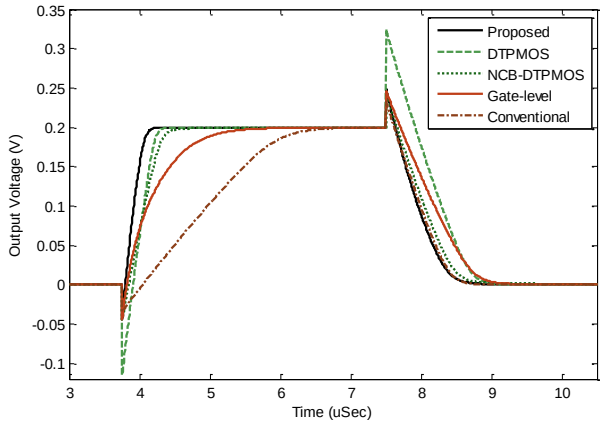

Fig. 7 Simulation results of the output voltage of a NOT gate using the proposed SC-DTPMOS technique in comparison with other structures.

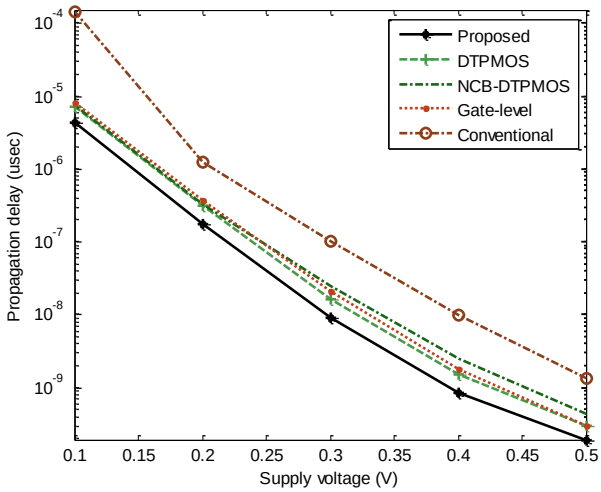

Fig. 8 Post layout simulation results for low-to-high propagation delay time of a NOT gate using the proposed SC-DTPMOS technique in comparison with other structures.

To ensure circuit functionality under different supply voltages, all of the schemes are simulated for V_{DD} spanning from 0.1V to 0.5V. Simulation results for the propagation delay, power consumption and power-delay product are depicted in Fig.8-10, respectively. As shown in Fig. 8, the proposed SC-DTPMOS outperforms all of the previous techniques in propagation delay. This is mainly due to lower threshold voltage and higher drive current during on-state. From Fig. 9, it is seen that for low supply voltages, the proposed circuit outperforms others. When the supply voltage increases, the transistor gets out of sub-threshold region. Hence, conventional structure (no dynamic threshold technique) outperforms others in power consumption since its PMOS transistor has the highest threshold voltage among other schemes. Fig. 10 clearly shows the superiority of the proposed structure over other dynamic threshold design techniques at low supply voltages. The power-delay product for the proposed SC-DTPMOS structure has the lowest value compared to other common structures.

Table 2 summarizes post layout simulation results for the proposed technique versus other structures in some process corners and different temperatures. As is seen from this table, propagation delays as well as power consumption have been improved. The proposed structure has the least propagation delay times (both

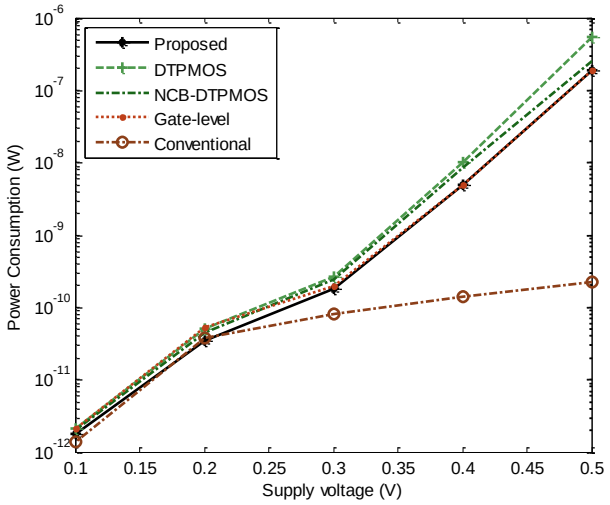

Fig. 9 Post layout simulation results for power consumption of a NOT gate using the proposed SC-DTPMOS technique in comparison with other structures.

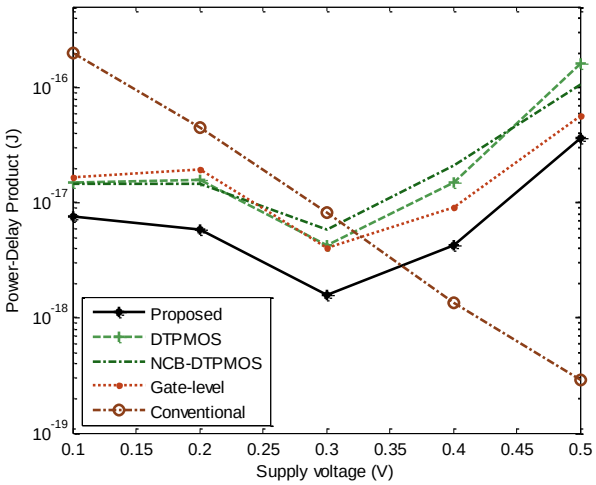

Fig. 10 Post layout simulation results for power-delay products of a NOT gate using the proposed SC-DTPMOS technique in comparison with other structures.

Table 2 Post layout simulation results for the proposed SC-DTPMOS structure compared to other structures.

Parameter	Corner @Temp	Conventional	NCB-DTPMOS	Gate-Level	DTPMOS	SC-DTPMOS
Technology-V_{DD}	TSMC 0.18µm CMOS technology- 0.2V					
Average power consumption (W)	TT@27°	37×10^{-12}	46×10^{-12}	52×10^{-12}	53×10^{-12}	39×10^{-12}
	FF@85°	1.9×10^{-9}	4×10^{-9}	3.5×10^{-9}	4.7×10^{-9}	3.5×10^{-9}
	SS@-40°	1.1×10^{-13}	1.6×10^{-13}	1.4×10^{-13}	1.6×10^{-13}	1.5×10^{-13}
Low-to-high propagation delay (Sec)	TT@27°	1200×10^{-9}	320×10^{-9}	370×10^{-9}	310×10^{-9}	170×10^{-9}
	FF@85°	26×10^{-9}	10×10^{-9}	10×10^{-9}	9.9×10^{-9}	6×10^{-9}
	SS@-40°	513×10^{-6}	106×10^{-6}	116×10^{-6}	85×10^{-6}	45×10^{-6}
High-to-low propagation delay (Sec)	TT@27°	490×10^{-9}	550×10^{-9}	690×10^{-9}	790×10^{-9}	460×10^{-9}
	FF@85°	8.2×10^{-9}	8.8×10^{-9}	11.3×10^{-9}	12.9×10^{-9}	7×10^{-9}
	SS@-40°	352×10^{-6}	377×10^{-6}	509×10^{-6}	567×10^{-6}	303×10^{-6}
Power-Delay Product (J)	TT@27°	4.4×10^{-17}	1.4×10^{-17}	1.9×10^{-17}	1.6×10^{-17}	0.67×10^{-17}
	FF@85°	4.9×10^{-17}	4×10^{-17}	3.5×10^{-17}	4.7×10^{-17}	2.1×10^{-17}
	SS@-40°	5.6×10^{-17}	1.7×10^{-17}	1.6×10^{-17}	1.4×10^{-17}	0.7×10^{-17}
Area (µm×µm)	-	3.4×7.1	5.0×7.1	3.4×7.1	3.4×7.1	5.2×7.1

high-to-low and low-to-high) and power-delay product among the well-known structures in all of the process corners and temperatures. It should be noted that the relative changes in the delays due to the variations in temperature and process corner in the proposed structure is less than all other structures. Table 2 clearly shows the effectiveness of the proposed SC-DTPMOS technique at low voltage, low power and high speed applications.

To evaluate the sensitivity of the structure due to changes in the absolute value of the parameters in the circuit (including W and L of the transistors), Monte-Carlo simulations were performed on the circuit. A Gaussian distribution was made in all of the parameters of the circuit with a 3-sigma of 1% relative error. The resulting histogram of the high-to-low propagation delay is shown in Fig. 11 for a number of 100 runs. As can be seen from this figure, the output changes due to the error has a 1-sigam of 0.1 nsec and a relative error of 0.1% which shows the low-sensitivity of the circuit to the variations of W and L of the transistors.

The circuit layout for the proposed SC-DTPMOS structure is shown in Fig. 12. The resulting die size is 5.2µm×7.1µm. It should be noted that as the proposed design has two extra elements, the occupied area has been increased in comparison with some other structures. In order to save more area, the capacitor has been designed using NMOSCAP technology instead of MIMCAP technology since it has more capacitance density. The bulk of the NMOSCAP has been connected to the ground.

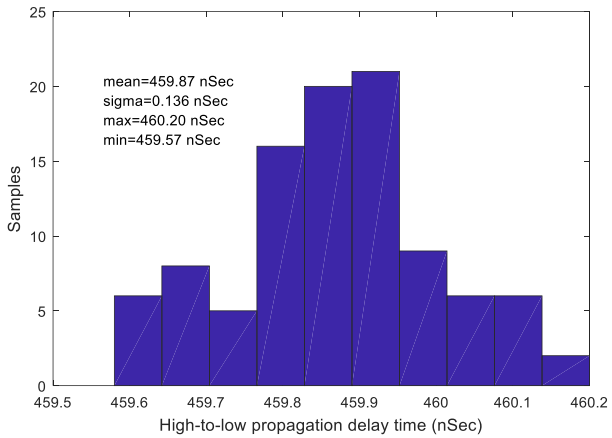

Fig. 11 The histogram of the propagation delay time of the proposed structure.

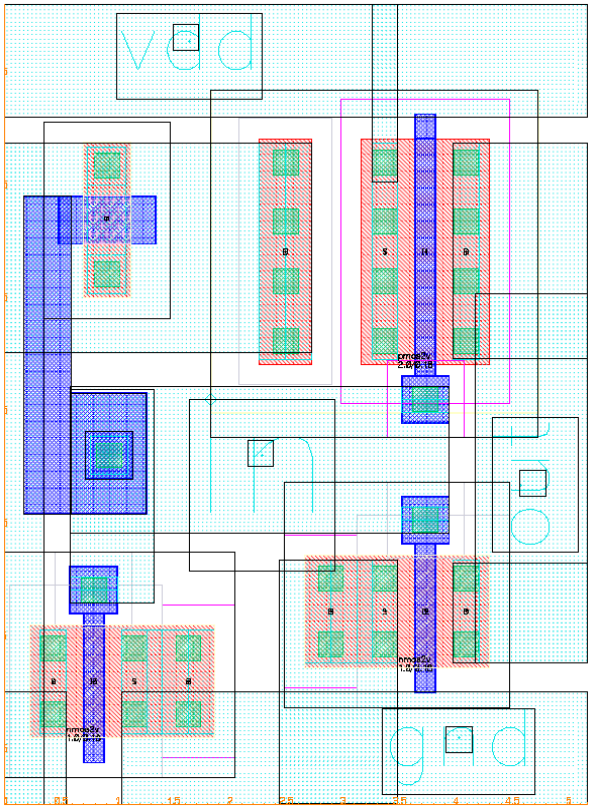

Fig. 12 Circuit layout design for the proposed SC-DTPMOS structure.

5 Conclusion

In this work, a new dynamic body biasing technique was proposed which outperforms previous dynamic threshold structures in terms of power consumption and propagation delay. In the proposed technique, a capacitor is charged and placed between the gate and the body of PMOS transistor to cause the threshold voltage to become lower. The new SC-DTPMOS technique is much suitable for low-voltage high speed application with high switching factor. Post layout simulation results verified the effectiveness of the proposed techniques.

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