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A New Solution to Analysis of CMOS Ring Oscillators

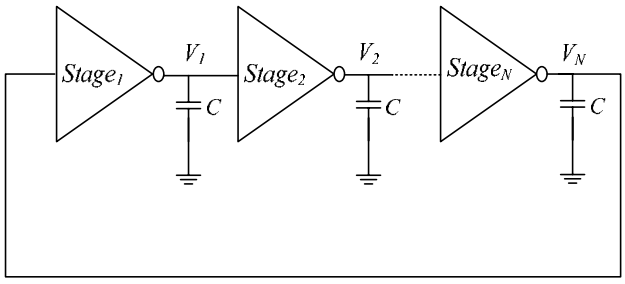
P. M. Farahabadi*, H. Miar-Naimi** and A. Ebrahimzadeh**

Abstract: New equations are proposed for frequency and amplitude of a ring oscillator. The method is general enough to be used for all types of delay stages. Using exact large-signal circuit analysis, closed form equations for estimating the frequency and amplitude of a high frequency ring oscillator are derived as an example. The method takes into account the effect of various parasitic capacitors to have better accuracy. Based on the loop gain of the ring, the transistors may only be in saturation or experience cutoff and triode regions. The analysis considers all of the above mentioned scenarios respectively and gives distinct equations. The validity of the resulted equations is verified through simulations using TSMC 0.18 µm CMOS process. Simulation results show the better accuracy of the proposed method compared with others.

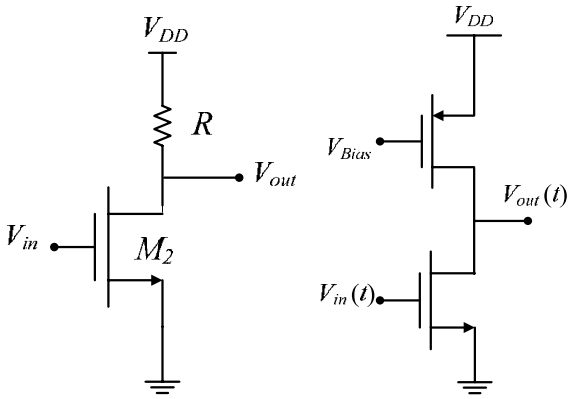
Keywords: CMOS voltage-controlled oscillators, high-speed integrated circuits, trigonometric equations, large-signal analysis.

1 Introduction

Voltage controlled oscillators (VCO) are most commonly used building blocks in communication applications like phase locked loops (PLL) and clock and data recovery circuits [1]-[5]. Due to lower power consumption, large tuning range and lower die space area, the ring oscillator (RO) is investigated in these applications. RO circuits must satisfy some specifications such as area, power, speed and phase noise, posing challenges to circuit and system designers. Also the correct amplitude and low phase noise are two criteria to obtain a suitable performance for VCO in a circuit. Obtaining the transfer function or any knowledge about the amplitude and frequency of the oscillator is necessary to overcome these tradeoffs [6]-[12]. Some simple mathematical equations have been presented for frequency of oscillation of the RO, commonly using small signal analysis [13]-[16]. All of these equations assume the RO as a linear small-signal circuit model and derive the oscillation frequency by adding the parasitic and secondary effects to the simple ideal frequency equation. However, because of the inherent nonlinear behavior of the RO, the accuracy of the equations is limited only for these assumptions.



(a)



(b) (c)

Fig 1. (a) N-stage single-ended RO. (b) Delay stage, with resistor load (c) Transistor Level load for delay stage.

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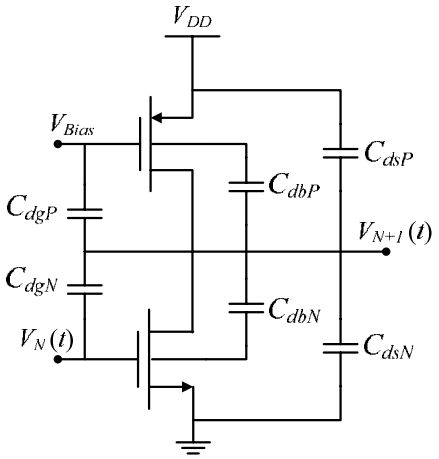

Fig. 2. Parasitic capacitors in a delay stage

Moreover, all of these equations cannot represent the amplitude of the output waveform of the RO exactly.

This paper presents a novel method to derive equations for both amplitude and oscillation frequency of the RO. In this method, the parameterized waveforms of the outputs are estimated and closed-form equations for unknown parameters are derived using differential equations. The rest of the paper is as follows: SECTION II introduces mathematical principle used to compute the frequency of oscillation and a brief review of the existing methods. Section III describes the proposed methodology to derive the equations for the amplitude and the frequency of oscillation. A new technique based on large signal analysis is presented to derive exact equations for the output frequency and amplitude in this section. Simulation results are compared with the values estimated by equations to show the validity of the method in section IV. Finally, section V gives the conclusions.

2 Literature Review on Frequency Equations

A ring oscillator consists of a number of gain stages in a unity gain feedback loop. To achieve oscillation, the circuit must satisfy two Barkhausen's criteria that mean the total phase shift and the gain of the feedback loop must be 2π and one respectively. An N-stage ring oscillator is shown in Fig. 1. Small signal analysis and the open loop transfer function for this circuit is written as below:

$$H(s)=[-g_m(R\,\|\,\frac{1}{Cs})]^N=(-1)^N\frac{(g_mR)^N}{(1+\frac{s}{\omega_0})^N} \qquad (1)$$

$$\omega_0=1/RC \qquad (2)$$

Because of the unity feedback gain, the open loop transfer function is the same as the loop transfer function. Total phase shift around the loop is written as (3) and for ω = 0 it is written like equation (4) that means the oscillator locks at DC level for even N, so the odd number of stages is necessary for oscillation in single-ended ring oscillators [4].

$$\phi(\omega)=-\pi-N\tan^{-1}(\omega/\omega_0) \qquad (3)$$

$$\phi(\omega)\big|_{\omega=0}=\begin{cases}2\pi & N=2n\\ \pi & N=2n-1\end{cases} \qquad (4)$$

Total phase shift 2π for oscillation is provided at ω_{osc} for odd N by (5). Equation (5) is most commonly used for the oscillation frequency of an RO in analog microelectronic design text books [12].

$$\omega_{osc}=\omega_0\tan(\pi/N) \qquad (5)$$

With simple simulations, one can find that this analysis is incorrect if the amplitude of outputs does not meet the small signal conditions. Also, small signal analysis does not give any idea about the amplitude of oscillation.

Considering RO as a chain of delay stages is another method which is also commonly used by designers. Assuming a delay of td for each stage, total phase shift 2π must be provided in the period of 2Ntd. Therefore, the oscillation frequency is as (6):

$$f=\frac{1}{2N\cdot t_d} \qquad (6)$$

A method to improve the accuracy of previous equation is proposed in [13]. The oscillation frequency in this method is given by (7). The set of parameters that have been used in this method is listed in Table 1.

Table 1. Differential Delay Stage parameters

N	Number of delay stages in the RO
t_d	Delay time of each stage in the RO
R_L	Equivalent resistance of the PMOS load of each delay stage
C_L	Load capacitance of the delay stage without parasitic elements
I_{SS}	Tail current used in the differential delay stage
V_{SW}	Peak to peak amplitude of the output voltage waveform

The time delay per stage is defined as the total change in differential output of the midpoint of the transition. This method only considers differential RO and cannot be extended to single ended structures.

Reference [14] models each delay stage as a simple RC circuit. Using (8), with V_{out}*(initial)* equals to V_{DD}

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and $V_{out}(final)$ equals to V_{DD}-V_{SW}, the delay per stage equals to R_LC_Lln2. Hence the frequency is given by (9).

$$f = \frac{1}{2N \cdot t_d} \tag{7}$$

$$V_{out}(t) = V_{out}(final) + [V_{out}(initial) - V_{out}(final)] \times \exp(-\frac{t}{RC}) \tag{8}$$

$$f = \frac{1}{2NR_LC_L \cdot \ln 2} \tag{9}$$

The method proposed in [15] assumes a ramp input to find delay to time constant to obtain (10).

$$f = \frac{1}{2N(0.8)R \cdot (C_{DBn} + C_{DBp} + C_{GDn} + C_{GDp} + C_L)} \tag{10}$$

This equation can be adapted for single-ended RO considered in this paper. The transistor parasitic elements that used in this equation are gate-drain, gate-bulk and drain-bulk capacitors. Parasitic capacitors in a delay stage are shown in Fig. 2.

Another method to derive an equation for the oscillation frequency of only differential ring oscillator is proposed in [16]. The final equation for obtaining the frequency is as (11) which is similar to (7), but a large signal analysis is used for calculating the value of capacitors accurately.

$$f = \frac{I_{SS}}{2NV_{SW} \times \left[\begin{array}{l} C_L + C_{gdp} + \frac{C_{jn}Ad_n}{(1+\frac{V_{DD}}{pb_n})^{mjn}} + \\ \frac{C_{jswn}Pd_n}{(1+\frac{V_{DD}}{pb_{swn}})^{mjswn}} + (1+\cos(\frac{\pi}{N}))W_nC_{gdon} + \\ C_{jp}Ad_p + C_{jswp}Pd_n \end{array}\right]} \tag{11}$$

The parameters used in this equation are exact HSPICE parameters of transistors. This method is more accurate than other presented methods but it cannot predict the amplitude or frequency when the transistors change the operation region during oscillation.

3 The Proposed Method

3.1 General Procedure

The method proposed in this paper is based on the exact differential equations governing on the RO. These equations are simply obtained using circuit analysis methods. The proposed method presents exact equations to find the frequency, amplitude and DC level of the output waveform of an RO while the last methods only give approximate expressions for "t_d" or frequency. At first it is assumed that all transistors are all in the saturation region. This is a common assumption in all the presented methods for representing the frequency of an RO. The proposed method is general enough to be applied on any structures but in this paper it is focused on an N-stage single-ended ring oscillator with common source stages. More complete equations for the other types of ring oscillator can be developed with the same analysis procedure. Assuming saturation for transistors, the differential equation of the circuit is obtained by a Kirchhoff's Current Law (KCL) at each drain node (Fig. 1(a)). Fig. 3 shows one common source stage of an RO with a resistor load and the currents used in mentioned KCL equation.

Equations (12) and (13) represent a nonlinear N-dimensional differential system. The effect of parasitic capacitors that are shown in Fig. 2 is written as (14) for more accurate estimation. Pure sinusoid waveform as (15) for the outputs is the key simplifying assumption that leads to straightforward analysis along with accurate results. Assuming this, the analysis is devoted to find amplitude, A, DC level, B, and frequency, ω. Although the output of an RO will not be purely sinusoidal, the frequency representation of a practical RO output shows that it is a reasonable assumption [2], [8].

$$\begin{cases} node_1 : \frac{V_1 - V_{DD}}{R} + C\frac{dV_1}{dt} + K(V_N - V_{th})^2 = 0 \\ node_2 : \frac{V_2 - V_{DD}}{R} + C\frac{dV_2}{dt} + K(V_1 - V_{th})^2 = 0 \\ \quad \text{M} \\ node_N : \frac{V_N - V_{DD}}{R} + C\frac{dV_N}{dt} + K(V_{N-1} - V_{th})^2 = 0 \end{cases} \tag{12}$$

$$K = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L}) \tag{13}$$

$$C = C_L + C_{gdp} + C_{gdn} + C_{dbp} + C_{dbn} \tag{14}$$

$$V_o(t) = B + A\cos\omega t \tag{15}$$

The phase relation among the outputs of an N-stage RO is shown in Fig. 4. Assuming equation for $V_2(t)$ as (15), the output of the first stage can be written as (16) considering the phase relations in Fig. 4.

$$\begin{aligned} V_1(t) &= V_2(t + (\frac{T}{2} - \frac{T}{2N})) \\ &= B + A\cos(\omega t + \frac{(N-1)\pi}{N}) \end{aligned} \tag{16}$$

Using a bit mathematical operations, equation (12), (15) and (16) can be combined and reduced to (17); the basic trigonometric equation of the proposed method.

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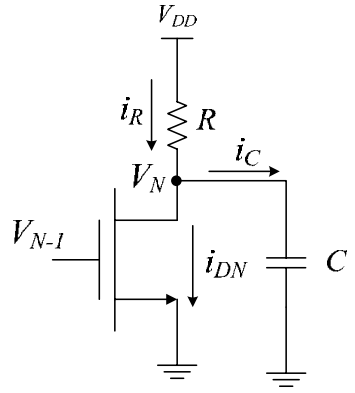

Fig. 3. Definition of currents for KCL in a delay stage.

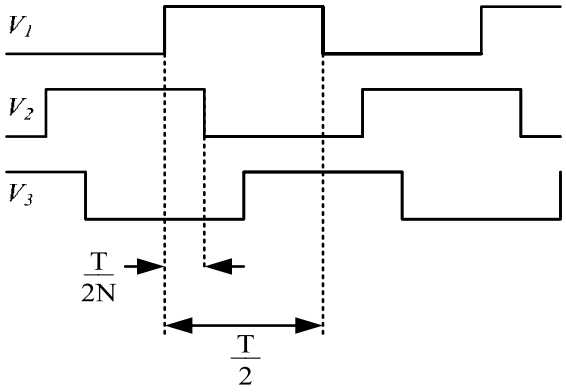

Fig. 4. Phase relation between waveforms.

$$\frac{B+A\cos\omega t-V_{DD}}{R}-\omega CA\sin\omega t+ K(B+A\cos(\omega t+\frac{(N-1)\pi}{N})-V_{th})^2=0 \quad (17)$$

Equation (17) holds for every time especially for three special times mentioned in (18) that leave three beneficial equations in (19).

$$\begin{aligned} &I)\ \sin\omega t=-1\ ,\ \cos\omega t=0\\ &II)\ \sin\omega t=0\ \ ,\ \cos\omega t=1\\ &III)\ \sin\omega t=0\ \ ,\ \cos\omega t=-1 \end{aligned} \quad (18)$$

$$\begin{cases} I)\ \dfrac{B-V_{DD}}{R}+\omega CA+K(B-A\sin\dfrac{\pi}{N}-V_{th})^2=0\\ II)\ \dfrac{B+A-V_{DD}}{R}+K(B-A\cos\dfrac{\pi}{N}-V_{th})^2=0\\ III)\ \dfrac{B-A-V_{DD}}{R}+K(B+A\cos\dfrac{\pi}{N}-V_{th})^2=0 \end{cases} \quad (19)$$

With simple calculations, the unknowns of (19) can be obtained. At the first step, the DC level of the output is obtained in term of circuit parameters as (20) explicitly. The amplitude is obtained in term of B and other parameters as (21). Knowing the B and A, the unknown frequency of oscillation is written as (22).

$$B=V_{th}+\frac{1}{2RK\cos\frac{\pi}{N}} \quad (20)$$

$$A=\sqrt{\frac{\frac{V_{DD}-B}{R}-K(B-V_{th})^2}{K\cos^2(\pi/N)}} \quad (21)$$

$$f=\frac{\frac{B-V_{DD}}{R}+K(B-A\sin(\pi/N)-V_{th})^2}{2\pi CA} \quad (22)$$

These closed-form equations can represent the frequency, amplitude and DC level of an N-stage single-ended ring oscillator just knowing the circuit parameters. Equation (21) shows that the amplitude is just proportional to the circuit parameters except capacitors. Also the frequency is inversely proportional to the C and R in (22). Note that the assumptions here are the output waveform is like a sinusoid and the transistors are all in saturation region. To verify the analysis above the following two conditions should be met.

I. The transistors should not meet triode region that means $V_{n-1}(t)<V_n(t)-V_{th}$.

II. The transistors should not meet cutoff region that means $B-A\geq V_{th}$.

Defining the voltage across the Gate-Drain junction in first delay stage as (23), if the first condition is satisfied, the transistors remain in saturation region. Using the maximum points as an additional condition, the expression (23) is reduced to (25). So expression (25) must be satisfied for using the proposed equations. Otherwise, transistors experience the cutoff or triode regions, so a more general analysis should be performed.

$$\begin{aligned} V_1(t)-V_2(t)&=A[\cos(\omega t+\frac{(N-1)\pi}{N})-\cos\omega t]\\ &=-2A\sin\frac{\omega t+\frac{(1-1)\pi}{N}+\omega t}{2}\sin\frac{\omega t+\frac{(N-1)\pi}{N}-\omega t}{2}\\ &=-2A\sin(\omega t+\frac{(N-1)\pi}{2N})\sin(\frac{(N-1)\pi}{2N}) \end{aligned} \quad (23)$$

$$\max\{V_1(t)-V_2(t)\}=2A\sin(\frac{(N-1)\pi}{2N})=2A\cos\frac{\pi}{2N} \quad (24)$$

$$2A\cos(\pi/N)<V_{th} \quad (25)$$

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3.2 Analytical Equations for The Case that Transistors Enter Triode region

Closed-form equations for the cases that transistors meet the triode or cutoff region can be easily obtained with the same analysis. Fig. 5 illustrates the sample output voltages when the transistors meet both triode and saturation region during an oscillation period. This plot gives the evidence that the output voltage of an RO can be assumed as a sinusoid waveform if transistors meet the triode region yet. All the published methods for estimating the frequency of an RO have not represented the acceptable accuracy for the cases that the operating region changes while this paper presents closed-form equations for both amplitude and frequency of the transistors meeting all operating regions.

The analysis proposed here is again based on the KCL equations at the output of each delay stage. These equations can be written as (26).

$$\begin{cases} \dfrac{V_1 - V_{DD}}{R} + C\dfrac{dV_1}{dt} + i_{D_1}(t) = 0 \\ \dfrac{V_2 - V_{DD}}{R} + C\dfrac{dV_2}{dt} + i_{D_2}(t) = 0 \\ \text{M} \\ \dfrac{V_N - V_{DD}}{R} + C\dfrac{dV_N}{dt} + i_{D_N}(t) = 0 \end{cases} \tag{26}$$

where $i_{Dk}(t)$ is the Drain current of transistor number K. The output voltage is assumed sinusoid waveform as (15) to make the problem traceable. For instance, the output of the second stage is considered as (15), so the first stage output is written as (16). The unknowns here are the frequency of oscillation, the output voltage amplitude and DC level of output that are f, A and B respectively. Considering the quadratic law between Drain current and the Gate-Source voltage for the second transistor, M_2, the Drain current is written as (27) for second stage. As shown in Fig. 5, the outputs are sinusoid-like waveform yet, but the frequency of these outputs cannot be obtained from any of presented expressions. Also, there is no analysis to estimate the amplitude of the output waveform. In this section, each transistor may meet the both triode and saturation regions during one period of oscillation, so the equation for Drain current of second stage is written as (27) that is shown in bottom of this page. Substituting (26)-(27), the N-dimensional equations are obtained. Solving the obtained equations using analytical rules is difficult, so the critical points are considered to make the problem traceable. Choosing these critical points is based on having knowledge about the times when transistors are exactly in the triode or saturation region. For example, for the times $\omega_t = 0$, the output $V_2(t)$ is at maximum as it is shown in Fig. 5, so the transistor M_2 is exactly in saturation region. The equations resulted from some critical points is written as (28)—(30) which are at the bottom of the next page. There are just two unknowns in both algebraic equations (28) and (29). Hence, the DC level, B, and the amplitude, A, are obtained using a simple numerical solution method. Using the obtained amplitude and DC level from (28) and (29) in (30), a closed-form equation for frequency of oscillation is written as (31). This expression is shown at the bottom of the next page.

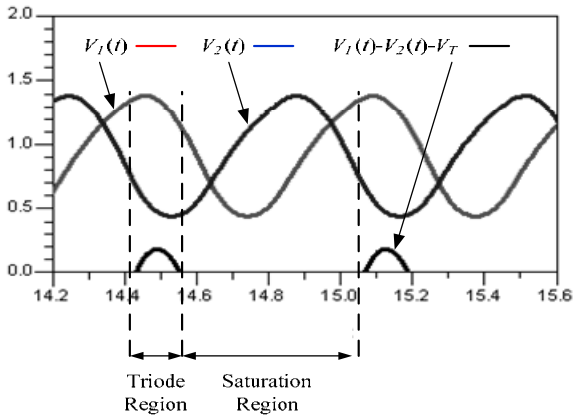

Fig. 5. Sample output voltages for the case that transistors meet both triode and saturation regions during oscillation.

$$i_{D2}(t) = \begin{cases} \dfrac{B + A\cos\omega t - V_{DD}}{R} - \omega CA\sin\omega t \\ +2K\{[B + A\cos(\omega t + \dfrac{N-1}{N}\pi) - V_{th}](B + A\cos\omega t) \\ -\dfrac{(B + A\cos\omega t)^2}{2}\} = 0 \qquad \text{for } V_1(t) > V_2(t) + V_{th} \\ \dfrac{B + A\cos\omega t - V_{DD}}{R} - \omega CA\sin\omega t \\ +K(B + A\cos(\omega t + \dfrac{N-1}{N}\pi) - V_{th})^2 = 0 \\ \qquad \text{for } V_1(t) < V_2(t) + V_{th} \end{cases} \tag{27}$$

$$\omega t = \pi \Rightarrow V_2(t) \text{ is minimum} \Rightarrow \frac{B - A - V_{DD}}{R} + 2K\{[B + A\cos(\frac{\pi}{N}) - V_{th}](B - A) - \frac{(B-A)^2}{2}\} = 0 \tag{28}$$

$$\omega t = -\frac{\pi}{N} \Rightarrow V_1(t) \text{ is minimum} \Rightarrow \frac{B + A\cos(\frac{\pi}{N}) - V_{DD}}{R} + \omega CA\sin(\frac{\pi}{N}) + K(B - A\cos(\frac{2\pi}{N}) - V_{th})^2 = 0 \tag{29}$$

$$\omega t = 0 \Rightarrow V_{2(t)} \text{ is maximum} \Rightarrow \frac{B + A - V_{DD}}{R} + K(B + A\cos(\frac{\pi}{N}) - V_{th})^2 = 0 \tag{30}$$

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$$f = \frac{B + A\cos(\frac{\pi}{N}) - V_{DD} + RK(B - A\cos(\frac{2\pi}{N}) - V_{th})^2}{2\pi RCA\sin(\frac{\pi}{N})} \quad (31)$$

3.3 Analytical Equations for The Case that Transistors Enter Cut-Off region

Each transistor of an RO experiences the cut-off region in a period of oscillation if the loop gain increases. This occurs when the expression (32) is not satisfied.

$$B - A \le V_{th} \quad (32)$$

where A, B are obtained by solution of (28) and (29). Fig. 6 shows a period of oscillation in the case that the expression (32) is not satisfied. This plot shows the all operating regions that a transistor may enter under this condition. Fig. 7 shows the circuit model for a delay stage while each state occurring. At the beginning of the period, transistor is off because of the low voltage at its gate connection, so the circuit is modeled as an RC circuit with a time constant. The transistor meets the saturation region when the voltage at the Gate connection overcomes the threshold voltage, V_{th}. In this state, the transistor can be modeled as a voltage controlled current source (VCCS) and increasing the gate voltage increases the current and causes the charge of the capacitor decreases. If the Drain-Gate voltage of the transistor becomes higher than threshold voltage, V_{th}, transistor experiences deep triode and triode region respectively.

Here, the transistor can be modeled as a small voltage controlled resistor that is parallel with load resistor, R, so the output voltage decreases with a small time constant because of small load resistor. Calculating the all break points and time constants is more difficult and not necessary for the case.

A simple method based on a novel approximation is proposed here. Because of short times in each period that transistors are in saturation and deep triode, it can be assumed that transistors are only in triode and cutoff. Hence, the output voltage is assumed as a triangular-like periodic waveform. The output voltage at each stage is written as (33).

$$V_N(t) = \begin{cases} V_{DD}(1 - e^{-t/RC}) & \text{for } 0 < t < t_m \\ 0 & \text{for } t_m < t < T \end{cases} \quad (33)$$

Fig. 8 shows sample waveforms and the estimated waveform for a three stage RO under this condition. Because of the phase relation between outputs, each transistor can experience the off region for only T/N of time at the end of each period. Hence, the unknown parameters, t_m, V_m, that are shown in Fig. 8 can be easily obtained. Equation (33) can be written for $V_2(t)$ at the time t_m as (34) and because of the phase relation, the output $V_1(t)$ is written as (35).

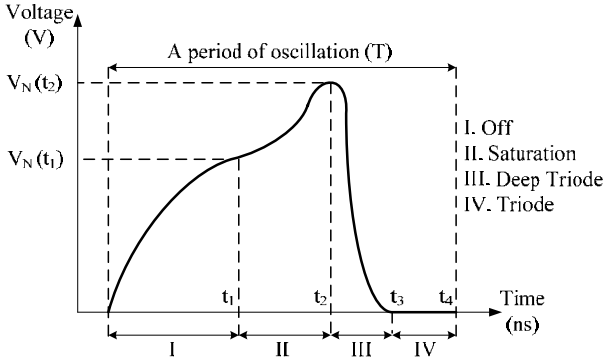

Fig. 6. A period of oscillation of output voltage for the case that the transistors experience all possible regions.

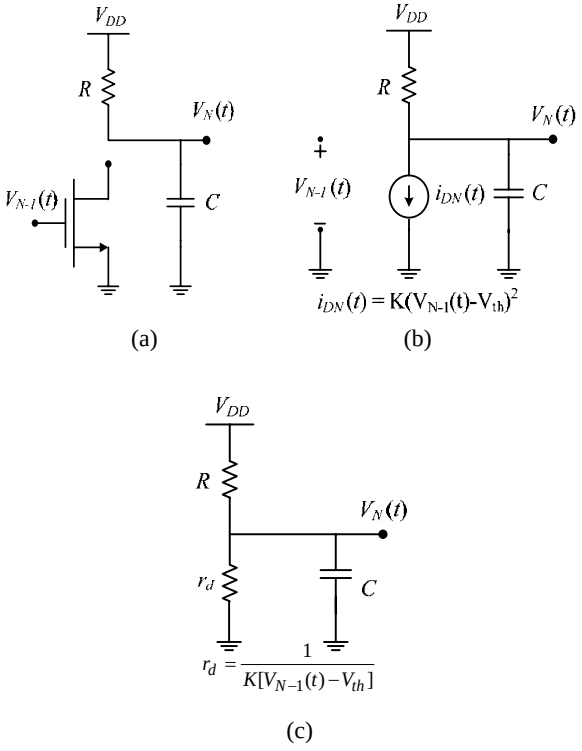

Fig. 7. Circuit models for each state occur in Fig.. 6. a) transistor off b) transistor is in saturation c) triode and deep triode region

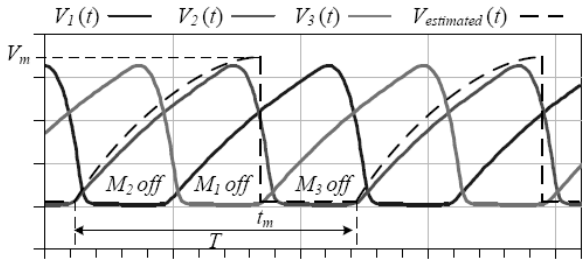

Fig. 8. A period of oscillation of output voltage for the case that transistors meet all regions.

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$$V_2(t_m) = V_{DD}(1 - e^{-t_m/RC}) \quad (34)$$

$$V_1(t) = V_2(t - T/N) = V_{DD}(1 - e^{-(t_m - T/N)/RC}) \quad (35)$$

An additional condition here is the voltage at gate-drain junction must satisfy (36) for edge of triode region. This condition occurs at time t_m referring (37), (38) and Fig. 8. Substituting (34)-(37) the unknown parameters can be defined as a function of T. Therefore, the only unknown parameter after all is period of output waveform, T.

$$V_2(t_m) - V_1(t_m) = V_{th} \quad (36)$$

$$V_{DD}[1 - e^{-t_m/RC}] - V_{DD}[1 - e^{-(t_m - \frac{T}{N})/RC}] = V_{th} \quad (37)$$

$$t_m = RCLn\frac{V_{DD}(e^{T/NRC} - 1)}{V_{th}} \quad (38)$$

The same expression can be used for V_1(t) at the time T as (39)-(40). Substituting (38)-(41) result in an equation for the period of time, T, as (42).

$$V_1(T) = V_2(T - T/N) = V_2[\frac{(N-1)}{N}T] = V_m \quad (39)$$

$$V_m = V_2(t_m) = V_{DD} - V_{th}(e^{T/NRC} - 1)^{-1} \quad (40)$$

$$V_{DD}[1 - \exp(-\frac{N-1}{N}.\frac{T}{RC})] = V_m \quad (41)$$

$$T = \frac{N}{N-1}RC\ln(\frac{V_{DD}}{V_{DD} - V_m}) \quad (42)$$

4 Simulation Versus Analytical Results

To evaluate the proposed method and compare with competitive methods, a test benchmark is created in this section using Advanced Design System software. The TSMC 1.8 V, 0.18 µm CMOS process have been used in simulations. Table 3 gives the details of technology, supply voltage, load capacitor, size and threshold voltages of the transistors used in simulations. First, a single-ended ring oscillator is simulated using different values of load capacitor for different oscillation frequencies. The sizes of the transistors were chosen here such that the circuit would oscillate over a wide range of capacitor. Different size of transistors is chosen to obtain all possible conditions in each experiment because of the direct relation between the amplitude of outputs and the loop gain. Higher loop gain causes higher amplitude; consequently more nonlinear behavior and different waveforms are available. Due to this, the size of the devices is changed in a wide range to test the circuit in different scenarios. For instance, the smaller transistor results in the smaller loop gain so that the outputs are fine sinusoid wave forms. The frequency is plotted as a function of C_L in this case. Second experiment is performed while the both number of delay stages and the sizes of the transistors are changed. In the third experiment, the amplitude and the frequency of oscillation are measured while load resistor is varied under simulation steps. These simulations are repeated for the cases that transistors change the operation region. The devices are larger to have more amplitude, so the change of operation regions is guaranteed in each scenario.

Table 2. Comparison between simulation results and calculated unknown parameters when devices enter the cutoff region

Load Capacitor C_L (pF)	Simulation results		Calculated values	
	Period (T) (nsec)	t_m (nsec)	Period (T) (nsec)	t_m (nsec)
1	1.11	0.63	0.90	0.58
2	1.22	0.71	1.13	0.70
3	1.43	0.82	1.36	0.84
4	1.65	0.93	1.58	0.97
5	1.81	1.02	1.80	1.11
6	1.96	1.10	2.03	1.24
7	2.15	1.20	2.26	1.38
8	2.30	1.30	2.48	1.50
9	2.44	1.40	2.69	1.65
10	2.59	1.63	2.92	1.80
Peak Voltage (V_m)	1.12 Volts		1.4 Volts	

Table 3. Details of Technology, Supply Voltage, Load Capacitor Range, Size and Threshold Voltages of Transistors

Technology TSMC 0.18 µm	
Supply Voltage	1.8 V
L_{min}	0.18 µm
µn.Cox	275.6×10^{-6} F/(V.s)
Capacitor (max/min)	10 pF / 1 pF
Size for Saturation (W/L)	50
Size for Triode (W/L)	80
Size for Cut-off (W/L)	300
V_{TN} (normal/low)	0.47 V / 0.267 V
V_{TP} (normal/low)	-0.46 V / -0.37 V

The calculated frequency by the proposed equations, (20), (21) and (22) when transistors are in the saturation region are compared with the simulation results

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obtained by the other methods. These comparisons are illustrated in Fig. 9 which shows the accuracy of proposed method. The equation that has been presented in [12] is inaccurate and it was eliminated from the results to have better comparison. Fig. 10 illustrates the simulation results compared with analytical equations (28), (29) and (31) for the case that the transistors meet both saturation and triode region during oscillation. A numerical method using MATLAB software is used to solve the equations (28) and (30) to obtain the amplitude and DC level of output. For the case that transistors enter the cutoff region, Fig. 11 shows the simulation results and the estimated output waveform of one stage. The unknown parameters of the estimated output are calculated by equations (38), (39), (43). Estimated results and actual values undergoes the variation of output capacitance are given in Table 2. In this experiment, the unknown parameters of the estimated outputs are calculated by equations (38), (39), (43) and a comparison between estimated and real values shows the accuracy of analytical equations. Based on the presented plots, it is evident that the equations proposed in this paper appear to be more accurate for all simulations in comparison with the others.

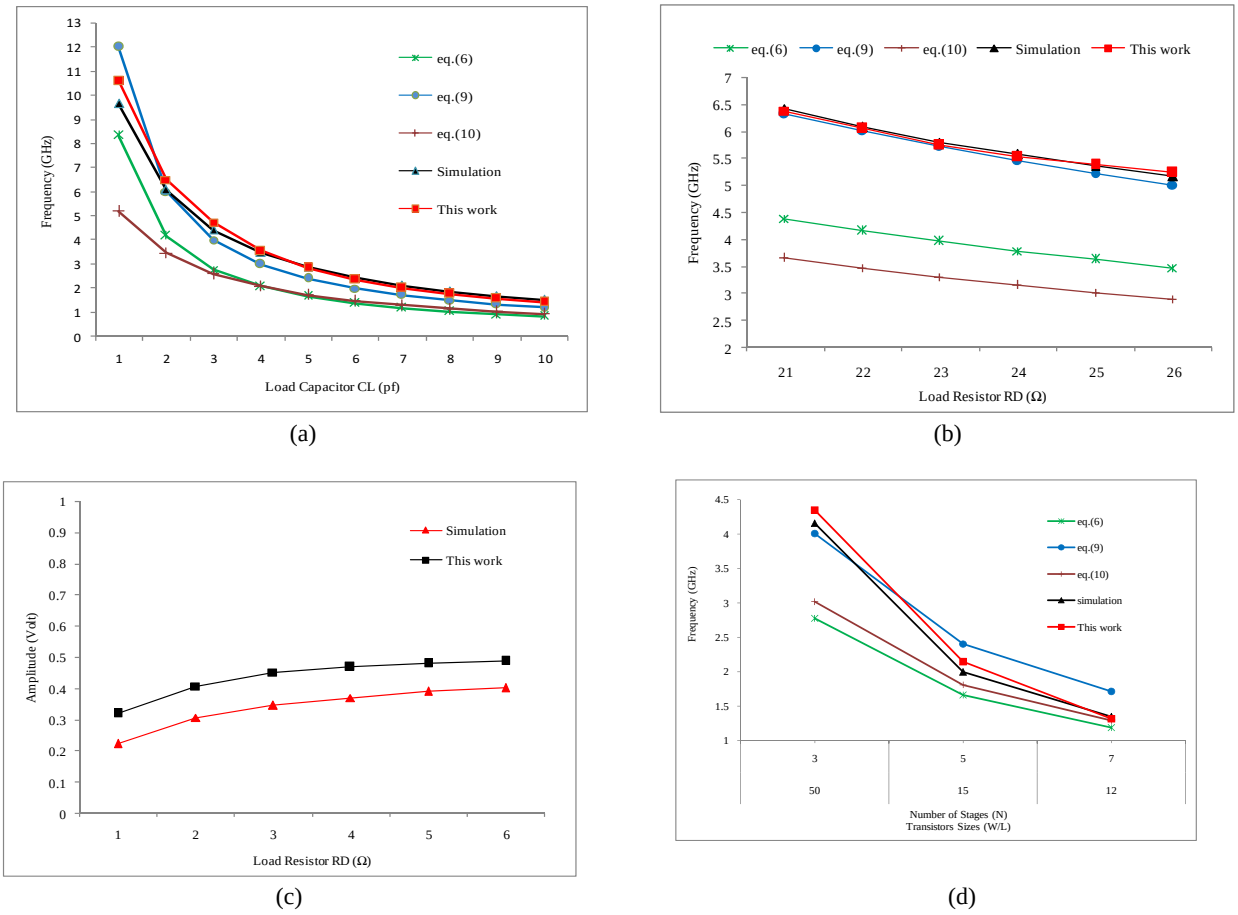

Fig. 9. Comparison of simulation and analysis results when transistors are in saturation region.
(a) Frequency versus C_L (b) Frequency versus R_D (c) Amplitude versus R_D (d) Frequency versus (N, W/L)

5 Conclusion

This paper has presented a novel method to derive exact analytical equations for the amplitude and frequency of ring oscillators. The output signal is assumed a sinusoidal waveform where the unknowns are amplitude, frequency and DC level. Applying the large signal analysis, the equations derived in this paper represent both amplitude and frequency more accurately than previous equations for a ring oscillator. Nonlinear behavior of an oscillator can be explained easily with the presented equations. Also, the equations are provided for all operation regions of transistors but the effect of channel length modulation and more parasitic element are challenging points that limits the analysis. These equations will be of significant to be used in guiding ring oscillator design. It also can provide designers more insight not only into design methodology, but also for estimating the phase noise, injection locking, etc; future works one may perform.

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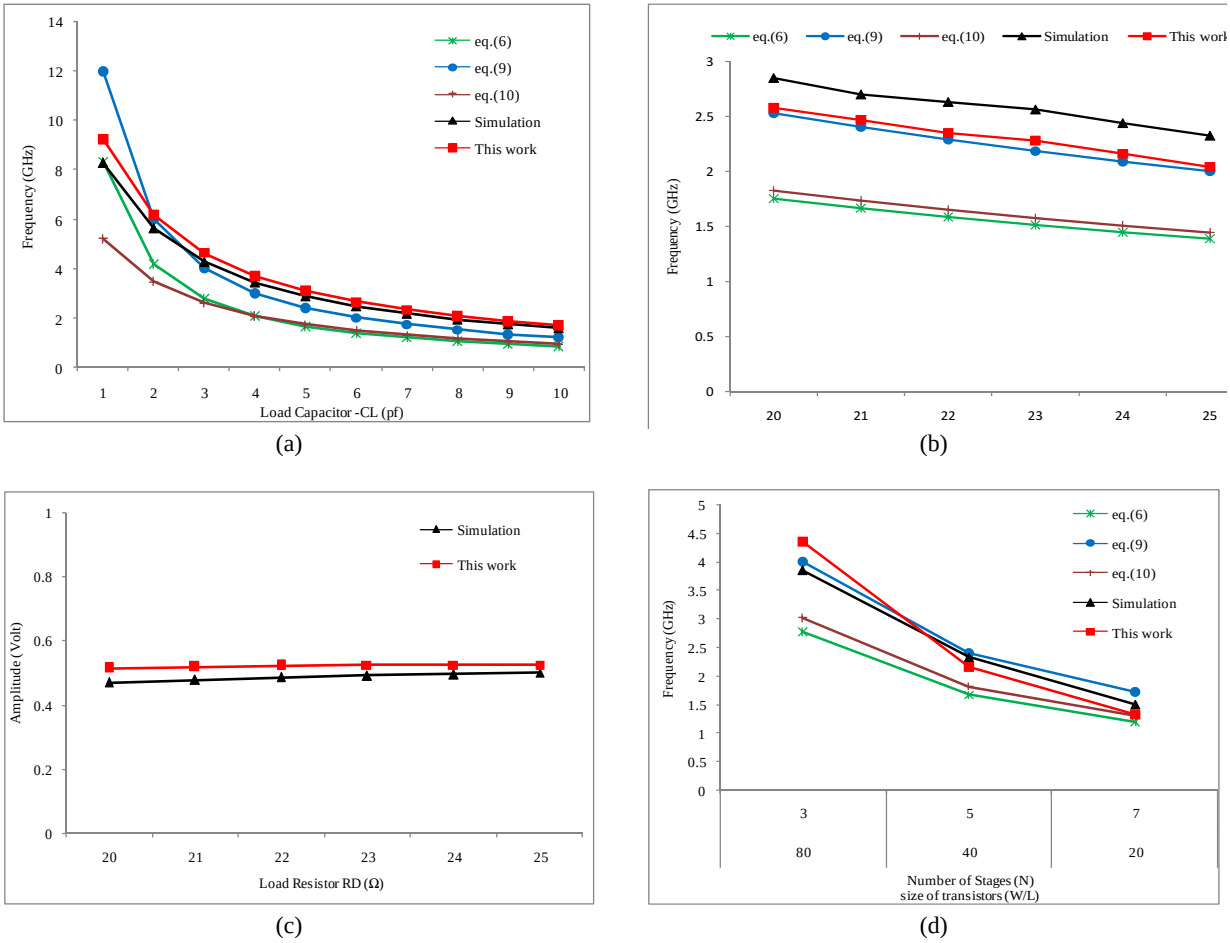

Fig. 10. Comparison of simulation and analysis results when transistors meet the triode region
(a) Frequency versus C_L (b) Frequency versus (N, W/L) (c) Amplitude versus R_D (d) Frequency versus R_D

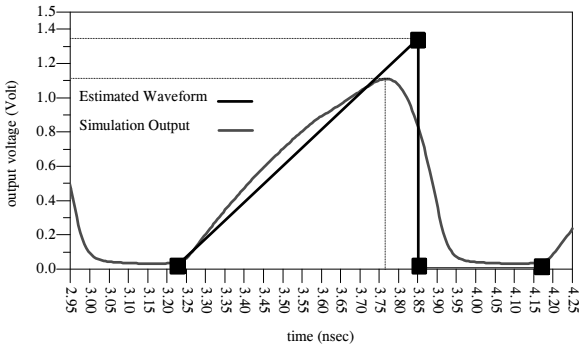

Fig. 11. Sample output voltage of an RO and the estimated waveform for the case that transistors meet cut-off region.

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