A Micropower Current-Mode Euclidean Distance Calculator for Pattern Recognition

E. Farshidi*

Abstract: In this paper a new synthesis for circuit design of Euclidean distance calculation is presented. The circuit is implemented based on a simple two-quadrant squarer/divider block. The circuit that employs floating gate MOS (FG-MOS) transistors operating in weak inversion region, features low circuit complexity, low power (<20uW), low supply voltage (0.5V), two quadrant input current, wide dynamic range and immunity from body effect. In addition, this circuit is designed in modular methodology, leading to a very regular structure. The circuit was successfully applied to the recognition of some simple patterns. Simulation results of the circuit by HSPICE show high performance in the separation and confirm the validity of the proposed technique.

Keywords: Euclidean distance calculator, pattern recognition, current-mode.

1 Introduction

Euclidean distance calculation, which is a direct measure of the similarity between two vectors [1-6], is a useful technique for pattern recognition by analyzing groups of vector data [3-6]. In fact, it can be employed to find optimum prototype vector, from which the input vector is compared. There are two ways to implement Euclidean distance calculator. One is employing digital computer, and the other is using analog circuits. Analog implementation of Euclidean distance calculator holds a series of advantages over digital implementation. The complexity of analog circuit blocks required to implement such systems is in general lower when compared with digital counterpart and, additionally, A/D and D/A interfaces towards sensors and actuators are not needed. Moreover, better performances can be obtained in terms of velocity of signal processing, by fully exploiting the capability of analog circuits to implement parallel processing. Because, it would be intolerably time consuming when the number of template patterns becomes quite large and the problem is in excess of even the state-of-the-art computer technologies. Hence, analog implementation employing parallel very-large-scale integration (VLSI) architectures is desired for real-time Euclidean distance calculator circuits. Recently some analog integrated forms of Euclidean distance calculator have been proposed [1-6]. One attempt is to design vector summation circuit in voltage-mode approach based on the bipolar dynamic translinear implementation [1]. However, in many situations, particularly in mixed A/D systems, it is desirable to implement the circuits in MOS technology [2]. But, in traditional voltage-mode architectures, the supply voltage level reduction has a clear impact on the dynamic range of the circuits. Current-mode approach deserves particular mention since it provides a large dynamic range for the currents considered now as processing variables, while maintaining reduced voltage swings. In current–mode processing the input signals which are mostly in current domain are nonlinearly transformed to the compressed voltage signal domain. Taking advantages of the current-mode approach, Euclidean distance calculator circuits were proposed in current-mode [3-6]. In these proposals, Euclidean distance calculator circuit has been performed by several basic building blocks, such as geometric-mean, squarer/divider, absoluter and subtracter. For design of these functions, stacked translinear loop [3-5] or class-AB linear transconductors [6] have been employed. The main drawbacks of theses proposed circuits are as follows: firstly, the extra needed functions lead to a large number of transistors and high power consumption; Secondly, in the circuit of stacked translinear MOSFET loops similar to class-AB transconductance, the body effect decreases the accuracy. Thirdly, in these circuits, the MOS transistors are operating in strong inversion, which are not capable to operate under low-power applications and will cause

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* E. Farshidi is with the Department of Electrical Engineering, Shahid Chamran University of Ahvaz, Ahvaz, Iran, 61357-831351
E-mail:Farshidi@scu.ac.ir

to restriction of dynamic range for low supply voltage applications. Energy efficiency of information processing is a key design criterion in the development of ultra-low-power systems. Low supply voltage and power consumption levels in the microwatt range demands novel analog design strategies specifically suited to this new scenario. These requirements confront designers with the search for new techniques, to revisit current methodologies and/or to find versatile elements. One of new ones is using FG-MOS transistors that are operating in weak inversion region [7, 8]. Therefore, analog current-mode circuit technique combined with the FG-MOS transistors that operate in weak inversion can lead to compact efficient circuits suitable for this purpose.

In this paper to overcome the above problems, a novel synthesis for current-mode Euclidean distance calculator is presented. In the presented synthesis, the number of basic building blocks is severely reduced and it just comprises simple two-quadrant squarer/divider unit [7, 9] as the fundamental unit. Therefore, the system complexity of the proposed system is much less than those reported before [3-6]. The full parallel property of the system reduces the identification time and lead to a very regular structure. In the presented synthesis, the squarer/divider unit is implemented with two-quadrant input using FG-MOS transistors. As, the proposed squarer/divider circuit operates in two-quadrant input, so the absoluter and subtracter units are not needed. In this circuit, the source of transistors is connected to the substrate; therefore, the proposed circuit is immune to the body effect. Also due the fact that the transistors are operating in weak inversion, the proposed circuit features low-power, low-voltage and wide dynamic range.

The paper is organized as follows. In section 2 mathematical theory and analysis of current-mode Euclidean distance calculator is discussed. Section 3 explains the proposed circuit design for two-quadrant squarer/divider unit, as the basic building block of Euclidean distance calculator. In section 4 no ideal effects is presented. Simulation results are presented and discussed in section 5 and concluding remarks are provided in section 6.

2 Analysis of Current-Mode Euclidean Distance Calculator

Euclidean distance calculator is attractive solution to pattern recognition when it is implemented for computing in parallel systems. It is the basis of finding optimal prototype vectors, from which the input vectors is compared. Hence, in this method, the similarity between each template V and an input unknown pattern U is measured by calculating the Euclidean distance $\mathrm{D}(\mathrm{U},\mathrm{V})$. The less distance $\mathrm{D}(\mathrm{U},\mathrm{V})$ is, the more similarity between V and U is. In other words, the Euclidean distance is a direct measure of similarity between the template vectors that is closest to an input vector, in the sense that among a finite set of reference vectors, the least distant one from the input is the most similar to the input [3-6]. The Euclidean distance between two *n*-dimensional vectors:

$$U = \begin{pmatrix} u_1 & u_2 & \dots & u_K \end{pmatrix} \tag{1}$$

and

$$V = \begin{pmatrix} v_1 & v_2 & \dots & v_K \end{pmatrix} \tag{2}$$

is represented as follows:

$$D(U,V) = \sqrt{\sum_{k=1}^{K} (u_k - v_k)^2} \tag{3}$$

where u_k and v_k are the *k*-th entry of vectors *U* and *V*, respectively.

By rearranging the definition for *K*-dimension vectors *V* and U in order to hardware implementation of the Euclidean distance circuit, (1) and (2) are expressed as follows:

$$I_U = \begin{pmatrix} I_{u_1} & I_{u_2} & \dots & I_{u_K} \end{pmatrix} \tag{4}$$

$$I_V = \begin{pmatrix} I_{v_1} & I_{v_2} & \dots & I_{v_K} \end{pmatrix} \tag{5}$$

where I_U and I_V are the current representation of vectors U and V, respectively. Also, I_{u_k} and I_{v_k} are the *k*-th entry of vectors I_U and I_V, respectively.

Employing current-mode approach, an equivalent function of (3) in current-mode is given as follows:

$$I_D = \sqrt{\sum_{k=1}^{K} \left(I_{u_k} - I_{v_k}\right)^2} \tag{6}$$

where I_D is the current representation of Euclidean distance $\mathrm{D}(\mathrm{U},\mathrm{V})$.

One straight method to circuit design of (6) is using a square-rooter and K squarer units, in addition of *K* subtracter units and K absoluter units [3-6]. However, an effective way is suggested in this work to reduce the number of basic building blocks. To this end, squaring operation is taken on both sides of (6), which results:

$$I_D^2 = \sum_{k=1}^{K} \left(I_{u_k} - I_{v_k}\right)^2 \tag{7}$$

A mathematically equivalent expression, but more precise considering the offset of the system [10], is obtained as:

$$I_D = \frac{\sum_{k=1}^{K} I_{d_k}^2}{I_D} \tag{8}$$

where I_{d_k} is the difference between *k*-th entry of two vectors U , V and it is equal to:

$$I_{d_k} = I_{u_k} - I_{v_k} \tag{9}$$

By breaking out the weighted summation of the numerator terms of (8), and also using the fact that $\frac{1}{y}\sum_i x_i = \sum_i \frac{x_i}{y}$, it can be rewritten as:

$$I_D = \sum_{k=1}^{K} \frac{I_{d_k}^2}{I_D} = \sum_{k=1}^{K} I_{SD,k} \tag{10}$$

where $I_{SD,k}$ is equal to:

$$I_{SD,k} = \frac{I_{d_k}^2}{I_D} \tag{11}$$

The right hand side of (11) is summation of n two-quadrant squarer/divider units. For each squarer/divider unit, the output current is $I_{SD,k}$ and the input currents are: difference between k-th entry of two vectors U, V (I_{d_k}), as the squared input of the unit and the output current of Euclidean distance calculator (I_D), as the divisor input of the unit. It should be pointed out that the squared input current in the numerator of squarer/divider unit is bidirectional current signal. Hence, the squarer/divider unit should be designed to operate two-quadrant.

Fig. 1 shows block diagram of the current-mode Euclidean distance calculator. In this figure, Euclidean distance calculation consists of K two-quadrant squarer/divider units that are connected in parallel form, according to (10). From this figure, it can be seen that to design Euclidean distance calculator it is just needed to design two-quadrant squarer/divider unit, as the fundamental unit. Therefore, the number of basic building blocks in the presented synthesis is severely reduced compared to the other proposed that reported before [3-6].

3 Circuit Design of the Proposed Squarer/Divider

The squarer/divider unit can be implemented by using of sigma-delta data converter [11], MOS translinear [3-5], or class-AB transconductance [6] circuits. All these above mentioned squarer/divider circuits operate in only one-quadrant input current. Additionally, employing sigma-delta converter needs a large number of transistors, switches, and capacitors that leads to a high circuit complexity, chip area and power consumption [11]. MOS translinear circuits can be categorized as follows: stacked loop, up-down loop and electronically simulated loop [12]. The stacked loop [3-5] similar to class-AB transconductance [6] suffers from body effect. Influence of the body effect in up-down loop [13] is smaller than in stacked loop but more circuits for current injection in transistors are required. In addition, for all squarer/divider units that previously reported in [3-6] and [11-13], transistors are working in saturated strong inversion, which lead to high power consumption and restricted dynamic range for low-voltage applications.

The proposed squarer/divider is designed based on the use of the FG-MOS transistors that operate in weak inversion [8]. A FG-MOS transistor with *N* input voltages consists of a floating gate electrode extended over the channel and *N* input gates located over the floating gate. In other words, the FG-MOS transistor is a MOS transistor with an isolated gate that capacitively coupled to the inputs. Fig. 2 shows the symbol diagram and equivalent circuit of the transistor with 2 input voltages. The drain current of a p-type FG-MOS transistor in weak inversion region is given by [8]:

$$I_d = I_s \exp\left(\frac{V_{dd} - V_{FG}}{nU_T}\right) \tag{12}$$

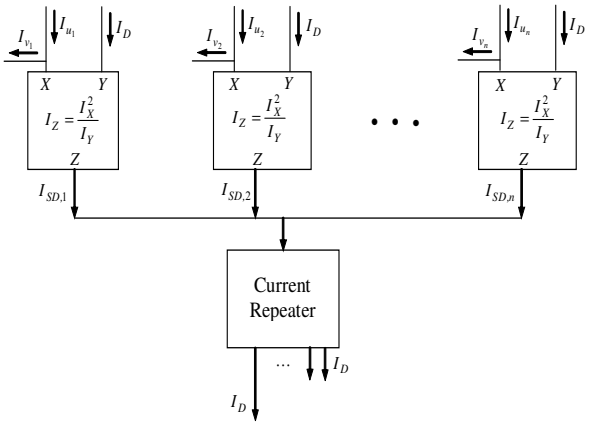


Fig. 1. Block diagram of the proposed current-mode Euclidean distance calculator

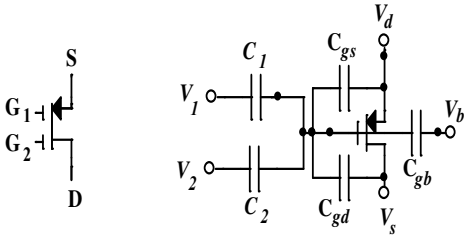


Fig. 2. Symbol diagram (left) and equivalent circuit (right) for a p-type FG-MOS transistor

where U_T stands for the thermal potential, I_s is a device dependent coefficient, n represents the subthreshold slope and V_{FG} is voltage of floating gate electrode.

Applying charge conservation law, the voltage at the floating gate with 2 equal input capacitances, which is used in this work, is obtained by:

$$V_{FG} = w_1V_1 + w_2V_2 + \frac{C_{gd}}{C_t}V_{gd} + \frac{C_{gs}}{C_t}V_{gs} + \frac{C_{gb}}{C_t}V_{gb} + \frac{Q_{fg}}{C_t} \quad (13)$$

In (13), V_i is the *i*-th input gate voltage $(i \in \{1,2\})$, C_t is the sum of capacitors that are connected to the floating-gate, C_{gd}, C_{gs}, C_{gb} are the parasitic capacitors between the floating gate and the drain, source and bulk, respectively, Q_{fg} is residual charge trapped at the floating gate during fabrication process (This latter charge can be made negligible by using the technique described in [14]) and w_i is input capacitance ratio of *i*-th input gate, and is defined as:

$$w_i = \frac{C_i}{C_t} \quad (14)$$

in which C_i is the input capacitance between the floating gate and the *i*-th input gate. From (14) it is evident that the input capacitance ratios of FG-MOS transistor with 2 equal input capacitances are 1/2 $(w_i = 1/2)$.

If the sum of input capacitances is much larger than parasitic capacitances, i.e.,

$$C_1 + C_2 >> C_{gd}, C_{gs}, C_{gb} \quad (15)$$

then using (13), the voltage at floating gate with 2 equal input capacitances can be approximated by:

$$V_{FG} \cong \frac{1}{2}V_1 + \frac{1}{2}V_2 \quad (16)$$

Substituting (16) into (12), the drain current of a p-type FG-MOS transistor, with 2 equal input capacitances, is as follows:

$$I_d = I_s \exp\left(\frac{1}{nU_T}\left(V_{dd} - \left(\frac{1}{2}V_1 + \frac{1}{2}V_2\right)\right)\right) \quad (17)$$

To make the input current of the squarer/divider operate in two-quadrant with positive and negative currents, a new synthesis by employing of FG-MOS transistors is presented. This will cause the squarer/divider to act as a full wave rectifier. To this end, each input current I_d of (11) is split into its differential representation (I_{dp}, I_{dn}) which are both strictly positive and are related to I_d by:

$$I_d = I_{dp} - I_{dn} \quad (18)$$

Substituting (18) into (11), the output current of each squarer/divider of Euclidean distance calculator is obtained as follows:

$$I_{SD} = \frac{(I_{dp} - I_{dn})^2}{I_D} \Rightarrow \quad I_{SD} = \frac{I_{dp}^2}{I_D} + \frac{I_{dn}^2}{I_D} - 2\frac{I_{dp}I_{dn}}{I_D} \quad (19)$$

The right hand side (RHS) of (19) consists of three one-quadrant functions: two one-quadrant squarer/dividers and one one-quadrant multiplier/divider. For implementation of these functions, the p-type FG-MOS transistors are employed. Fig. 3 shows the circuit of a one-quadrant squarer/divider consisting of three FG-MOSs, where it is assumed all transistors are operating in weak inversion region. The I-V relationships for transistors M1, M2 and M3 with 2 equal input capacitances are given by:

$$I_1 = I_{s1}\exp\left(\frac{1}{n1U_T}\left(V_{dd} - \left(\frac{1}{2}V_1 + \frac{1}{2}V_1\right)\right)\right) \quad (20)$$

$$I_2 = I_{s2}\exp\left(\frac{1}{n2U_T}\left(V_{dd} - \left(\frac{1}{2}V_2 + \frac{1}{2}V_2\right)\right)\right) \quad (21)$$

$$I_3 = I_{s3}\exp\left(\frac{1}{n3U_T}\left(V_{dd} - \left(\frac{1}{2}V_1 + \frac{1}{2}V_2\right)\right)\right) \quad (22)$$

Squaring both sides of (22) and then substituting (20) and (21) into it, the following expression will be obtained:

$$\left(\frac{I_3}{I_{s3}}\right)^{2n3} = \left(\frac{I_1}{I_{s1}}\right)^{n1}\left(\frac{I_2}{I_{s2}}\right)^{n2} \Rightarrow \quad \left(\frac{I_1}{I_{s1}}\right)^{n1} = \frac{\left(\frac{I_3}{I_{s3}}\right)^{2n3}}{\left(\frac{I_2}{I_{s2}}\right)^{n2}} \quad (23)$$

By assumption that FG-MOS transistors M1, M2 and M3 are identical, i.e., $n1 = n2 = n3 = n$ and $I_{s1} = I_{s2} = I_{s3} = I_s$, then, (23) will be converted to $I_1 = I_3^2 / I_2$. Therefore a one-quadrant squarer/divider

circuit is obtained by taking a copy of I_1 as the output, while I_2 and I_3 are as the inputs.

Fig. 4 shows the circuit of a one-quadrant multiplier/divider which consists of four FG-MOSs that operate in weak inversion**.** The I-V relationships for transistors M1, M2, M3 and M4 with 2 equal input capacitances are given by:

$$I_1 = I_{s1}\exp\left(\frac{1}{n1U_T}\left(V_{dd}-\left(\frac{1}{2}V_3+\frac{1}{2}V_4\right)\right)\right) \quad (24)$$

$$I_2 = I_{s2}\exp\left(\frac{1}{n2U_T}\left(V_{dd}-\left(\frac{1}{2}V_2+\frac{1}{2}V_2\right)\right)\right) \quad (25)$$

$$I_3 = I_{s3}\exp\left(\frac{1}{n3U_T}\left(V_{dd}-\left(\frac{1}{2}V_2+\frac{1}{2}V_3\right)\right)\right) \quad (26)$$

$$I_4 = I_{s4}\exp\left(\frac{1}{n4U_T}\left(V_{dd}-\left(\frac{1}{2}V_2+\frac{1}{2}V_4\right)\right)\right) \quad (27)$$

Multiplication of (24) by (25) and also (26) by (27), and then comparing the results, it is obtained as follows:

$$\left(\frac{I_3}{I_{s3}}\right)^{n3}\left(\frac{I_4}{I_{s4}}\right)^{n4}=\left(\frac{I_1}{I_{s1}}\right)^{n1}\left(\frac{I_2}{I_{s2}}\right)^{n2}\Rightarrow$$

$$\left(\frac{I_1}{I_{s1}}\right)^{n1}=\frac{\left(\frac{I_3}{I_{s3}}\right)^{n3}\left(\frac{I_4}{I_{s4}}\right)^{n4}}{\left(\frac{I_2}{I_{s2}}\right)^{n2}} \quad (28)$$

By assumption that FG-MOS transistors M1, M2, M3 and M4 are identical, i.e., $n1=n2=n3=n4=n$ and $I_{s1}=I_{s2}=I_{s3}=I_{s4}=I_s$, then, (28) will be converted to $I_1 = I_3 I_4 / I_2$. Therefore, a one-quadrant multiplier/divider circuit is obtained by taking a copy of I_1 as the output, and copies of I_2, I_3 and I_4 as the inputs.

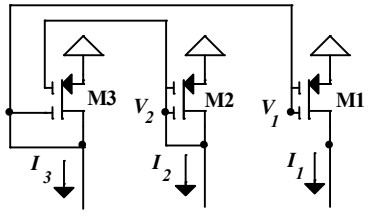


Fig. 3. FG-MOS based one-quadrant squarer/divider

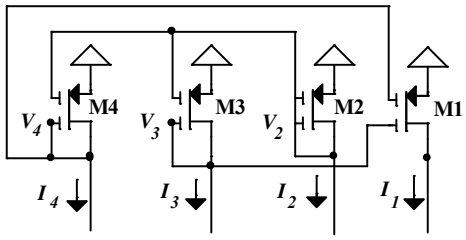


Fig. 4. A FG-MOS based one-quadrant multiplier/divider

Therefore, a one-quadrant multiplier/divider circuit is obtained by taking a copy of I_1 as the output, and copies of I_2, I_3 and I_4 as the inputs.

Fig. 5 shows the complete circuit of the proposed two-quadrant squarer/divider circuit which is implemented based on (18) and (19). In this figure, Transistors M1, M4 and M5 similar to transistors M2, M4 and M6 form two one-quadrant squarer/dividers for implementation of the first and second terms of RHS of (19) according to Fig. 3. Also, Transistors M3, M4, M5 and M6 form a one-quadrant multiplier/divider. This multiplier/divider and current mirror transistors (M9, M10) are employed for implementation of the third term of RHS of (19) according to Fig. 4. It should be pointed out that, the common elements of these three circuits are merged. For implementation of (18), transistors M5, M6, M7 and M8 are employed. As Fig. 5 shows, the sources of FG-MOSs are connected to the substrate, so the body effect is completely eliminated. The circuit complexity of this circuit is much lower than those of up-down and electronically simulated MOS translinear based circuits. Also, the figure shows the minimum supply voltage of the circuit is one V_{gs} plus one V_{ds}, and since the transistors are operating in weak inversion, therefore this circuit can work in low-power, low-voltage and wide dynamic range. In addition, combination of Fig. 1 and 5 reveal that the number of components in the proposed circuit is much less than those reported before [3-6].

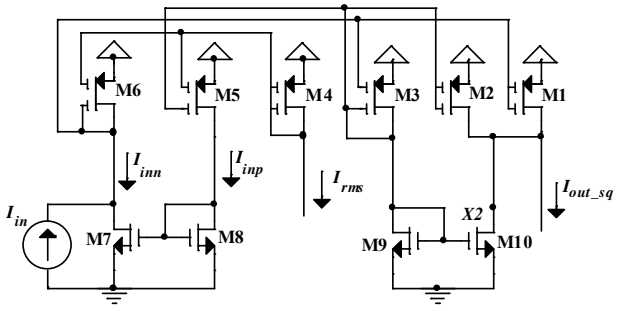


Fig. 5 Circuit diagram of the proposed two-quadrant squarer/divider

4 Non Ideal Effects

The expressions presented in the previous sections are valid by assumption that influences of the mismatching and thermal noise effects that cause deviations from the ideal relation of FG-MOS transistors are negligible. In this section analysis of mismatching of subthreshold slope, mismatching of saturation currents, thermal noise and quantization noise is described.

4.1 Mismatching in subthreshold slopes

If saturation current of transistors M1-M4 in (28) are identical ($I_{s1} = I_{s2} = I_{s3} = I_{s4} = I_s$) but the subthreshold slopes in this equation differ from the ideal values as follows (in order to find maximum deviation):

$$n1 = n\ ,\ n2 = n3 = n + \Delta n\ ,\ n4 = n - \Delta n \qquad (29)$$

then, accomplish a Taylor expansion ($\Delta n << n$) for the terms $(I_i)^{\pm\frac{\Delta n}{n}}$ ($i \in \{1,2,3,4\}$) in (28) gives:

$$(I_i)^{\pm\frac{\Delta n}{n}} \cong 1 \pm \frac{\Delta n}{n}\ln(I_i) \qquad (30)$$

Making rational power of both sides of (28) by $\frac{1}{n}$ and then substituting (29) and (30) into (28) results:

$$I_1 \cong \frac{I_3 \cdot I_4}{I_2} \cdot \frac{\left(1+\frac{\Delta n}{n}\ln I_3\right)\left(1+\frac{\Delta n}{n}\ln I_4\right)}{\left(1-\frac{\Delta n}{n}\ln I_2\right)} \Rightarrow$$

$$I_1 \cong \frac{I_3 I_4}{I_2}\left(1+\frac{\Delta n}{n}\ln I_3\right)\left(1+\frac{\Delta n}{n}\ln I_4\right)\left(1+\frac{\Delta n}{n}\ln I_2\right) \qquad (31)$$

$$\Rightarrow I_1 \cong \frac{I_3 \cdot I_4}{I_2} \cdot \left(1+\frac{\Delta n}{n}\left(\ln I_3 + \ln I_4 + \ln I_2\right)\right)$$

By assumption that $I_L \le I_i \le I_H$, maximum deviation of (31) from ideal is: $\frac{I_H^2}{I_L} \cdot \frac{\Delta n}{n} \ln I_H$. Evidently, Equation (23) is a special case of (28). Therefore, maximum deviation of (23) is the same as obtained for (28). In such case maximum deviation of output current I_D in (10) caused by mismatching in subthreshold slope is:

$$Max\_dev(I_D) = 3K\frac{I_H^2}{I_L} \cdot \frac{\Delta n}{n} \ln I_H \qquad (32)$$

4.2 Mismatching in saturation currents

A similar analysis can be done for saturation currents. If subthreshold slope of transistors M1-M4 in (28) are identical ($n1 = n2 = n3 = n4 = n$) but the saturation current slopes in this equation differ from the ideal values as follows (in order to find maximum deviation):

$$I_{s1} = I_s,\ I_{s2} = I_s - \Delta I_s,\ I_{s3} = I_{s4} = I_s + \Delta I_s \qquad (33)$$

Substituting (33) into (28) results:

$$I_1 = \frac{I_3 \cdot I_4}{I_2} \cdot \frac{\left(1+\frac{\Delta I_s}{I_s}\right)^2}{\left(1-\frac{\Delta I_s}{I_s}\right)} \qquad (34)$$

By assumption that ($\Delta I_s << I_s$), it results $\left(1+\frac{\Delta I_s}{I_s}\right)^2 \cong \left(1+\frac{2\Delta I_s}{I_s}\right)$ and $\left(1-\frac{\Delta I_s}{I_s}\right)^{-1} \cong \left(1+\frac{\Delta I_s}{I_s}\right)$. Thus (34) can be rewritten as follows:

$$I_1 = \frac{I_3 \cdot I_4}{I_2} \cdot \left(1+\frac{2\Delta I_s}{I_s}\right)\left(1+\frac{\Delta I_s}{I_s}\right) \Rightarrow$$

$$I_1 = \frac{I_3 \cdot I_4}{I_2} \cdot \left(1+\frac{3\Delta I_s}{I_s}\right) \qquad (35)$$

By assumption that $I_L \le I_i \le I_H$, maximum deviation of (35) from ideal is: $\frac{3I_H^2}{I_L} \cdot \frac{\Delta I_s}{I_s}$. Maximum deviation of (23) is the same as obtained for (28). Thus, maximum deviation of output current I_D in (10) caused by mismatching in saturation currents is:

$$Max\_dev(I_D) = 3K\frac{3I_H^2}{I_L} \cdot \frac{\Delta I_s}{I_s} \qquad (36)$$

4.3 Thermal noise

Shot noise represented by current source can be easily incorporated in equations of multiplier/divider and squarer/dividers. If each FG-MOS transistor that is biased with drain current $I_i(t)$ accompanied by a shot noise source $i_{n,i}(t)$, then it can be shown [15], equivalent noise at the output of multiplier/divider by using (28) is as follows:

$$I_{n-eq,1}(t) = I_1\left(\frac{i_{n,3}}{I_3} + \frac{i_{n,4}}{I_4} - \frac{i_{n,2}}{I_2}\right) + i_{n,1} \qquad (37)$$

As equation squarer/divider is a special case of a multiplier/divider, then, its equivalent noise is as follows:

$$I_{n-eq,1}(t) = I_1\left(\frac{2i_{n,3}}{I_3} - \frac{i_{n,2}}{I_2}\right) + i_{n,1} \qquad (38)$$

4.4 Quantization noise

If the patterns are partitioned into K grids, in which, each grid is quantized according to its color, i.e., the white/black color is represented by the currents I_H and I_L, then accepted noise of output current I_D, which is quantization noise, is equal to:

$$Quantization\_noise(I_D) = \frac{I_H - I_L}{K} \qquad (39)$$

It should be pointed out that quantization noise of (39) is inherent noise of the proposed circuit. Therefore, for proper operation, this noise should be lower than other non idealities such as thermal noise of (38), mismatching noises of (32) and (36).

5 Simulation Results

The current-mode Euclidean distance calculator circuit based on the block diagram of Fig. 1, and the proposed two-quadrant squarer/divider of Fig. 5 was designed. The circuit was simulated by HSPICE with TSMC 0.18um CMOS process parameters, confirming the accuracy of the proposed method. $V_{dd} = 0.5\text{V}$ and $I_N = 200\text{nA}$ were employed. The aspect ratios of the transistors were chosen 0.6um/0.3um. For all FG-MOS transistors, the value of the input capacitance ratio was assumed 1/2 and also the model of reference [16] is used.

To demonstrate application of this proposed Euclidean distance calculator circuit, this circuit is employed to template matching in pattern recognition system. As Fig. 6 shows, the patterns are partitioned into a 3x3 grid, in which each grid filled with either white or black color, and characterized, by a vector *P*. For circuit realization, each grid is quantized according to its color, i.e., the white/black color is represented by the current 300nA/100nA.

A transient simulation of the circuit was carried out in Fig. 7 for providing the similarity measure between three input testing patterns, denoted as $\text{Ui}\,(\text{i} \in \{1,2,3\})$, and nine template patterns, denoted as $\text{Vi}\,(\text{i} \in \{1,2,\ldots,9\})$. Fig. 8 shows the Euclidean distance between each input pattern and the nine template patterns. During simulation, the set of each input pattern corresponding to the input vector was held constant while on the 9 template patterns (corresponding to the template pattern vector) were serially recalled, beginning from vectors V1 until vector V9 (Fig. 7), recalling the next template pattern vector every 1 us. Under the above described conditions, the output, for the input patterns of U1, U2 and *U3* are shown in Fig. 8(a), Fig. 8(b) and Fig. 8(c), respectively. Evidently, the minimum of this distance suggests the nearest match between input pattern and template patterns. The results of simulation show that these template patterns with the maximum matching degree of the input patterns U1, U2 and U3 are V2, V6 and V4 at the times 1us, 5us and 3us, respectively. Because the output current of the proposed circuit functions as expected, taking the minimum value of Euclidean distance between the above mentioned input patterns and template patterns. These figures reveals that, these input patterns can be recognized correctly for this circuit and the simulation results are in agreement with the analysis calculations. The given example in the illustration showed that this circuit performs the function of a Euclidean distance calculation well. Simulation results show that the maximum power consumption of the Euclidean distance calculator circuit is less than 20uW. Also, identification time of 250ns and errors less than 1% can be found for input current amplitudes from 100nA to 300nA. This input range with low supply voltage is wider than those reported before [3-6]. With the parallel processing characteristic and the mentioned merits, this circuit is suited for analog implementation of Euclidean distance calculator algorithm. To provide more insight into the technique proposed here, a comparison was made with formerly reported current-mode Euclidean distance calculator circuit in Table I. From this table, supply voltage and power consumption of the proposed Euclidean distance circuit is lower than other reported before [3-6]. In addition, the proposed circuit is two quadrant input current, and also it is immune from body effect.

P1	P2	P3
P4	P5	P6
P7	P8	P9

P

Fig. 6. The schedule of the entries (*p1* to *p9*) of the pattern vector *P*

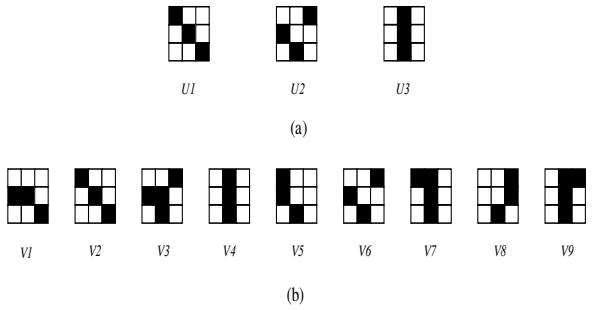
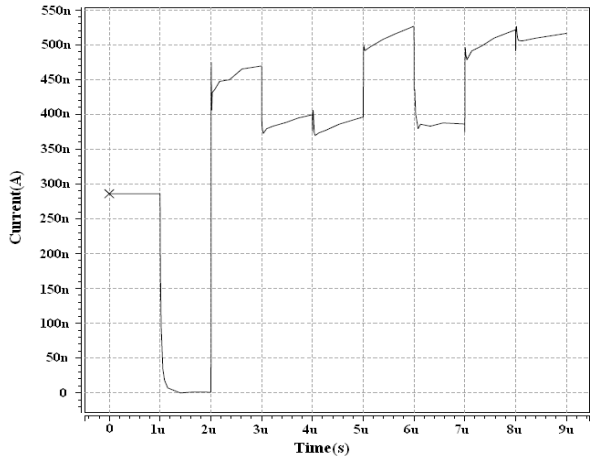
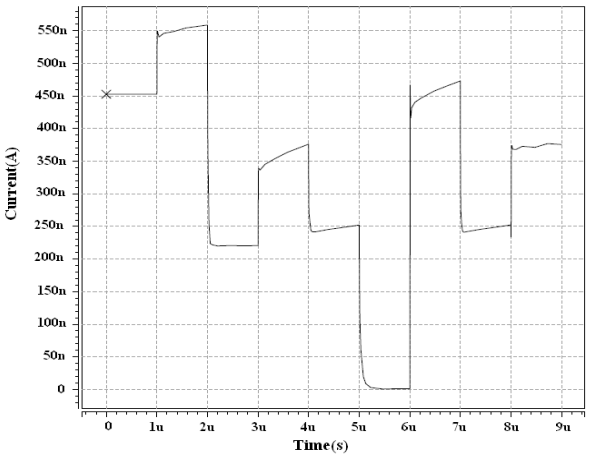


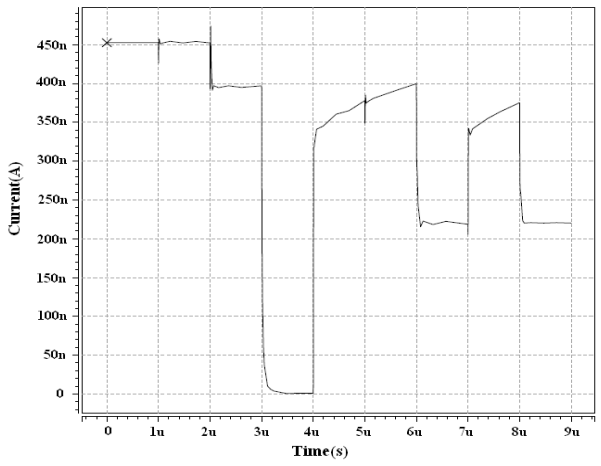
Fig. 7. a) Input patterns Ui (up) b) Template patterns Vi (down)



(a)



(b)



(c)

Fig. 8. Time response of the Euclidean distance calculator circuit for input patterns of a) U1 b) U2 c) U3

Table 1. A comparison between some Euclidean Distance Circuits

Parameter	Ref. [3, 4]	Ref. [5]	Ref. [6]	This Work
Technology	0.6u	0.35u	0.5u	0.18u
Supply Voltage	$2V_{gs}+V_{ds}$ (3.3V)	$2V_{gs}+V_{ds}$	$2V_{gs}+V_{ds}$ (3.3V)	$V_{gs}+V_{ds}$ (0.5V)
Power Consumption	15mW	Expected >10mW	16mW	<20uW
Circuit Complexity (Transistor Count)	>250	>50	>300	100
Body Effect	Yes	Yes	Yes	No
Operation Area of Squarer Input	1 Quad.	1 Quad.	1 Quad.	2 Quad.
Error	1%	Not Reported	Not Reported	1%

6 Conclusion

A new synthesis process for implementation Euclidean distance calculator is presented. The circuit was designed using FG-MOS transistors that operate in weak inversion. The current-mode approach for this circuit allows it to work at low supply voltage. Beside, as the circuit employs FG-MOS transistors operating in weak inversion region, it features low power consumption with large dynamic range. According to the modular design, it can be extended easily without adjusting any device parameter as the dimension of the vector space increases. The full parallel property of the recognizing system reduces the identification time. With the mentioned merits, the proposed circuit is suitable for real world low power and low supply voltage applications. To demonstrate the function of the proposed method, the circuit was successfully used as the core of a recognition system for template matching. Simulation results demonstrate the functionality of the circuit.

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Ebrahim Farshidi was born in Shoushtar, Iran, in 1973. He received the B.Sc. degree in 1995 from Amirkabir University, Iran, the M.Sc. degree in 1997 from Sharif University, Iran and the Ph. D. degree in 2008 from electrical engineering at IUT, Iran, all in electronic engineering. He worked for Karun Pulp and Paper Company during 1997–2002. From 2002 he has been with shahid chamran university, Ahvaz, where he is currently an assistant professor in the Department of Electrical Engineering. He is author of more than 15 technical papers in electronics. His areas of interest include current-mode circuits design, low power VLSI circuits, and data converters.