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An Ultra-Low Power Variable Gain Current Mirror

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Abstract: A power efficient gain adjustment technique is described to realize programmable gain current mirror. The dissipation power changes over the wide gain range of structure are almost negligible. This property is in fact very interesting from power management perspective, especially in analog designs. The simple structure and constant frequency bandwidth are other ever-interesting merits of proposed structure. The programming gain range of structure is from zero up to 18dB under operating frequency range from 72 kHz to 173 MHz. The maximum power dissipation of designed circuit is only 3.1 µW which is drawn from 0.7 V supply voltage. Simulation results in 0.18 µm CMOS TSMC standard technology demonstrate the high performance of the proposed structure.

Keywords: Variable Gain Current Mirror (VGCM), Constant Frequency Bandwidth, Relocating Pole-Zero.

1 Introduction

DURING the last decades, the rapid growth of portable applications enforced the design of low voltage and low power CMOS circuits. In order to decrease the power consumption, it is crucial to reduce the power supply. Since a low voltage operating circuit becomes necessary, the current mode technique is ideally suited for this purpose [1]. Variable Gain Current Mirrors (VGCMs) are one of the major building blocks for current mode circuit design. VGCMs are required widely in applications such as automatic gain control [2], tuning of continuous time filter [3], and current amplification [4]. The property of tunable gain in current mirrors may also be beneficial to compensate the effects of transistor mismatches and process variations [2, 5-8]. Currently, the research on tunable current mirrors are mainly focused on introducing an efficient method for adjusting the gain, reduction of supply voltage and power consumption, increment of gain tuning range, and operating speed. Up to now, several methods are introduced to change the gain of current mirrors [3, 9-16]. Nevertheless, each work has its own drawbacks. For instance, [10] fails to operate in low voltage, [11] has a limited tuning range, and [3] suffers from low frequency bandwidth. In [9, 13, 14] the level shifters, and in [15] the floating gate transistors are used to achieve the gain tuning function. Also these techniques are promising, however, the presence of level shifters in signal path leads to increased power supply and decreased frequency bandwidth. On the other hand, the floating gate devices are commonly available in double-poly fabrication processes. The power consumption in [12] has been decreased, however, its tuning range and frequency bandwidth are very limited [16] deliver wide tuning range, but it works with a high supply voltage that is not suitable for low voltage and low power applications. In the all of the mentioned circuits, in order to adjust the gain, the operating current or voltages of circuits are varied significantly. However, these kinds of adjusting gain methods are not suitable for high performance applications that require ultra-low power consumption.

In this paper, a very low voltage, low power, zero-pole reposition based VGCM structure is presented which delivers very small power consumption variation in all-over the gain tuning range. The proposed technique enables the structure to deliver some ever interesting features of low power consumption, wide programmable gain range, and acceptable frequency bandwidth. On the other hand, the bandwidth of proposed structure can simply be tuned as well.

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Therefore, the proposed circuit would lend itself for use in applications where the frequency bandwidth tuning is a must. The rest of the paper is organized as follows: Section 2 discusses the proposed structure. The simulation results are presented in Section 3. Finally, Section 4 concludes this work.

2 Proposed Circuit

2.1 Operational Principle

Fig. 1 shows conceptual operation of the proposed technique. The proposed gain adjustment technique well depicted in the bode diagram in Fig. 1. The main idea is to achieve the variable gain function through relocating the poles and zero positions of the circuit, the technique which originally presented at [17-18].

To further understand the operation of the proposed technique, let us explain the idea from Fig. 1. To do so, consider a current mirror with two dominate poles (P_1 and P_2) and one zero (Z_1), so that $Z_1<P_1<P_2$. Suppose that the circuit has a DC current gain of A_0. So, the bode diagram of current transfer function will have the amplitude of A_0 at DC. As the frequency increases, the amplitude of will be A_0 until Z_1 occurs, which causes the amplitude to rise. The amplitude will continue to rising until the first pole, P_1, happens. After, the amplitude will be flat again and remains constant until the second pole, P_2, occurs. This leads the amplitude to start falling until it reaches to zero in infinity. Taking attention to this diagram, one can easily notice that there is a straight relation between the distance of Z_1 and P_1, and the extent that the amplitude will raise until it became flat again. In other word, the distance between Z_1 and P_1 directly determines the amplitude in window between two poles, the desired frequency bandwidth.

In addition to zero-pole repositioning based gain control scheme, the proposed structure also utilizes level shifting method to adjust the gain as well. The combination of level shifting and zero-pole repositioning based gain control methods efficiently helps to extend the gain range of proposed structure.

The final conceptual frequency response of proposed method is depicted in Fig .1. This method gives a variable gain function at midband frequency from P'_1 to P'_2 witch is very interesting in many automatic gain control (AGC) applications and receiver front ends [19]. The 3-dB cutoff frequency at lower corner of frequency bandwidth can simply be changed by varying the value of capacitor C_1, which interestingly need no extra power consumption. The choice of specific application determines the lower corner of frequency bandwidth for VGCM. The presented VGCM, therefore, finds its applications well in multi-standard transceiver structures [20]. The core circuit of proposed VGCM structure is depicted in Fig. 2.

The gain adjustment is simply accomplished by varying the geometry of transistor M_8. This method introduces some negligible variation to the power consumption, while effectively changes the gain.

Thus, the resulted structure promised to be extremely low power. The proposed VGCM structure can interestingly works well with very low power consumption, while delivers high performance with acceptable gain control range. In the following section the transistor level realization of the proposed technique is described.

2.2 Transistor Level Implementation of the Proposed VGCM

The transistor level schematic of a wide-swing low voltage cascade current mirror is presented in Fig .2.

In the proposed CM, the implementation of cascade transistors of M_5-M_6 satisfies the required current transfer accuracy, while the level-shifting transistors of M_1-M_2 decrease the minimum input voltage requirement of structure. Hence, the minimum input and output voltages of proposed current mirror will be decreased down to $2V_{dsat}$. This turns the proposed CM to a preferred choice in low power and low voltage applications. In order to add variable gain capability to the proposed CM, the circuit is modified as the one shown in Fig. 3.

The elements of the proposed circuit are arranged so that appropriately introduces the required zero and poles to the frequency transfer function of the structure. Additionally, selecting an appropriate amount for C_1 can

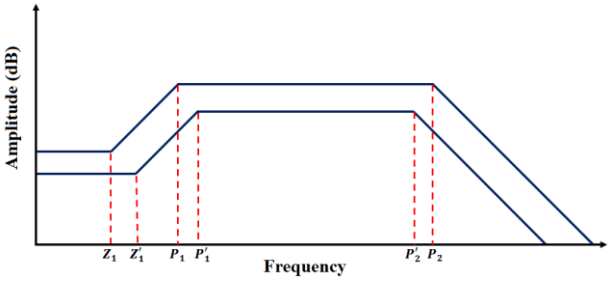

Fig. 1 The conceptual frequency response of VGCM.

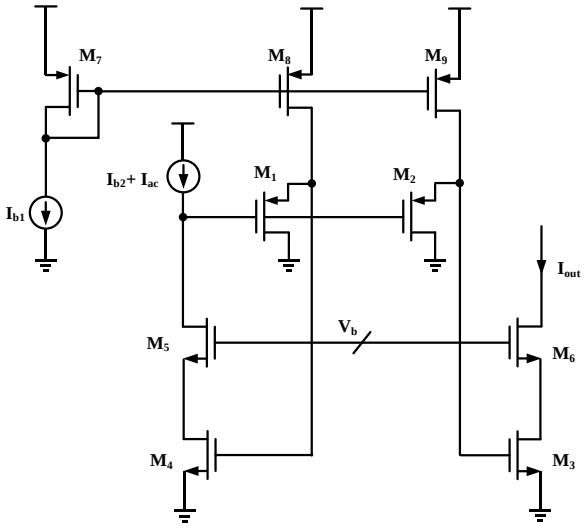

Fig. 2 The schematic of core circuit of VGCM structure.

locate the zero at lower frequencies compared to the poles. The well combination of elements in the structure makes it very simple to adjust the location of zero and pole, and consequently the gain of structure. This can simply be accomplished by changing the effective width of transistor M_8. This, in fact, changes the g_m (trans-conductance) of M_1 and consequently the location of zero and pole in the frequency axis. Changing the effective width of M_8, however has another effect, that is shifting the gate-source voltage of M_3 (and negligibly M_4). This is accomplished through trans-linear loop of M_1-M_4.

These two mechanisms (level shifting and zero-pole repositioning) aide each other to effectively accomplish a wide gain control range.

The width of M_8 can easily programed by changing its dimension through the switching cascade transistors by signals V_1 to V_7. This favorably allows the gain to be adjusted from zero to 18 dB with accepting the variation of only 0.8 µW in power consumption. Another method for achieving tunable gain is deviation of current bias (Ib_1). Although varying Ib_1 is easier process than changing transistor M_8 dimension, this method, however consumes more power than first one during different gain setting. The capacitor C_1 determines the lower 3-dB cutoff frequency locations in the frequency axis. The increment in value of capacitor makes the lower 3-dB cutoff frequency to be shifted to the lower frequencies. This is very interesting as the operating bandwidth can simply be programed to the desired value, addressing the bandwidth requirements for different applications.

3 Simulation Results

The proposed structure is simulated in 0.18 µm standard CMOS technology. In this design C_1 is 2 pF and the width of M_8 varied from 0.4-21 µm. Fig. 4 shows the frequency response of the proposed VGCM at various gain setting. This figure illustrates that by varying the dimension of M_8, the current gain ranges from zero to 18 dB. The 3-dB bandwidth of structure is evaluated to be 173 MHz and interestingly remains well-constant all over the gain range. Beside the gain programing capability, the proposed structure offers the bandwidth programmability as well. This capability is depicted in Fig. 5. The bandwidth programming is routinely accomplished by changing the value of C_1 from 0.2 to 2 pF. Fig. 6 shows the input referred noise current of the proposed VGCM. The input referred noise evaluated to be less than 9.28 pA/√Hz at the gain of 0 dB and operating frequency of 72 kHz, which is the worst cases study. The inset of Fig. 6 shows input referred noise current versus current gain at frequency of 10 MHz.

The Monte-Carlo simulation is done on the threshold voltage of the VGCM in the case of C_1 as 2 pF and width of M_8 is 0.4 µm. The total number of runs was 100 and results are drawn in Fig. 7. This figure illustrates that for the 15 mv deviation of threshold voltage, the variation of gain is rather low. To verify the effectiveness of the new structure over process, voltage, and temperature (PVT) variations, VGCM is simulated in different process corners under different supply voltages and temperatures. The results are summarized in Table 1. It can be seen that the VGCM preserves the performance in the whole studied cases. The comparison between the proposed VGCM and some other published works is reported in Table 2.

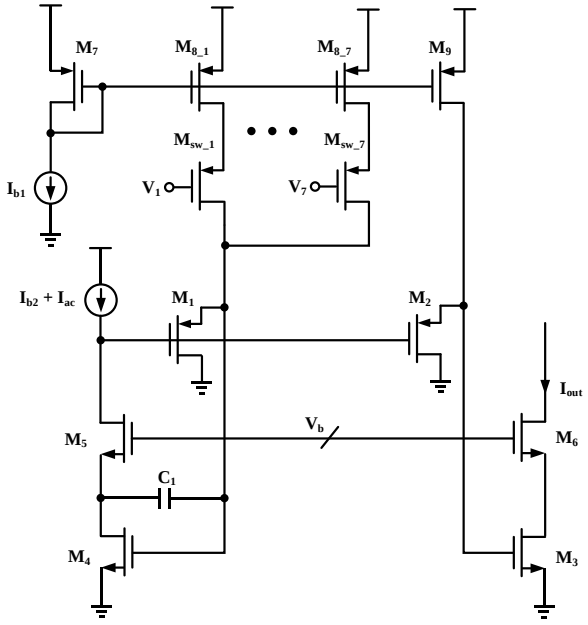

Fig. 3 Schematic of the proposed VGCM.

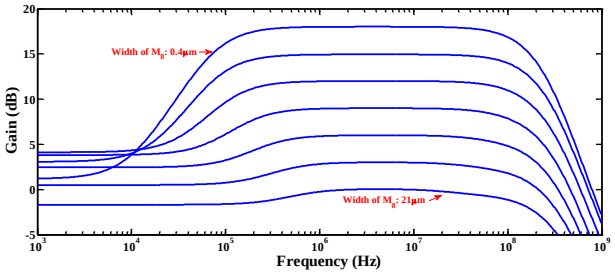

Fig. 4 The frequency response of VGCM at various gain setting.

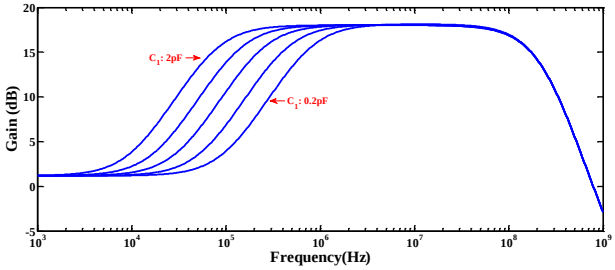

Fig. 5 The frequency response of VGCM at various lower 3-dB cutoff frequencies.

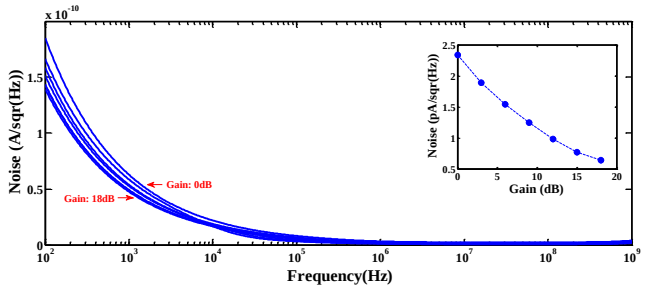

Fig. 6 The input referred noise characteristic of VGCM.

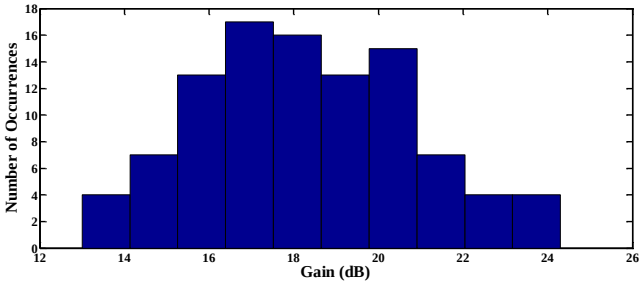

Fig. 7 The results of Monte-Carlo simulation with applying 15 mv variation in threshold voltage.

Table 1 The PVT analysis of the proposed structure.

	tt 27°, 0.7 V	tt 80°, 0.66 V	ss 27°, 0.7 V	ss 100°, 0.65 V	ff 27°, 0.7 V	ff 0°, 0.8 V
Gain [dB]	18	16.6	17.4	15.1	14.2	14

Table 2 Performance Comparison of the proposed structure with some other recent works.

	[a][12]	[16]	[21]	[22]	[23]	This Work
CMOS Process [µm]	0.35	0.18	0.5	0.18	0.18	0.18
Power consumption [µW]	61	900	2.05	41.1	6.9	2.3-3.1
Supply voltage [V]	1.5	1.5	±1.2	1	1.8	0.7
3-dB Bandwidth [MHz]	1.708	100	0.189	93.7	33.6	173
Gain range [dB]	-1.9 to 1.58	0 to 20	0 to 16	-4.3 to 14.9	1.3 to 21	0 to 18
IRN [pA/√Hz]	-	-	-	4.33	1.1	9.28

[a] Measurement Results

4 Conclusion

A new simple method for tuning the gain of current mirror is presented in this work. Beside the low power consumption of the proposed circuit, its other important advantage is its very small power consumption variation at various gain settings. In addition, this new architecture is well suited to work under low voltage supply, helping to further reduce the power consumption. These features make the proposed design to be used in ultra-low-voltage applications. The gain of the current mirror can be simply varied from 0dB to 18dB, while the 3-dB bandwidth of the circuit remains constant around 173 MHz. The maximum power consumption of a proposed VGCM is only 3.1 µW which is drawn from a 0.7 V power supply. Simulation results in 0.18 µm standard CMOS technology, confirm effectiveness of the designed circuit.

References

[1] C. Toumazou, F. J. Lidgey, and D. Haigh, *Analogue IC design: the current-mode approach*, Vol. 2. Presbyterian Publishing Corp, 1990.

[2] M. Siripruchyanun, "A low-voltage, low-power current-mode automatic gain control (AGC) for battery-powered equipment," in *Third IEEE International Workshop on Electronic Design, Test and Applications*, p. 4–pp, 2006.

[3] J. Ramirez-Angulo, C. Durbha, A. J. López-Martín, and R. G. Carvajal, "Highly linear wide tuning range CMOS transconductor operating in moderate inversion," in *IEEE international symposium on circuits and systems (IEEE Cat. No. 04CH37512)*, Vol. 1, p. I–805, 2004.

[4] H. F. A. Hamed and S. Kaya, "Low voltage programmable double-gate MOSFETs current mirror and its application as programmable-gain current amplifier," in *14th IEEE International Conference on Electronics, Circuits and Systems*, pp. 391–394, 2007.

[5] G. Tsirimokou, C. Psychalinos, and A. S. Elwakil, "Digitally programmed fractional-order Chebyshev filters realizations using current-mirrors," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2337–2340, 2015.

[6] M. Altun and H. Kuntman, "Design of a fully differential current mode operational amplifier with improved input–output impedances and its filter applications," *AEU-International Journal of Electronics and Communications*, Vol. 62, No. 3, pp. 239–244, 2008.

[7] M. A. Youssef and A. M. Soliman, "A novel CMOS realization of the differential input balanced output current operational amplifier and its applications," *Analog Integrated Circuits and Signal Processing*, Vol. 44, No. 1, pp. 37-53, 2005.

[8] C. Laoudias and C. Psychalinos, "Applications of current mirrors in analog signal processing," *Physics Department, Electronics Laboratory, University of Patras, Rio Patras, Greece*.2012.

[9] A. K. Gupta, J. W. Haslett, and F. N. Trofimenkoff, "A wide dynamic range continuously adjustable CMOS current mirror," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 8, pp. 1208–1213, 1996.

[10] J. Ramirez-Angulo, S. R. S. Garimella, A. J. Lopez-Martin, and R. G. Carvajal, "Gain programmable current mirrors based on current steering," *Electronics Letters*, Vol. 42, No. 10, pp. 559–560, 2006.

[11] M. Tikyani and R. Pandey, "A new low-voltage current mirror circuit with enhanced bandwidth," in *International Conference on Computational Intelligence and Communication Networks*, pp. 42–46, 2011.

[12] C. Laoudias and C. Psychalinos, "Low-voltage CMOS adjustable current mirror," *Electronics Letters*, Vol. 46, No. 2, pp. 124–126, 2010.

[13] A. Zeki and A. Toker, "Tunable linear CMOS current mirror," *Analog Integrated Circuits and Signal Processing*, Vol. 50, No. 3, pp. 261–269, 2007.

[14] W. Surakampontorn and K. Kumwachara, "CMOS-based electronically tunable current conveyor," *Electronics Letters*, Vol. 28, No. 14, pp. 1316–1317, 1992.

[15] S. A. Jackson, J. C. Killens, and B. J. Blalock, "A programmable current mirror for analog trimming using single poly floating-gate devices in standard CMOS technology," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, Vol. 48, No. 1, pp. 100–102, 2001.

[16] B. Sedighi and M. S. Bakhtiar, "Variable gain current mirror for high-speed applications," *IEICE Electron. Express*, Vol. 4, No. 8, pp. 277–281, 2007.

[17] H. F. Baghtash and A. Ayatollahi, "A zero-pole reposition based, 0.95-mW, 68-dB, linear-in-dB, constant-bandwidth variable gain amplifier," *Circuits, Systems, and Signal Processing*, Vol. 33, No. 5, pp. 1353–1368, 2014.

[18] H. F. Baghtash, "A 0.74 mW, linear-in-dB, constant bandwidth, variable gain amplifier based on zero-pole repositioning technique," *Analog Integrated Circuits and Signal Processing*, Vol. 84, No. 2, pp. 303–313, 2015.

[19] E. Sobotta, R. Wolf, N. Joram, and F. Ellinger, "RF variable gain amplifier with linear control and automatic matching in 28 nm CMOS," in *IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems*, pp. 1–5, 2015.

[20] K. Bao, X. Fan, L. Tang, Z. Hua, and Z. Wang, "A programmable gain amplifier for multi-mode multi-standard wireless receivers," in *12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, pp. 1–3, 2014.

[21] M. Kumngern, F. Khateb, and T. Kulej, "A digitally programmable gain amplifier for ultra-low-power applications," *Analog Integrated Circuits and Signal Processing*, Vol. 85, No. 3, pp. 433–443, 2015.

[22] H. F. Baghtash, "Body controlled threshold voltage shifting variable gain current mirror," *Analog Integrated Circuits and Signal Processing*, Vol. 93, No. 1, pp. 115–121, 2017.

[23] T. Azadmousavi, H. F. Baghtash, and E. N. Aghdam, "A Power Efficient Gain Enhancing Technique for Current Mirror," *Iranian Journal of Electrical and Electronic Engineering*, Vol. 14, No. 2, pp. 137–142, 2018.

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