Hybrid Series & Shunt Active DC Line Conditioner

S. M. Dehghan*, A. Yazdian* and M. Mohamadian*

Abstract: In this paper a hybrid active DC line conditioner for fluctuations and ripples reduction in voltage and current of DC power systems is proposed. Malfunctions in operation of equipments and systems which are supplied by low quality distribution power systems are one of the main effects of DC voltage ripple. In the proposed configuration a hybrid system including series and shunt active line conditioners for ripple reduction of load voltage and source current is used. Simulation and experimental results are provided to show the performance of the proposed configuration in different states.

Keywords: Active Noise Cancellation, Active Power Line Conditioner, DC Voltage.

1 Introduction

DC power systems used in communication and traction systems, are increasingly used in offices, commercial facilities, factories and homes due to growing number of electronic equipments. Ripples and fluctuations of voltage or current in DC power system could cause errors in operation of electronic and electric equipment. Using passive power filters could partially reduce ripples, but with a slow dynamic response [1, 2].

Recently, active power filters have been proposed for ripple reduction in magnet power supplies and high voltage direct current (HVDC) station [2-7].

In this paper a configuration of series and shunt active line conditioners is used to reduce the voltage ripple of DC power networks using a hybrid power line conditioner (HPLC). Figure 1 shows the structure of this system, where series and parallel active power line conditioners are used simultaneity to reduce fluctuations of load voltage and source current. Similar configurations are used in AC systems previously.

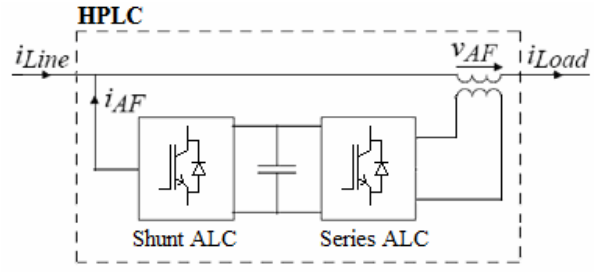

Fig. 1 Structure of hybrid power line conditioner.

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Using digital control techniques such as model reference controller, repetitive controller and deadbeat controller, reliability and functionality of this configuration is enhanced.

The paper is organized as follows. Section 2 describes ripple reduction of load voltage using HPLC and its modeling and the control techniques. Ripple reduction of source current using HPLC is described in Section 3. Sections 4 and 5 present simulation and experimental results.

2 Load Voltage Compensation

The basic concept used in the used configuration is to insert a voltage source in series with the load which has 180 degrees phase shift regard to the voltage ripple.

This can be done using a series active line conditioner that is shown in Fig. 2. This system includes a voltage source inverter, an LC filter and a transformer with the ratio of N. In this figure V_{DC} is DC voltage of bus and V_r indicates ripple voltage. The goal is to inject V_{AF} into DC bus, such that the load voltage is almost constant DC voltage.

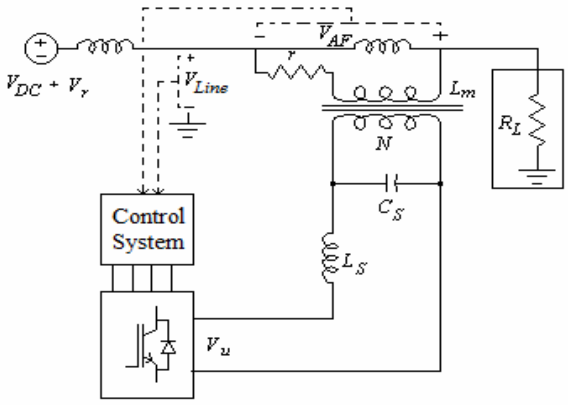

Fig. 2 Series active line conditioner to reduce the ripple of load voltage.

To compensate undesired components of load voltage, first source voltage is sampled and then passed through a high pass filter to produce reference voltage which can be used as reference for series inverter. This is implemented with the help of a special coupling transformer described in the following section.

2.1 Series Compensation

The secondary of the coupling transformer is connected in series with DC bus. Whether the HPLC works or not, the current of load always passes through the transformer. Thus the main load current (DC current) causes the transformer core to be biased or even saturated [7]. To reduce the magnetic bias, a bypass inductor in parallel with the high frequency transformer is used as illustrated in Fig. 2. In this approach, the bypass inductor, which is implemented with a gapped core, serves as the DC bypass element. The high frequency transformer is implemented to inject compensating voltage. The winding resistance of inductor must be smaller than winding resistance of transformer so that DC current doesn't pass through the transformer. A small resistance, r, is used in series with transformer to guarantee a high impedance pass for DC current.

2.2 Series Compensation Model

Neglecting the leakage inductance of transformer and with following assumptions for the series resistance, r, and L_m and L_s inductors

$$r << (L_m 2\pi f_{min} \,||\, R_L) \tag{1}$$

$$L_m << L_T \tag{2}$$

$$L_S << N^2 L_m \tag{3}$$

and referring to Fig. 2, the transfer function of transformer secondary voltage can be given by

$$V_{AF}(s) = \frac{1/N}{L_S C_S S^2 + \left(L_S / N^2 R_L\right) S + 1} V_u(s) + \frac{Z_m}{Z_m + R_L} V_r(s) \tag{4}$$

where

$$Z_m(s) = \frac{L_S S / N^2}{L_S C_S S^2 + 1} + r \tag{5}$$

and V_u is inverter output voltage and f_{min} is defined as smallest frequency component of the voltage ripple.
In Fig. 3, the ac model of series active line conditioner is shown and it can be seen that the secondary voltage of transformer depends on voltage ripple (V_r) as well as inverter voltage.

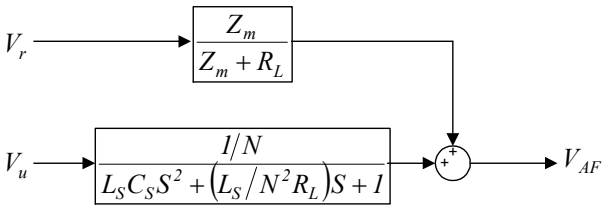

Fig. 3 The ac model of series active line conditioner.

Since $Z_m << R_L$ so V_r doesn't have that much effect on V_{AF} and therefore it can be eliminated from the model.

2.3 Discrete Model of Series Active Line Conditioner

In order to design a digital controller, the discrete model of series active line conditioner must first be identified. In the first step, the discrete model of PWM inviter must be obtained.
Figure 4 shows the circuit diagram of a series active line conditioner in a DC network. Continuous state equations of series active line conditioner are

$$\begin{aligned} \dot{x_c}(t) &= A x_c(t) + B V_u(t) \\ y(t) &= C x_c(t) + D V_u(t) \end{aligned} \tag{6}$$

where

$$\begin{aligned} x_c(t) &= \begin{bmatrix} v_c(t) \\ \dot{v_c}(t) \end{bmatrix} \\ A &= \begin{bmatrix} 0 & 1 \\ -\omega_p^2 & -2\zeta_p \omega_p \end{bmatrix} \\ B &= \begin{bmatrix} 0 \\ \omega_p^2 \end{bmatrix} \\ C &= \begin{bmatrix} 1/N & 0 \end{bmatrix} \\ D &= \begin{bmatrix} 0 & 0 \end{bmatrix} \end{aligned} \tag{7}$$

where ζ_υ, ω_υ are damping ratio and natural frequency of inverter which are defined as follows:

$$\omega_p = \frac{1}{\sqrt{L_S C_S}} \tag{8}$$

$$\zeta_p = \frac{1}{2N^2 R_L} \sqrt{\frac{L_S}{C_S}} \tag{9}$$

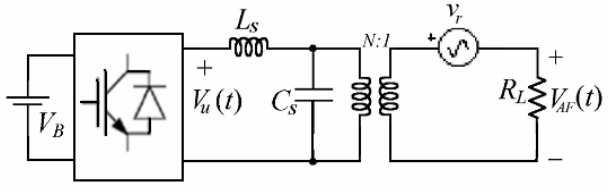

Fig. 4 Series active line conditioner diagram.

V_u is a pulse voltage source with a magnitude of (V_B, 0, $-V_B$). If sinusoidal pulse width modulation (SPWM) is used for switching of inverter, the power switches are turned on and off two times during each sampling period T so that V_u has a magnitude of $+V_B$ or $-V_B$, and width $\Delta T(k)/2$. Therefore, the discrete state equation is

$$\begin{aligned} X(k+1) &= e^{AT}X(k) \\ &+\int_{(T-\Delta T)/4}^{(T+\Delta T)/4} e^{A(T-\tau)}BV_B d\tau \\ &+\int_{(3T-\Delta T)/4}^{(3T+\Delta T)/4} e^{A(T-\tau)}BV_B d\tau \end{aligned} \quad (10)$$

If the switching frequency be n_p times sampling frequency, the state equation is:

$$\begin{aligned} X(k+1) &= e^{AT}X(k) \\ &+\int_{(T-\Delta T(k))/4n_p}^{(T+\Delta T(k))/4n_p} e^{A(T-\tau)}BV_B d\tau \\ &+\int_{T/2n_p+(T-\Delta T(k))/4n_p}^{T/2n_p+(T+\Delta T(k))/4n_p} e^{A(T-\tau)}BV_B d\tau \\ &+\ldots+\int_{(2n_p-1)T/2n_p+(T-\Delta T(k))/4n_p}^{(2n_p-1)T/2n_p+(T+\Delta T(k))/4n_p} e^{A(T-\tau)}BV_B d\tau \end{aligned} \quad (11)$$

The higher order term ΔT^2 is neglected in the series expansion because ΔT is smaller in magnitude than T. Therefore discrete state equation is simplified as follows:

$$X(k+1) = e^{AT}X(k) + \frac{1}{2n_p}\left(\sum_{i=0}^{2n_p-1} e^{\frac{4n_p-1-2i}{4n_p}AT}\right)BV_B\Delta T(k) \quad (12)$$

or in matrix form:

$$X(k+1) = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} X(k) + \begin{bmatrix} h_1 \\ h_2 \end{bmatrix} \Delta T(k) \quad (13)$$

where

$$\begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} = e^{AT} \quad (14)$$

$$\begin{bmatrix} h_1 \\ h_2 \end{bmatrix} = \frac{1}{2n_p}\left(\sum_{i=0}^{2n_p-1} e^{\frac{4n_p-1-2i}{4n_p}AT}\right)BV_B \quad (15)$$

From Eq. (13), the discrete transfer function of series active line conditioner output in the z-domain is obtained

$$V_{AF}(z) = \frac{b_1 z + b_2}{z^2 + a_1 z + a_2} V_u(z) \quad (16)$$

where the input variable and the gains of the equation are:

$$V_u(k) = \frac{\Delta T(k)}{T} \quad (17)$$

$$\begin{aligned} b_1 &= h_1 T / N \\ b_2 &= (h_2 g_{12} - h_1 g_{22})T / N \end{aligned} \quad (18)$$

$$\begin{aligned} a_1 &= -(g_{11} + g_{22}) \\ a_2 &= g_{11}g_{22} - g_{12}g_{21} \end{aligned} \quad (19)$$

Equation (16) is the discrete transfer function of series active line conditioner that is used to design the digital controller.

2.4 Voltage Control

Figure 5 shows the control system of series active line conditioner that includes two controllers, reference model controller and repetitive controller. In this way, the control law $V_u(n)$ is

$$V_u(n) = V_{uMRC}(n) + V_{uRP}(n) \quad (20)$$

where V_{uMRC} and V_{uRP} are MRC output and repetitive controller output respectively.

The objective of the MRC is to modify the structure of the plant so that its input-output properties are the same as reference model, which describes the desired input-output properties of the closed-loop system [8]. The parameters of the reference model can be chosen to improve the dynamic response or to increase stability margin of the closed-loop system. Therefore, a reference model is chosen as:

$$W_m(s) = \frac{W_{Zm}(s)}{W_{Rm}(s)} = \frac{\omega_m^2}{S^2 + 2\zeta_m\omega_m S + \omega_m^2} \quad (21)$$

where ζ_m and ω_m are damping ratio and natural frequency of the reference model. Discrete transfer function of reference model can be obtained using a zero-order-hold method [9].

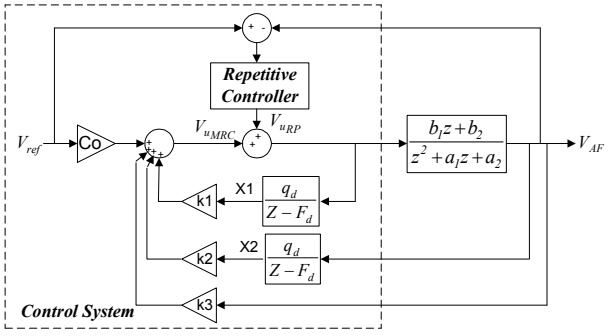

Fig. 5 Control system of series active line conditioner.

$$W_m(z) = \frac{c_1 z + c_2}{z^2 + d_1 z + d_2} \quad (22)$$

In Fig. 5, the control law of MRC is defined as [10]:

$$V_{uMRC}(n) = K^T X(n) + c_o V_{ref}(n) \quad (23)$$

where V_{ref} is the reference voltage which can be obtained by passing source voltage through a high-pass filter. c_o is a scalar feed forward parameter and $K^T = [k_1 k_2 k_3]$ is the control vector. The state variables vector, X, is defined as:

$$X^T = \begin{bmatrix} x_1 & x_2 & V_{AF} \end{bmatrix} \quad (24)$$

where x_1 and x_2 are the auxiliary variables and are obtained as follow:

$$x_1(n+1) = F_d x_1(n) + q_d V_u(n) \quad (25)$$

$$x_2(n+1) = F_d x_2(n) + q_d V_{AF}(n) \quad (26)$$

where (F_d, q_d) is a controllable pair.

$$(Z - F_d)^{-1} q_d = \frac{\alpha(Z)}{\Lambda(Z)} \quad (27)$$

and

$$\alpha(z) = \begin{bmatrix} Z^{m-2} & Z^{m-1} & \dots & Z, 1 \end{bmatrix}^T \qquad m \geq 2 \quad (28)$$

$$\Lambda(s) = \Lambda_o(s) W_{Zm}(z) = Z^{m-1} + \lambda_{m-2} Z^{m-2} + \dots + \lambda_1 Z + \lambda_o \quad (29)$$

Parameter m is the order of the system to be controlled. In the proposed series active line conditioner, m=2. Thus from Eq. (27)

$$(z - F_d)^{-1} q_d = \frac{1}{z + \lambda_o} \quad (30)$$

$$F_d = e^{-\lambda_o T} \quad (31)$$

$$q_d = (1 - e^{-\lambda_o T}) \frac{1}{\lambda_o} \quad (32)$$

The transfer function of closed-loop system including series active line conditioner and the MRC is

$$G_{MRC}(z) = \frac{c_o (z - F_d)(b_1 z + b_2)}{Gr}$$
$$Gr = (z^2 + a_1 z + a_2)(z - F_d - k_1 q_d) - (k_3 (z - F_d) + k_2 q_d)(b_1 z + b_2) \quad (33)$$

$[k_1 k_2 k_3]$ must be chosen such that with canceling the zeros and the poles in closed-loop transfer function, the transfer function will be equal to the reference model.
It is not always possible to choose a vector control, $[k_1 k_2 k_3]$, with exact match between the closed-loop transfer function and the reference model. This vector can be optimally obtained from simulation of the discrete MRC using an adaptation algorithm, such as least mean squares (LMS) algorithm [11].

$$e(n) = V_{AF_m}(n) - V_{AF}(n) \quad (34)$$

where V_{AFm} is output of reference model and e is error. Thus

$$K(n+1) = K(n) - \mu \nabla_a (E[e(n)^2]) \quad (35)$$

where $E[e(n)^2]$ is mean square error. ∇_a and μ are the indicators respectively for gradient and step-size. Using LMS algorithm will simplify the above equation [8].

$$K(n+1) = K(n) - 2\mu e(n) \frac{\partial e(n)}{\partial K} \quad (36)$$

$$K(n+1) = K(n) - 2\mu e(n) \begin{bmatrix} 1 & a_1 & a_2 \\ 0 & b_1 & b_2 \\ -b_1 & b_1 F_d - b_2 & b_2 F_d \end{bmatrix} \begin{bmatrix} V_{AF}(n-1) \\ V_{AF}(n-2) \\ V_{AF}(n-3) \end{bmatrix} \quad (37)$$

Although the closed-loop system with MRC can have satisfactory dynamic response and stability margin, however the feedback system usually presents a high THD for nonlinear cyclic loads [9]. Consequently, a repetitive controller is added to the control system. The repetitive control law can be written as:

$$V_{uRP} = c_r e_r(n + M - l) + Q_r V_{uRP}(n - l) \quad (38)$$

$$e_r(n) = V_{ref}(n) - V_{AF}(n) \quad (39)$$

where c_r is the repetitive controller gain, M is the time advance step size, l is the number of samples in a reference signal period, and Q_r is a constant. Q_r can be equal or smaller than unit, witch is used to improve the robustness of the closed-loop system.

3 Source Current Ripple Reduction

If the load is a source of harmonic current, this current through bus resistance can produce a voltage ripple. Therefore the ripple of source current must be reduced.

In this paper, injecting inverse ripple current into bus using a parallel active line conidintioner is proposed as shown in Fig. 6 where, V_{line}, V_{DC} and V_r are line voltage, DC part of voltage and voltage ripple respectively. As shown in Fig. 6, the load current is sampled and then passed through a high-pass filter to obtain the reference current.

3.1 Shunt Active Line Conditioner

In this system, inverter current, i_{af}, is calculated using

$$i_{af}(s) = \frac{V_{line}(s) - V_{av}(s)}{L_a S + 1/C_a S} \tag{40}$$

where V_{line} is line voltage, V_{av} is inverter output voltage and L_a is smoothing inductor. A series capacitor, C_a, is used to prevent DC current from passing through inverter. The C_a capacitance must be chosen such that its impedance to ripple frequency be negligible compared to the smoothing inductor impedance.

$$L_a S >> \frac{1}{C_a S} \tag{41}$$

$$C_a >> \frac{1}{L_a (2\pi f_{min})^2} \tag{42}$$

f_{min} is defined as the smallest ripple frequency of current or voltage. With above assumptions, equation (40) can be simplified as follow:

$$i_{af}(s) = \frac{V_r(s) - V_{av}(s)}{L_a S} \tag{43}$$

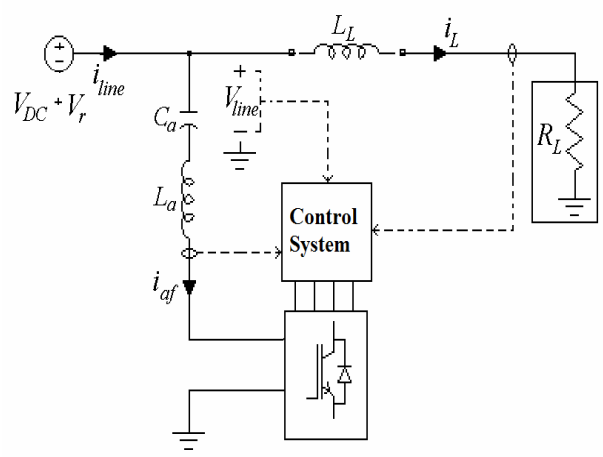

Fig. 6 Structure of parallel active line conidintioner.

where V_r is voltage ripple that is obtained from the output a high-pass filter with line voltage as input.

$$V_r(s) = V_{line}(s) - V_{DC}(s) \tag{44}$$

The discrete form of equation (43) is presented as: [12]

$$i_{af}(n+1) = \frac{T}{L_a}(V_{av}(n) - V_r(n)) + i_{af}(n) \tag{45}$$

where T is the sampling period. Figure 7 shows the z-domain model of parallel active line conidintioner. Regarding delay time for computations, a unit lag transfer function z^{-1} is added as part of the system model [13].

3.2 Current Control

Figure 8 shows the block diagram of parallel active line conidintioner with its control system. Control function H_i and H_v should be calculated such that inverter current follows reference current.

The Closed-loop transfer function of inverter current is

$$\begin{aligned} i_{af} = & \frac{(T/L_a)H_i(z)}{Z^2 - Z + (T/L_a)H_i(z)} i_{ref}(z) \\ & - \frac{(T/L_a)(H_v(z) - Z)}{Z^2 - Z + (T/L_a)H_i(z)} V_r(z) \end{aligned} \tag{46}$$

To achieve an ideal reference current tracking, the reference-output transfer function must be unity, while ripple-output transfer function should be zero. Thus

$$H_{i_{ideal}}(z) = (L_a/T)(Z^2 - Z) \tag{47}$$

$$H_{v_{ideal}}(z) = Z \tag{48}$$

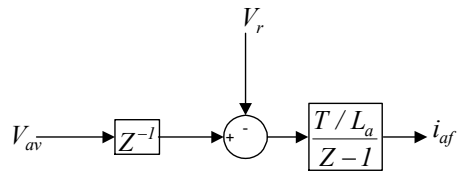

Fig. 7 Discrete model of parallel active line conidintioner.

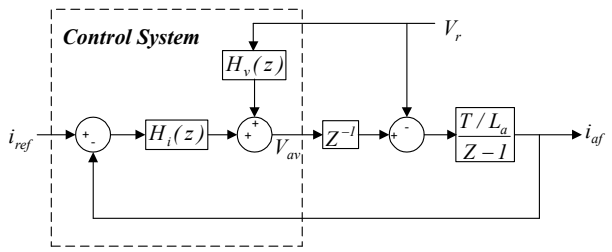

Fig. 8 Current control system of HPLC.

However, the realization of above control functions is not feasible due to the order of numerators which are higher than the order of the respective denominators. Therefore they must be modified and approximated.
To make H_v causal, the value of V_r in the next sampling point is predicated from its past and present values using extrapolation technique. A linear extrapolation used for this purpose yields [14]:

$$V_r(n+1) \approx 2V_r(n) - V_r(n-1) \tag{49}$$

Thus transfer function H_v given by

$$H_v(z) = \frac{2Z-1}{Z} \tag{50}$$

To generate a proper transfer function for H_i with a deadbeat response, reference-output transfer function is defined as follow:

$$\frac{i_{af}(z)}{i_{ref}(z)} = Z^{-2} \tag{51}$$

Thus transfer function H_i will be

$$H_i(z) = \frac{(L_a/T)Z}{Z+1} \tag{52}$$

Regarding the term Z^{-2} in equation (51), the inverter current follows reference current with delay time of 2T:

$$i_{af}(n) = i_{ref}(n-2) \tag{53}$$

To solve this problem, reference current can be predicated using a linear extrapolation method:

$$\begin{aligned} &i_{ref}(n+2) = \\ &2i_{ref}(n+1) - i_{ref}(n) = \\ &3i_{ref}(n) - 2i_{ref}(n-1) \end{aligned} \tag{54}$$

Therefore reference current should be multiplied by the following transfer function:

$$H_r(z) = \frac{3Z-2}{Z} \tag{55}$$

Figure 9 shows the block diagram of current control system.

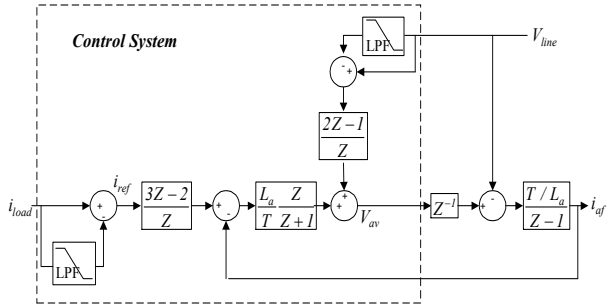

Fig. 9 Current control system for the parallel active line conidintioner.

Table 1 Simulation parameters of HPLC.

Element	Value
Ls	1 mH
Cs	25 uF
RL	102 ohm
VS	63 V
Fs	10050 Hz
K1	-13.75
K2	14.32
K3	0
Qd	0.0085
Fd	0.7189
Co	1
Cr	0.1
Lp	1 mH
Cp	2000 uF
Cdc	1000uF
La	51 mH
Ca	5000 uF
t	0-0.5 S

4 Simulations

The proposed configuration in this paper is simulated. Series and parallel active line conidintioners are used to reduce ripple of load voltage and source current respectively. Since 48V DC bus is typically used as a telecommunication industry standard, a three-phase voltage source and rectifier is chosen to produce 48V DC. To emphasis the problem of ripple, a half-wave rectifier is used. The DC bus load is a resistive load plus an inverter with RLC load in its ac side which produces harmonic current in DC bus. Table 1 shows simulation parameters.
For measuring voltage fluctuations and comparing simulation results, the ripple factor (RF) is defined as follow [15]:

$$RF = \frac{V_{AC}}{V_{DC}} = \frac{\sqrt{\sum_{i=1}^{n} V_i^2}}{V_{DC}} * 100\% \tag{56}$$

where, V_{AC} is the ripple voltage peak value. The model has been simulated for 25 cycles of input ac side voltage supply. In t=0.2S, series active line conidintioners and in t=0.35S, parallel active line conidintioners is activated. Figure 10 shows load voltage and Fig. 11 and Fig. 12 show the spectra of load voltage, respectively before and after series active line conidintioners is activated. It is seen that ripple factor is reduced from 19 percent to 0.75 percent.

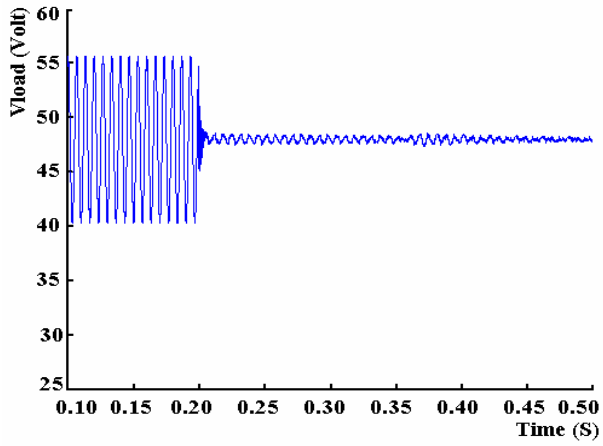

Fig. 10 The load voltage (Reduced ripple using HPLC).

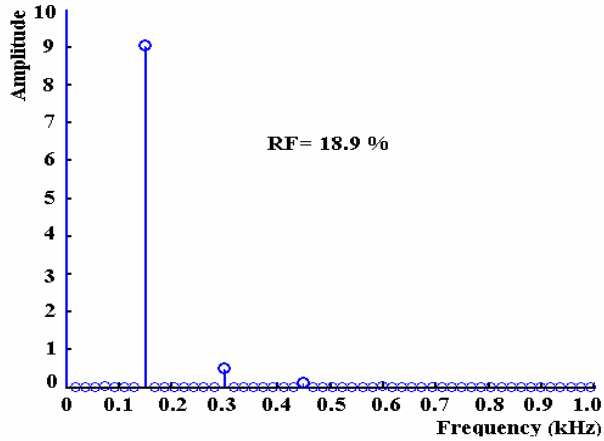

Fig. 11 The spectra of load voltage (Before operate HPLC).

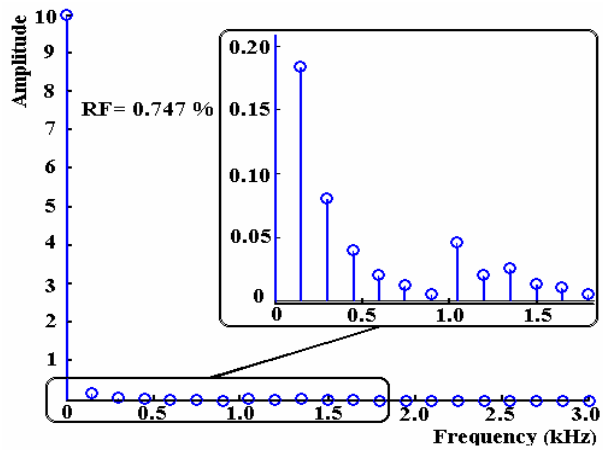

Fig. 12 The spectra of load voltage (After operate HPLC).

Figure 13 shows the source current waveform. It is seen that with series active line conidintioners in circuit, only partial compensation of current ripple has happened. The major part of current ripple is due to nonlinear parallel load, which is cancelled out after activation of parallel active line conidintioners. In Fig. 14 and Fig. 15 the spectra of source current, before and after HPLC activation is shown respectively. It is seen that ripple factor is reduced from 31% to 3.1%.

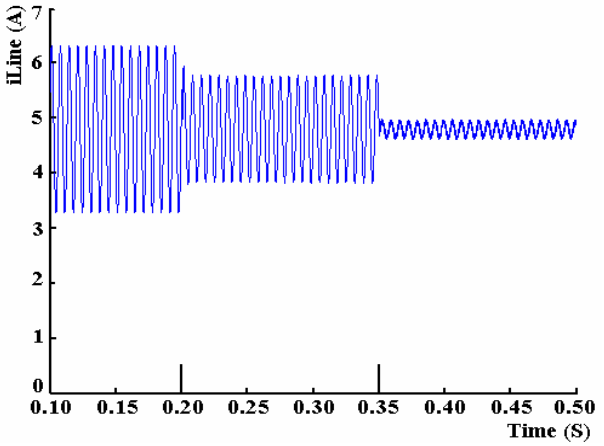

Fig. 13 The source current (Reduced ripple using HPLC).

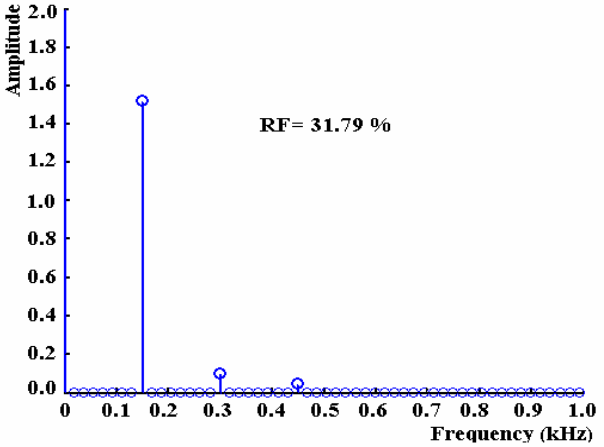

Fig. 14 The spectra of source current (Before operate HPLC).

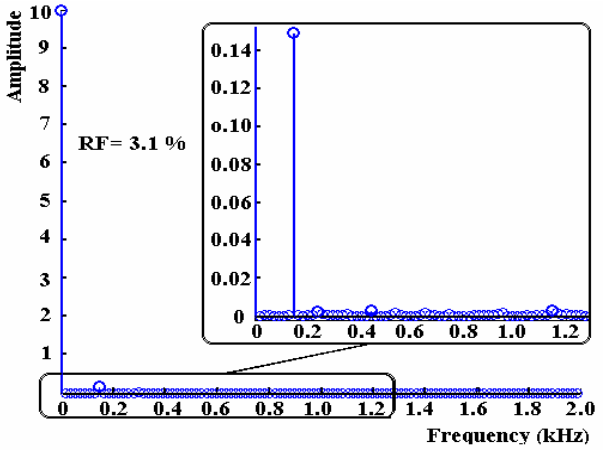

Fig. 15 The spectra of source current (After operate HPLC).

Figure 16 shows ripple factor of load voltage versus load current. As seen in this figure, the HPLC has better performance in heavy load.
Also, dynamic response of proposed system is examined with a step change in load. In this simulation value of load is changed from 5 ohm to 4.2Ω in t=0.2Sec (equivalent to a change in average DC current from 9.6 to 11.7 A). In Fig. 17, it is shown that the HPLC response time is 0.02S (Approximately three cycles of current ripple).

5 Experimental Results

A laboratory prototype of HPLC has been designed and implemented for a 48V DC bus and 5A load. A digital central controller processor (DCCP) including a PC and a data acquisition card is used to control active line conidintioner. Figure 18 shows the block diagram of implemented prototype. Table 2 shows features of implemented prototype.

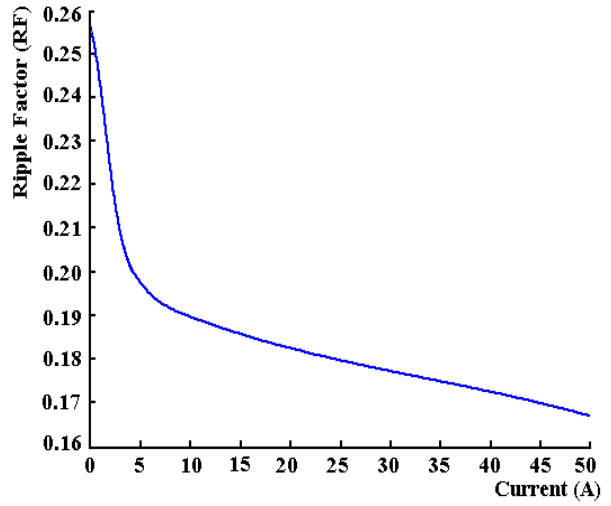

Fig. 16 The ripple factor of load voltage versus load current.

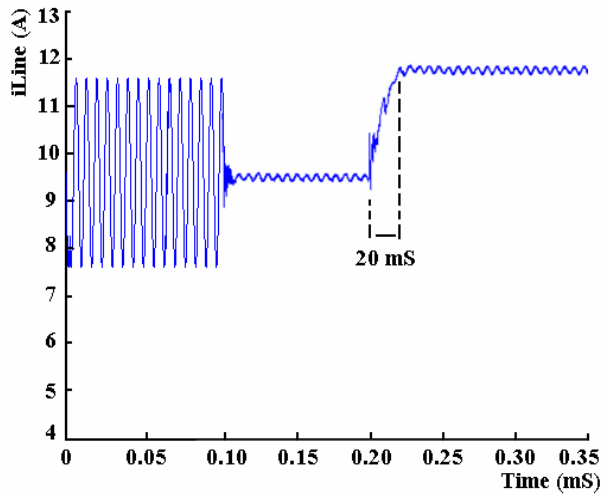

Fig. 17 The source current with varying load.

Figure 19 shows source voltage and load voltage waveform. As it can been seen, the active line conidintioner has reduced ripple voltage to a desirable level. The spectra of source and load voltage waveforms are shown in Fig. 20 and Fig. 21. It is seen that ripple factor is reduced from 5.5% to less than one percent. Figure 21 shows that in spite of the reduction of low frequency components magnitude, because of switching frequency, the high frequency components magnitude increases.

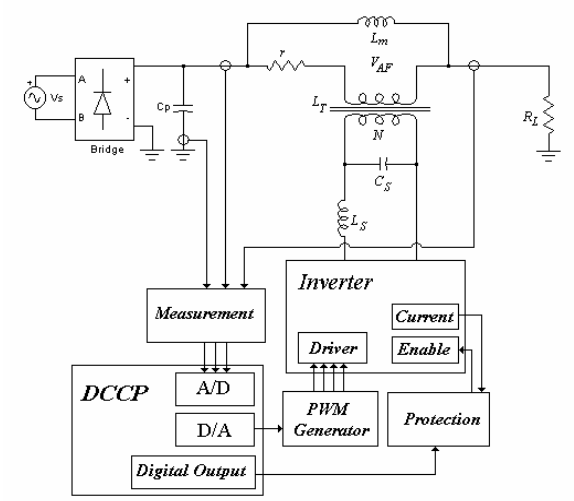

Fig. 18 Block diagram of experimental HPLC setup.

Table 2 Features of implemented prototype.

Element	Value
Rate of Power	250 W
Ls	1 mH
Cs	22 uF
Lm	1 mH
Transformer	25/5 Volt
RL	10 ohm
VS	16 V
Sampling Frequency	12800 Hz
Switching Frequency	12800 Hz
PC	Intel P3
Data Acquisition Card	Advantech PCI1716

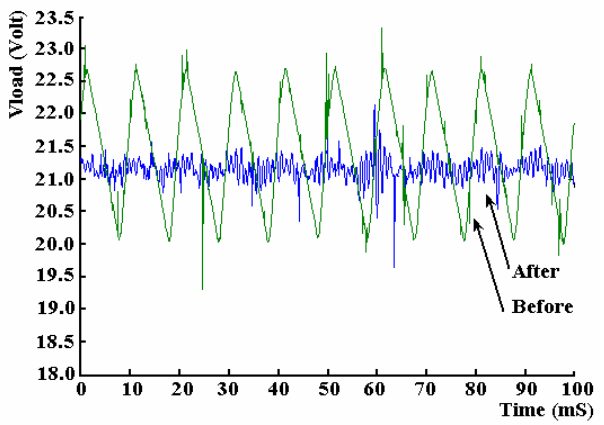

Fig. 19 Load voltage and source voltage profiles.

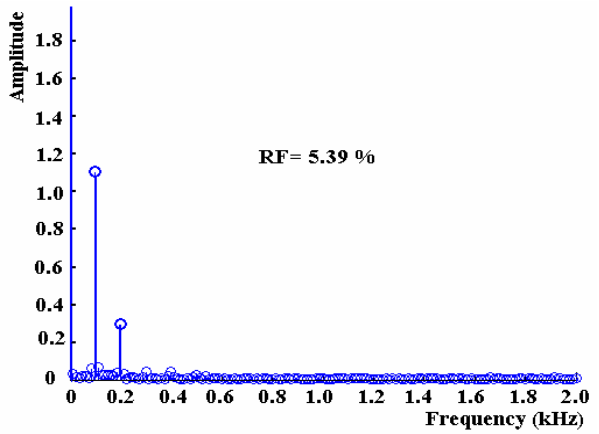

Fig. 20 The spectra of source voltage

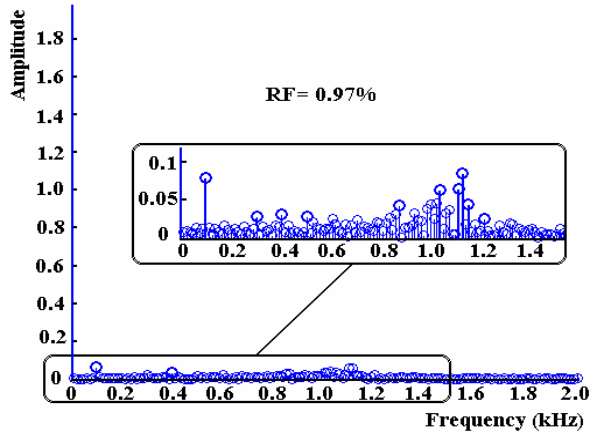

Fig. 21 The spectra of load voltage.

6 Conclusions

In this paper, a hybrid system including series and parallel active line conidintioners is used to reduce voltage ripple in DC power systems. Advanced digital control techniques are used to control PWM voltage source inverters. The simulation results show the performance of the proposed configuration in terms of ripple reduction. It reduces the ripple factor (RF) of load voltage and source current to less than one and five percent respectively. A laboratory prototype of proposed system has been implemented. The experimental results show that HPLC has reduced RF of load voltage to less than one percent as expected through simulation results.

Acknowledgments

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