A Novel Active Feedback Frequency Compensation Scheme for Two-Stage OTA

H. Faraji Baghtash* (C.A.) and Kh. Monfaredi**

Abstract: A novel active feedback frequency compensation scheme is presented in this work. Based on the proposed technique, an amplifier with two main poles in its frequency bandwidth can be easily compensated by introducing a pole-zero pair in a local feedback. The proposed method is mathematically analyzed and then based on the derived formulations, a design procedure is established. The capability of the proposed technique is examined considering a well-known two-stage amplifier, considering just a trivial modification on its input stage. To gain an analogous and fair insight, the performance of the proposed structure is compared with that of the optimally designed miller-compensated two-stage amplifier. The post-layout simulations are accomplished with TSMC 180nm CMOS standard technology. The Spectre post-layout simulations show that the proposed structure outperforms the traditional structure in terms of power consumption and gain bandwidth product. The robustness of the design is checked with Monte Carlo simulations.

Keywords: Low Voltage, Low Power, Frequency Compensation, Operational Amplifier.

1 Introduction

O PERATIONAL trans-conductance amplifier (OTA), is essentially one of the most common and widely used blocks in analog signal processing [1-4]. Beside its vast usage in application requiring signal amplification, they have been also known as versatile blocks, finding widespread applications in many structures such as voltage followers, current-to-voltage converters, active rectifiers, integrators, and various types of filters. Among other specifications of the OTA blocks, the DC-gain and operating frequency bandwidth are considered as the two most important parameters that normally required to be maximized during the design procedure. Unfortunately, there is a severe tradeoff between these two parameters, which means that improving one of these parameters will strictly degrade the other one. Cascoding and cascading of the amplifier blocks are two most common approaches for boosting the overall gain. Due to the supply voltage scaling imposed by nowadays technology downscaling, the performance improvement expected by cascoding is essentially diminished, while the cascading gains more attention than ever. Unfortunately, cascading degrades the stability of the overall amplifier. Hence, the two cascaded stages are typically preferred to maintain the desirable stability. Even with two cascaded stages, the overall amplifier is usually prone to be unstable when used in feedback configurations. Hence the frequency compensation is usually required for two stage OTAs.

So far, several frequency compensation techniques have been proposed for two-stage amplifiers, all of which are variants of well-known Miller compensation scheme [5]. In this scheme, a Miller capacitance is usually inserted between input and output nodes of the second stage (gain stage) [6-9]. This moves the poles of amplifier in opposite directions along the frequency axis, and hence by decreasing the frequency of dominant pole and increasing the frequency of non-dominant pole, improves the amplifier stability. The pure Miller compensation technique, however, produces a right half-plane zero. Different variants of Miller compensation scheme have somehow tried to either
淘汰这个右半平面上的零点或将其转换到一个左半平面上。例如，如果在反馈器中添加一个零点，使得它可能有效删除右半平面上的零点或将其转换到一个左半平面上[10, 11]。一些其他变种的米勒补偿方法已被提出，用于实现电压跟随器[12-14]，电流跟随器[12, 13, 15, 16]，电流放大器[15]，或者电流镜[17, 18]在反馈或前馈路径。

米勒的方案是证明的有效补偿技术。尽管其理论和设计方法已被广泛接受，且可容易地用于补偿任何两级放大器，但它也有一些缺点，比如服务器。例如，米勒电容会降低增益带宽乘积。这样做会降低增益带宽乘积的速率并破坏PSRR的放大器。

在这个工作，我们提出了一种新型的反馈频率补偿方案，为双级OTAs。该新方案是一种替代方法，用于传统的米勒补偿技术，有效地解决了PSRR和带宽的衰减问题。该新方法要求一个更小的电容；使得芯片面积的减小，并增加了额外的功率到原始放大器。

该论文组织如下。第二章描述了新方案的理论。原点的定义和相关的数学方程提供了这章。模拟结果在第三章给出，最后，第四章总结了论文。

2 The Proposed Compensation Scheme

一个合理设计的双级未补偿放大器通常有两个单独的极点，没有零点在其频率带宽中。因此，简化了频域频域的频域频域函数的一个两极点放大器可以由以下方程给出：

\[ A(s) = \frac{A_0}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} = \frac{A_0 p_1 p_2}{(p_1 + s)(p_2 + s)} \] (1)

其中，\( A_0 \), \( p_1 \), and \( p_2 \)是DC增益，第一，第二极点的放大器，分别。自增益

不频域补偿的，\( p_1 \)和\( p_2 \)是较小的增益带宽，GBW的频率，i.e. \( p_1 < p_2 < \text{GBW} \)。

为了解释频率补偿方案，我们将其用于放大器，\( A(s)\)，在反馈环路中，如图1，和得到一些公式。做这些，频率补偿方案将被讨论，其有效性将被验证如我们所做。

图1显示了负反馈放大器的方框图，它由一个放大器“\( A \)”和反馈块“\( \beta \)”组成。该反馈系统（如图中），其增益带宽频率为\( \omega_0 = p_1 A_0 (1 + \alpha \beta_0) \)，该闭环的频率转移函数应该为1，i.e. \( |A_{\text{CL}}(\omega_0)| = 1 \)。
Considering this condition gives:

\[ \left( \frac{1 + \alpha \beta_0}{\alpha} - \frac{p_1 A_0}{p_2} \right)^2 \left( \frac{1}{1 + \alpha \beta_0} \right)^2 + \left( \frac{p_1 A_0}{p_2} \frac{A_0}{\alpha(1 + \alpha \beta_0)} \right)^2 - \left( \frac{1 + \alpha \beta_0}{\alpha} \right)^2 = 1 \]  

(7)

On the other hand, at unity-gain bandwidth frequency, the phase margin requirement should be satisfied as well, i.e. \( PM = \angle A_{V_2} (\omega_0) + 180 \). Calculating the \( PM \) of (6) at \( \omega = \omega_0 \) gives:

\[ PM = 180 + \tan^{-1} \left( \frac{\omega_0}{\alpha} \right) - \tan^{-1} \left( \frac{\omega_0 (1 + \alpha \beta_0)}{p_1} \right) - \angle D(s), \]

\[ \angle D(s) = \tan^{-1} \left( \frac{\alpha (2 \omega_0 - \sqrt{\Delta})}{p_1 A_0} \right) + \tan^{-1} \left( \frac{\alpha (2 \omega_0 + \sqrt{\Delta})}{p_1 A_0} \right) \]  

(8)

where, \( \Delta \) is given by:

\[ \Delta = \left( \frac{p_1 A_0}{\alpha} \right)^2 - 4 A_0 \left( \frac{1 + \alpha \beta_0}{\alpha} \right) p_1 p_2 \]  

(9)

Replacing \( \omega_0 \) by its equivalence in (8) gives:

\[ PM = 90 + \tan^{-1} \left( \frac{\alpha}{1 + \alpha \beta_0} \right) - \angle D(s), \]

\[ \angle D(s) = \tan^{-1} \left[ \frac{2 \alpha}{1 + \alpha \beta_0} - \frac{4 \alpha (1 + \alpha \beta_0)}{p_1 A_0} - 1 \right] \]

\[ + \tan^{-1} \left[ \frac{2 \alpha}{1 + \alpha \beta_0} + \frac{4 \alpha (1 + \alpha \beta_0)}{p_1 A_0} - 1 \right] \]  

(10)

Solving (7) and (10), gives the values of \( \alpha \) and \( \beta_0 \) that satisfy the required phase margin. The resulted values are not exact, as some approximations have been considered to derive these equations; however, they give a good start point to initiate some iterations to find the proper values that truly satisfy the phase margin requirements.

In the following section the realization of the proposed compensation scheme on a two stage amplifier is discussed.

3 Circuit Realization Based on the Proposed Scheme

In this section, the proposed compensation method is embedded on a well-known two stage amplifier to examine its performance. Let us initially investigate the effect of the proposed scheme on an ideal two-pole op-amp block, before considering the aforementioned two stage amplifier. Fig. 2(a) depicts a realization of the proposed compensation technique where, \( \beta(s) \) is given by \( \beta(s) = \alpha(s + 1/R_C) \). As can be seen in Fig. 2(a), despite the simple realization of the proposed technique, this configuration imposes a serious limitation on the compensated amplifier. In other words, its negative input is not available anymore when it is utilized in a feedback loop. To resolve this issue, the amplifier structure requires a little modification. This can be simply accomplished by adding an extra inverting input to the amplifier considering, as is shown in Fig. 2(b). Considering this inverting input, the amplifier has two distinct inverting ports, one is used for the realization of the compensation network and the other one is available for any other application, such as general feedback network configuration. Undoubtedly, this is not the only application that the proposed scheme can be applied to, and other configurations compatible with the proposed compensation technique can be certainly found or developed. Nevertheless, this article aims to show the performance of the proposed compensation scheme in a simple configuration.

Fortunately, the realization of the modified 3-input amplifier is very straightforward. Fig. 3 depicts the transistor level implementation of the modified amplifier. As it can be seen in Fig. 3, the third input is obtained simply by embedding an extra NMOS transistor satisfying the DMOS design methodology conditions [19], highlighted with red color, in the differential pair of amplifier.

Now, let us derive some formulations for expressing some of the small-signal characteristics of the proposed amplifier shown in Fig. 3.

3.1 The Frequency Response Analysis

Considering the resistances seen from the drains of Mp2 and Mp3, respectively as \( R_i \) and \( R_h \), and regarding that \( g_{m1} = g_{m2} = g_{m3} = g_I \) and \( g_{mp3} = g_{is} \), the following equations can be written.

\[ V_{in} = -g_I R_i \left( -g_I V_{gs2} + \frac{g_I V_{gs2}}{2} + \frac{g_I V_{gs1}}{2} \right) \]  

(11)
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where,

\[ R_i = r_{op2} + 1.5r_{out}, \quad R_{th} = r_{op3} + r_{ab3} \quad (12) \]

Performing some simplifications gives:

\[ V_{out} = g_i g_{th} R_i R_{th} \left( V_{op} - \frac{V_{m-} - V_{op}}{2} - \frac{V_{cp}}{2} \right) \quad (13) \]

From (12), it can be observed that if the two negative input ports of the proposed amplifier are tied together, the proposed amplifier acts as a regular amplifier (with two input ports) with differential DC gain of \( A_v(0) = g_{mn} R_{in}. \) On the other hand, if the proposed amplifier is configured as Fig. 2(b) with positive input node tied to the ground (\( V_{in} = 0 \)), the DC voltage gain is given by \( A_v(0) = g_{mn} R_{in}/2. \)

Considering \( V_{in} = 0 \) and substituting \( V_{op} = \beta V_{out} \) into (13) gives:

\[ \frac{V_{out}}{V_{m-}} = -\frac{A_o}{1 + A_o \beta} \quad (14) \]

where,

\[ A_o = g_i g_{th} R_i R_{th} \quad (15) \]

So far, the effects of the parasitic capacitances are neglected in gain analysis, yielding just the DC voltage gain. As it will be shown in the next section (see Fig. 4), the proposed amplifier has two distinct poles in its operating frequency range. Considering Fig. 3, these two poles occur at frequencies equal to \( p_1 = 1/R_i C_i \) and \( p_2 = 1/R_{th} C_{th}, \) where, \( C_i \) and \( C_{th} \) are given by (16). Hence, Eq. (14) can be rewritten as (17)

\[ C_i = c_{dp2} + c_{dp2} + c_{op3}, \]

\[ C_{th} = c_{dp3} + c_{dp3} + c_L \quad (16) \]

The Eq. (17) shows that if the proposed amplifier is configured as Fig. 2(b), its frequency transfer function is Analogous with that is of Fig. 1 (refer to (2)). Therefore, the formulations derived in previous section can be exploited to obtain the frequency response of the compensated amplifier, as well as, the corresponding values for R and C that satisfy (10).

3.2 The PSRR Analysis

To evaluate the PSRR of the proposed circuit, consider the amplifier configuration as in Fig. 4, where the power supply variations is shown with \( V_{dd}. \) Respecting this figure, the output voltage can be defined as:

\[ V_{out} = -\frac{A(s)}{2} V_{m-} - \frac{A(s)}{2} V_{op} + A_{dd}(s) V_{dd} \quad (18) \]

where \( A_{dd}(s) \) is the voltage gain from \( V_{dd} \) to \( V_{out}. \) Replacing \( V_{op} \) with \( \beta V_{out} \) in (18) gives:

\[ V_{out} = -\frac{A(s)}{2+2A(s)\beta(s)} V_{m-} + \frac{2A_{dd}(s)}{2+2A(s)\beta(s)} V_{dd} \quad (19) \]

Recalling the definition of the PSRR which is given by 
\( (V_{out}/V_{in})(V_{out}/V_{dd}), \) from (19), the PSRR of the proposed circuit is given by:

\[ |PSRR| = \frac{A(s)}{2A_{dd}(s)} \quad (20) \]
The $A(s)$ already is defined in (17), though if $A_{dd}(s)$ can be determined properly, the PSRR can be obtained accordingly. To do so, we need to tie the inputs of the amplifier to the ground and obtain the transfer function from $V_{dd}$ to $V_{out}$. Fortunately, in this configuration, the proposed amplifier acts exactly like a traditional uncompensated two-stage amplifier. Therefore, $A_{dd}(s)$ is given by [20, 21]:

$$A_{dd}(s) = \frac{1}{1 + \frac{s}{p_1}}$$

(21)

Substituting $A(s)$ and $A_{dd}(s)$ from (17) and (21) in to (20) gives the PSRR value as:

$$\text{PSRR} = \frac{A_i}{2\left(1 + \frac{\lambda}{p_2}\right)}$$

(22)

4 Post-Layout Simulation Results

The performance of the proposed compensation scheme and its application on the modified two-stage amplifier (see Fig. 3) is investigated through Spectre post-layout simulations with TSMC 180nm CMOS standard technology. After compensation, the performance of the proposed structure is compared with that of the traditional two-stage miller-compensated amplifier. To have a fair comparison, each amplifier is optimally designed and compensated to have 50° phase margin at the presence of a 30pF load capacitance. The layout view of the amplifiers is shown in Fig. 5. The transistors’ aspect ratios and the amplifiers’ bias conditions are summarized in Table 1.

The frequency behavior of an uncompensated two-stage amplifier, with the specifications given in Table 1, is shown in Fig. 6. This figure shows that the amplifier has two poles in its frequency bandwidth, making the frequency compensation necessary to enable the amplifier to be appropriately used in feedback configurations. The poles are evaluated to be $p_1 = 162$ kHz and $p_2 = 18.75$ MHz.

### Table 1 The bias conditions and transistors’ dimensions.

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Traditional</th>
<th>Proposed</th>
</tr>
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<tr>
<td>Ib</td>
<td>56 µA</td>
<td>100 µA</td>
</tr>
<tr>
<td>Mb1</td>
<td>27µm/540nm</td>
<td>27µm/540nm</td>
</tr>
<tr>
<td>Mb2</td>
<td>108µm/540nm</td>
<td>108µm/540nm</td>
</tr>
<tr>
<td>Mb3</td>
<td>540µm/540nm</td>
<td>54µm/540nm</td>
</tr>
<tr>
<td>Mn1, Mn2</td>
<td>56µm/180nm</td>
<td>56µm/180nm</td>
</tr>
<tr>
<td>Mn3</td>
<td>NA</td>
<td>56µm/180nm</td>
</tr>
<tr>
<td>Mp1</td>
<td>140µm/540nm</td>
<td>280µm/540nm</td>
</tr>
<tr>
<td>Mp2</td>
<td>140µm/540nm</td>
<td>140µm/540nm</td>
</tr>
<tr>
<td>Mp3</td>
<td>2*700µm/540nm</td>
<td>140µm/540nm</td>
</tr>
</tbody>
</table>

**Fig. 5** The layout view of the design.

**Fig. 6** The frequency behavior of the uncompensated two-stage amplifier.
The numerical values of $\alpha$ and $\beta_0$ must be obtained to compensate the circuit with the proposed compensation scheme. Considering the configuration of Fig. 2(b), the value of $\beta_0$ is obtained as 0.66. Substituting the values of $\beta_0, p_1$, and $p_2$ into (10), gives the value of $\alpha$ for a specified PM. Taking 50° phase margin into account, the value of $\alpha$ evaluated to be 2.23. The value of $\alpha$ equal with 2.23 is translated to the 80MHz pole frequency in the feedback network, i.e. $p_f = 80\text{MHz}$. This gives the RC value of about 2ns. Selecting the value of $R = 6k\Omega$, gives the value of $C = 0.33\text{pF}$. Simulating the compensated amplifier with the values obtained for $R$ and $C$, the phase margin of about 47° is obtained which is very close to the desired value. To achieve a strictly precise result, the design is re-simulated by sweeping the value of $C$ around its predicted value. This gives the proper value for $C$, that is $C = 0.4\text{pF}$, which essentially delivers the required 50° phase margin. As stated in the first paragraph of this section, an optimally designed miller compensated amplifier is considered to compare its performance with that of the proposed structure. Fig. 7 shows the frequency behavior of the proposed circuit versus frequency behavior of the traditional miller compensated amplifier.

As can be observed from Fig. 7, both of the amplifiers deliver the same amount of PM, which is about 50°. Comparing the results, it is clear that the traditional amplifier presents a little higher DC gain, however, its maximum operating frequency is much less than the proposed one. In other word, the proposed structure delivers a larger gain bandwidth product value, which makes it more suitable for high frequency applications. The power supply rejection ratios (PSRR) of both amplifiers are compared in Fig. 8. As is shown, although the PSRR value of the proposed structure is less than that of the traditional one in lower frequencies, but the PSRR of the traditional amplifier starts to roll off much faster, presenting much less PSRR than the proposed amplifier in higher operating frequencies (especially in Fig. 8(a)). This, in fact, was predictable as it is the intrinsic disadvantage of the miller compensated amplifiers. The higher DC value of PSRR in traditional amplifier is due to its higher DC gain in this specific design.

The transient step response of the proposed amplifier is compared with the response of traditional amplifier in Fig. 9. As this figure shows, both of the amplifiers are stable and deliver fast rising and settling time. As is shown in Fig. 9, the proposed structure settles two times faster than the traditional amplifier.

To evaluate the robustness of the proposed structure against process uncertainties, the Monte Carlo simulation is performed to examine the two most important and vulnerable parameters, namely phase margin and DC gain. As is shown in the histograms of Fig. 10, the robustness of the proposed structure is acceptable, which assures its well-functionality after fabrication.

The important specifications of the proposed structure, incorporating the novel active feedback compensation scheme is compared with that of the traditional miller compensated amplifier in Table 2. Examining Table 2 shows that the two amplifiers are almost the same in most of the parameters except the merits of gain bandwidth product and power consumption. In fact, the amplifier designed based on the proposed compensation
scheme delivers much more gain bandwidth product consuming much less power. This makes the proposed structure more power efficient and favorable for low power and high speed applications.

5 Conclusion

A novel active feedback frequency compensation scheme is presented in this work. The Spectre post layout simulations proved that a two-stage amplifier can be well-compensated based on the proposed active feedback frequency compensation scheme. The effectiveness of the proposed method is also verified through the mathematical formulations as well. The simulations were done utilizing TSMC 180nm CMOS standard technology. The Spectre post layout simulations showed that the proposed structure outperforms the traditional structure in terms of power consumption and gain bandwidth product. The robustness of the design was checked with Monte Carlo simulations exhibiting acceptable results.

References


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