Multi-Objective Learning Automata for Design and Optimization  
A Two-Stage CMOS Operational Amplifier

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Abstract: In this paper, we propose an efficient approach to design optimization of analog circuits that is based on reinforcement learning method. In this work, Multi-Objective Learning Automata (MOLA) is used to design a two-stage CMOS operational amplifier (op-amp) in 0.25μm technology. The aim is optimizing power consumption and area so as to achieve minimum Total Optimality Index (TOI), as a new and comprehensive proposed criterion, and also meet different design specifications such as DC gain, Gain-Band Width product (GBW), Phase Margin (PM), Slew Rate (SR), Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR) etc. The proposed MOLA contains several automata and each automaton is responsible for searching one dimension. The workability of the proposed approach is evaluated in comparison with the most well-known category of intelligent meta-heuristic Multi-Objective Optimization (MOO) methods such as Particle Swarm Optimization (PSO), Inclined Planes system Optimization (IPO), Gray Wolf Optimization (GWO) and Non-dominated Sorting Genetic Algorithm II (NSGA-II). The performance of the proposed MOLA is demonstrated in finding optimal Pareto fronts with two criteria Overall Non-dominated Vector Generation (ONVG) and Spacing (SP). In simulations, for the desired application, it has been shown through Computer-Aided Design (CAD) tool that MOLA-based solutions produce better results.

Keywords: Analog Circuit Design, Area and Power Optimization, Multi-Objective Learning Automata, Total Optimality Index.
1. Introduction

The main field of this paper is related to three topics: integrated circuit design, meta-heuristic optimization methods, and the use of Learning Automata (LA) based on the reinforcement learning approach. Its main topic is the relationship between the Multi-Objective Learning Automata (MOLA) in terms of optimal design of operational amplifiers (op-amps), which are one of the most used modules in analog integrated circuits. In the following, in three different parts these main topics are described separately.

Op-amps are one of the most important sub-sections in analog circuits. A two-stage op-amp is used widely for various applications due to its robustness and structure. For example in [1], a novel low-voltage two-stage operational amplifier employing resistive biasing is presented. In [1], for each stage, an independent common-mode feedback a circuit has been used which reduced the power consumption and increased output voltage swing. Analog circuit design is a challenging process which involves the characterization of complex trade-offs between nonlinear objectives and the specifications such as DC gain, Gain-Band Width product (GBW), Phase Margin (PM), Slew Rate (SR), Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR) etc. Due to the complexity of analog circuits, their manual design with high performance and low power is not simple. Therefore, intelligent optimization methods are required for automation and optimal sizing of CMOS analog ICs design [2]. One of the most well-known categories is the meta-heuristic algorithms.

Meta-heuristic algorithms have high performance and ability for solving optimization problems. The purpose of meta-heuristic algorithms is to find proper values for the decision design parameters of an optimization problem to optimize one/multiple objective function [3]. These methods are being developed to design the size of analog circuits. With the advancement of ICs manufacturing technology, it is important to design circuits with high accuracy and in the smallest size possible. Heuristic-based approaches perform circuit design in the form of the Single-Objective (SO) and Multi-Objective (MO) optimization. Usually analog circuits have several conflicting performances. For this reason, the Multi-Objective Optimization (MOO) has
also been introduced for the automated design of CMOS analog ICs. It would be useful to produce a set of results for the designers with the best trade-off between performances. Unlike SO optimization methods, a MOO algorithm attempts to find non-dominated solutions during the optimization process. In designing amplifier circuits, power and area are in conflict with each other; so that by decreasing the channel length, the speed of MOSFETs increases (which means reducing the delay). This increase in speed leads to increased power consumption. Therefore, MO techniques are used simultaneously to reduce the power consumption and area of MOSFETs [4]. Meta-heuristic methods are applied for MO analog circuit optimizations.

One of the important MO methods is the NSGA-II evolutionary algorithm. NSGA-II was proposed in 2002 by Deb [5]. It is a modified version of Genetic Algorithm (GA) [6] with elitist approach. The GA concept is developed from natural evolution process. Based on the Darwin theory “survival of fittest”, the GA mimics the natural evolution method. The elitism approach used to copy best parents and offspring (i.e., child) produce by the genetic operators. In NSGA-II algorithm, non-dominated solution is obtained from the current parents and their offspring using objective functions. This algorithm has shown its ability in many applications. Therefore, in this paper, it is used as one of the competing algorithms and is assigned in a sub-section [5].

Several studies have been carried out in the design and optimization of circuits, which have achieved favorable results by providing approaches based on circuit theory and intelligent optimization techniques. For example, GSA-PSO algorithm was used to optimization differential amplifier circuit with current mirror load and CMOS two-stage operational amplifier circuit [7]. In [8], a new approach is proposed to automatically size three conventional amplifier circuits. In order to enhance the performance of automatic sizing of analog circuits, a new shrinking circles technique has been used [9]. A Weighted Expected Improvement based Bayesian Optimization (WEIBO) is proposed for the automated analog circuit sizing [10]. The hierarchical Non-dominated Sorting Genetic Algorithm II (hNSGA-II) [11] and Improved Brain Storm Optimization (IMBSO) [12] algorithms are proposed for MOO of circuits. An Inversion Coefficient (IC) optimization based
analog/RF circuit sizing approach is proposed in three different circuits [13]. One of the other important approaches that is ignored in the optimal design of analog circuits and can be applied along with meta-heuristic algorithms is LA based on the reinforcement learning.

LA is a reinforcement learning approach that is an unsupervised optimization method and one of the main components in adaptive learning systems. It is an important research area of Artificial Intelligence (AI) and has a wide range of applications in, for instance data mining [14,15], image processing [16,17] and optimization [18-20]. The general technique of choosing an action from a series of actions is related to the highest reward compared to other actions. This result is achieved through interactions with the environment in terms of a sequence of repetitive feedback cycles. By learning to choose the optimal action, the automata adapt themselves to the environment, needless to have detailed information about the environment model [21]. The idea of LA was first introduced by Tsetlin to model biological learning mechanism [22]. In LA research, various types of LA-based algorithms have been developed. In this work, we have used the MO version of Learning Automata (MOLA) method [23] for the automated design of a two-stage CMOS op-amp. This paper focuses on the design of circuit parameters, considering the assumption of the appropriate topology is selected by the designer.

This paper contains several contributions that are listed as follows:

- A new application of LA for MOO in the optimal design of CMOS analog IC.
- Proper definition of design parameters and objective functions to create an effective trade-off between performance characteristics.
- Implementation of an automated design simulation tool by creating a link between two usable software environments.
- Providing a comprehensive criterion to evaluate the proposed approach due to the simultaneous effect of objectives and design specifications on the optimization problem.
The statistical evaluation of the proposed approach based on numerical results obtained from circuit simulations with other competing algorithms.

This paper is organized as follows. Section 2 introduces our proposed tool, case study, and along with a description of the MOLA method and rival meta-heuristic MOO algorithms. In Section 3, the considerations for design and optimization of the proposed circuit are provided. The simulation results are reported in Section 4. Finally, in Section 5 the conclusion is expressed.

2. Meta-heuristic Approaches for Multi-Objective Simulation-based Optimization

In real applications, we constantly deal with problems that under specific circumstances are faced with several objective functions simultaneously. These issues are in the field of MOO. In other words, the role of a MOO is to simultaneously optimize two or more objective functions. These objectives are usually in trade-off. So, the meta-heuristic approaches are the best candidate for solving them. In this method, unlike the SO method, which only receives an acceptable solution, there is a set of optimal solutions, known as Pareto-optimal solutions or Pareto-front. In such problems, a set of solutions, which complies each objective function with an acceptable level, is defined as optimal solutions.

In this section, an automated MO simulation-based optimization approach is proposed for intelligent and optimal design of analog IC. The proposed Computer Aided Design (CAD) tool is applied for this purpose. It should be noted that analog circuits are simulated by HSPICE simulator. By connecting MATLAB and HSPICE software, the optimization process is done (Fig. 1). In the beginning, design parameters and design specifications are determined by the designer, while a reasonable predefined range is also taken into account for each design parameter. Note that design parameters consist of the length and width of the CMOS transistors, capacitor values, and biasing current.
Continue on this section, the desired amplifier circuit, the MOLA method with other MOO algorithms employed is explained.

2.1. Two-stage CMOS op-amp

In order to show the performance of the proposed MOLA method in the design of analog circuits, a two-stage CMOS op-amp in 0.25μm technology is used. There are 13 design parameters in this circuit. In Fig. 2, a two-stage CMOS op-amp is shown with Miller compensation capacitance. Miller’s compensation technique is used to frequency compensation in this amplifier to utilize bandwidth, phase margin, and circuit stability. This movement of the amplifier pole to reduce the frequency of dominant pole improves the amplifier stability. Therefore, a low-frequency pole can be established with moderate capacitor value, saving considerable chip area [24]. Design parameters in this circuit include transistor widths and lengths, biasing current (I\text{bias}), compensation capacitance (C\text{c}), and load capacitance (C\text{L}). Here, the appropriate matching relations are also imposed as $M_1 \equiv M_2$, $M_3 \equiv M_4$, and $M_5 \equiv M_8$. Furthermore, the positive power supply ($V\text{DD}$) and the negative power supply ($V\text{SS}$) are equal to 2.5V and -2.5V, respectively [8]. This circuit set values for the $C\text{C}$ and $C\text{L}$ that provide $C\text{C} > 0.22C\text{L}$ [7]. Desired specifications (small-signal differential voltage gain (DC gain), Gain-Band Width product (GBW), Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR), etc) are in accordance with Table 1.
In this paper, for the first time, the MOLA method is used along with four rival MOO algorithms (called NSGA-II [5], MOPSO [25], MOIPO [26], and MOGWO [27]). In the following, the description of the proposed algorithm is presented with four competing algorithms.

2.2. Non-dominated Sorting Genetic Algorithm II (NSGA-II)

In NSGA-II, sorting and ranking all solutions are created by the main features (diversity, convergence, and robustness of solutions in the Pareto-front) in order to choose better solutions to create new offsprings. The NSGA-II is based on fast non-dominated sorting and crowding distance assignment methods. The NSGA-II creates a population of individuals and then creates a non-domination level to rank and sort each individual. Then, it utilizes cross-over, mutation, and selection operators to produce new offspring. Subsequently, the
parents and offsprings are combined before partitioning the new combined pool into fronts [5]. The flowchart of the NSGA-II algorithm is depicted in Fig. 3.

![Flowchart of the NSGA-II algorithm](image)

**Fig. 3.** Flow chart of the NSGA-II algorithm

2.3. Multi-Objective Particle Swarm Optimization (MOPSO)

The PSO is one of the most important intelligent optimization algorithms [28]. One of the most popular and effective proposals for MO versions of the PSO optimization algorithm is presented in [25]. The position of the non-dominated particles is stored in a repository. Then, the search space is divided into a number of hypercubes. These non-dominated particles are located in accordance with the values of their objective functions in the hypercubes. While the maximum number of iterations is not provided, the speed and position of the particles are updated. Then the contents of the repository are updated. This update consists the inserting
all the currently non-dominated locations in the repository and the removal of the dominated locations from it during the process. Since the repository size is limited, whenever it gets full, hypercubes that contain more particles in themselves are identified and the excess particles are randomly removed from the hypercubes [25].

The flowchart of the MOPSO algorithm is shown in Fig. 4.

![Flow chart of the MOPSO algorithm](image)

**Fig. 4. Flow chart of the MOPSO algorithm**

2.4. **Multi-Objective Inclined Planes system Optimization (MOIPO)**

The search factors in Inclined Planes system Optimization (IPO) algorithm are the number of small balls that are located on a sloping surface without friction. Three attributes of position, height and angels in relation to other balls are considered for each ball. The main idea of this algorithm is to assign a height to each ball according to its objective function. Height values represent the potential energy of the balls, and the movement of the balls downwards converts potential energy to kinetic energy and causes acceleration. In fact, agents tend
to fine their potential energy and to reach the minimum point(s). The position of each agent is a possible solution in the problem space [29]. The MO version of the algorithm has been created in [26]. Also, Fig. 5 shows its flowchart.

**Fig. 5. Flow chart of the MOIPO algorithm**

2.5. **Multi-Objective Gray Wolf Optimization (MOGWO)**

The Gray Wolf Optimization algorithm is inspired by the hierarchical structure of the wolf position in the group as well as its structure and duties in hunting. In this algorithm, the search factors corresponding to wolves, the hunting process corresponds to the process of finding the optimal response and the location of the hunt corresponding to the optimal response position [30]. MOGWO flowchart is shown in Fig. 6.
2.6. **Multi-Objective Learning Automata (MOLA)**

The MOLA is found more practicable and efficient in finding accurate solutions for complex optimization problems. The number of automata used in the MOLA method is equal to the dimensions of the problem. For $N$ dimensional problem, the MOLA includes $N$ automata [23]. The structure of learning automata for MOLA has been shown in Fig. 7. Each automaton is responsible for searching one dimension and acts independently in the environment.
The $i$-th learning automata is defined by $\{x_i, A_i, r, P_i, U\}$, where $\chi_i = \{x_i\}$ is the set of possible states on the $i$-th dimension. Also, $x_i$ is the dimensional state on the $i$-th dimension ($x_i \in [x_{\text{min},i}, x_{\text{max},i}]$), the minimum and maximum values in the $i$-th dimension are $x_{\text{min},i}$ and $x_{\text{max},i}$, respectively. In MOLA, $A_i = \{a_{i,\eta}\}$ is the set of possible actions which the learning automata can take on dimension $i$, $a_{i,\eta}$ indicates that an action moves left ($l=1$) or right ($l=2$) and $\eta$ is step length. Note that $r$ is a scalar value and shows reinforcement signal. It is produced through the environment to indicate the quality of the action of moving $x_i$ in a step length on the selected path. Also, $P_i$ consists of two probabilities $p_1$ and $p_2$. Where $p_1$ shows the probability of selection the left path or the right path on $i$-th dimension. Assume that the right path is selected, the probability of choosing a cell between the $k$ cells located on the path determines by probability of $p_2$. Also, $U$ is a scheme adopted to calculate the probabilities of actions, $P$.

In the MOLA method, each dimension is divided into $D$ cells. This means that, $\chi_i$ is divided into $D$ subsets and subset includes all dimensional states located in the cell. Therefore, $N \times D$ cells are produced for an $N$-dimensional search space. Considering the $x_{\text{min},i}$ and $x_{\text{max},i}$ are minimum and maximum values in the $i$-th dimension, respectively. Also, $D$ is number of divisions of each cell. Then, $w_{c,i}$ is the width of a cell in $i$-th dimension, and it is calculated by (1).
In the beginning of the action search, in order to estimate the choice of a better solution on the path, we should be able to choose one of two possible directions. In other words, the path values must be determined by the amount of the cell values on the path.

As shown in Fig. 8, the value of $L_2(x_i)$ is specified by the values of $k$ adjacent cells on the right path, where $k$ is the integer predefined value and $c_{i,j}$ is $j$-th cell in $i$-th dimension. Also, $j$ is calculated by (2).

$$j = \text{floor}(x_i - x_{\text{min}}) / \omega_{i,j}$$

(2)

The value of a path can be estimated as (3). Where $v_{i,m}$ presents the $m$-th element of the vector which is placed on path $l$. Also $\lambda_i$ is calculated with $0 \leq \lambda_i \leq 1$ and $(1 - \lambda_i) \sum_{k=1}^{i-1} \lambda_i^{k-1} = 1$, subject to $(1 - \lambda_i) \lambda_i^{i-2} \geq \lambda_i^{i-1}$.

$$L_i(x_i) = (1 - \lambda_i) \sum_{m=1}^{i-1} \lambda_i^{m-1} v_{i,m} + \lambda_i^{i-1} v_{i,s} \quad l = 1,2$$

(3)

Fig. 8. The two possible paths taken by a search starting at dimensional state $x_i$ on the $i$-th dimension [23]

Two probabilities of $p_1$ and $p_2$ are obtained from (4) and (5). Where $V(x_i)$ is cell value. Temperature $\tau$ creates trade-off between the exploration and exploitation.

$$p_1(L_i(x_i)) = \frac{e^{\lambda_i V(x_i) / \tau}}{\sum_{l=1}^{2} e^{\lambda_i V(x_i) / \tau}} \quad l = 1,2$$

(4)

$$p_2(c_{i,s}) = e^{V(x_i) / \tau} \frac{1}{\sum_{s=1}^{k} e^{V(x_i) / \tau}} \quad l = 1,2 \quad s = 1,..,k$$

(5)
By choosing a cell, an action moves to the new cell with a step length that can be denoted as $\eta$. Which is calculated in accordance to (6). In (6), the distance (in the form of number of cells) between the current cell and the selected cell is $\xi$ and $\zeta$ is a random number ($\zeta \in [0,1]$).

$$\eta = (\xi + \zeta) \omega_{i,j}$$ \hspace{1cm} (6)

Therefore, when the $L_I$ is selected, current dimensional state $x_i$ moves to $x_i = x_i - \eta$ and with the choice of $L_2$, $x_i$ moves to $x_i = x_i + \eta$. Then a reinforcement signal is used to check the new dimensional state $x_i$. When dimensional state $x_i$ moves to $x'_i$, the $i$-th element of the current state $X(x_i)$ is replaced by $X(x'_i)$. Reinforcement signal is assigned to cell $c_{i,j}$ according to (7). In (7), $r = 1$ indicates that the solution is desirable and $r = 0$ presents an undesirable response.

$$r(X(x'_i)) = \begin{cases} 1 & \text{if } X(x'_i) \text{ is a non-dominated solution} \\ 0 & \text{otherwise} \end{cases}$$ \hspace{1cm} (7)

The reinforcement signal is applied to update the cell value of cell $c_{i,j}$ which dimensional state $x'_i$. Considering that $L_{max}(x_i) = \max \{L_1(x_i), L_2(x_i)\}$ and $L_{min}(x_i) = \min \{L_1(x_i), L_2(x_i)\}$ are the two estimated path values at $x_i$. Also, weights $\alpha_i$ and $(1 - \alpha_i)$ present the influence of previous estimates and path values on the new estimate, respectively. Then, the value of cell $c_{i,j}$, where the current dimensional state $x_i$ locates, is updated as (8). In (8), the $L_{max}(x_i)$ has a greater influence on the cell value than $L_{min}(x_i)$, therefore parameter $\lambda_2$ should be given such that $(1 - \lambda_2) > \lambda_2$.

$$V(x_i)|_{\omega_{i,j}} \leftarrow r(X(x_i)) + \alpha_i V(x_i)|_{\omega_{i,j}} + (1 - \alpha_i)(1 - \lambda_2)L_{max}(x_i) + \lambda_2 L_{min}(x_i)$$ \hspace{1cm} (8)

A repository saves all non-dominated solutions in an elite list, $L$. If $X(x'_i)$ dominates all of the $L$ solutions, it is known as $X_{best}$ and then $L$ is updated. In (9), the relation between $X$ and $X_{best}$ is shown.
\[
X_{best} \leftarrow \begin{cases} X(x') & \text{if } X(x') \text{ is a non-dominated solution} \\ X_{best} & \text{otherwise} \end{cases}
\] (9)

Where

\[
X(x') = [x_1, \ldots, x_i, x'_i, x_{i+1}, \ldots, x_N]
\] (10)

Then \( L \) is updated according to (11). Where \( B \) is set of the solutions which is dominated by \( X_{best} \)

\[
L \leftarrow \begin{cases} L \cup \{X_{best}\} - B & \text{if } r = 1 \\ L & \text{otherwise} \end{cases}
\] (11)

To increase the variety and explore the solutions of radiation solutions, we apply perturbations according to (12). Where \( \beta \) is random variable (\( \beta \in [0,1] \)).

\[
X' \leftarrow X + \Delta + \beta(X_{best} - X)
\] (12)

Also, \( \Delta \) is calculated according to (13). Where \( \zeta \) is random variable (\( \zeta \in [0, \frac{k}{D}] \)). The input to the sign function is the subtraction of the two adjacent cell values of \( j_i, c_{ij} \), which is represented by (14)

\[
\Delta_i = sign(\kappa)\zeta(x_{max,j} - x_{max,j})
\] (13)

\[
\kappa = V(y_{i,j}, c_{ij}, x_{max,j}) - V(z_{i,j}, c_{ij}, x_{max,j})
\] (14)

The sign function acts as (15)

\[
\text{sign}(\kappa) = \begin{cases} 1 & \kappa > 0 \\ -1 & \kappa < 0 \end{cases}
\] (15)

The \( N_{femax} \) is a given maximum number of objective functions evaluations by which the MOLA computations proceed in episodes.

3. The Considerations for Design and Optimization of the Proposed Circuit
The approach is based on intelligent sizing to power and area optimization using the proposed meta-heuristic methods. So, in this Section, the objective functions, the proposed new index, and Pareto-front evaluation criteria are presented.

3.1. Objective Functions

In this paper, intelligent methods are used to optimize the two important and essential indicators of amplifier circuits that are in conflict with each other, namely power consumption and area. This Objective functions are considered as follows.

- Minimizing power consumption
- Minimizing the area

3.2. Total Optimality Index (TOI)

In this paper, due to the diversity and multiplicity of qualitative indicators in the design problem, a total criterion is presented that illustrates the success of the optimization method. This criterion can be used to investigate the performance of the proposed optimization method in the design problem. Therefore, a criterion called Total Optimality Index (TOI) is proposed. The TOI has been introduced to express the impact of the design specifications and the objective functions of the problem. The lower value of TOI represents the more favorable response. In the paper, TOI is not considered as an objective function.

The main purpose of the proposed index is to provide a comprehensive criterion for verifying the superiority and success of an intelligent optimization method employed in the optimal design of the problem; so that the audience, through the numerical values of this index, can grasp the definitive and comprehensive success of the proposed approach in this paper. Therefore, its scientific basis is based on the merging of the parameters the objective functions, problem constraints, and some mathematical tools in such a way as to achieve the optimal value of each of the parameters can be found in the minimum/maximum value of the index. For this
purpose, in addition to incorporating the optimal values of the objective functions, the circuit constraints are also intelligently taken into account. The resulting values of this index are to be minimized, and its low value represents the success of an optimization method to overcome the design challenge and to achieve global optimal solutions while satisfying the exact constraints of the problem.

Assuming that $A$ is total area of the MOSFET in $\mu$m$^2$ and $P$ is the power consumption in mW (as the objective functions), $C$ is design specifications (constraints) and $C_B$ is specifications boundary value in the problem of designing an amplifier circuit. Then, the index is defined as follows:

$$\text{TOI} = \frac{\text{normalized} \left( \frac{A(\mu m^2) \cdot P(mW)}{\text{sum}(C_B)} \right)}{\text{sum}(C_B)}$$

(16)

In (16), to balance the values of power and area, the amount of area is normalized between zero and one and due to the negativity of some of the design specifications, the $|C_B|$ is used. The most desirable TOI (minimum) is created by minimizing objective functions and maximizing the design specifications. The design of the TOI is such that the main focus is on the objective functions of the problem and a minor improvement in one of them will minimize the TOI.

3.3. Pareto-front evaluation criteria

In order to evaluate Pareto-front, two criteria of the Overall Non-dominated Vector Generation (ONVG) and Spacing (SP) are used. Despite the existence of other criteria for studying the quality of the Pareto-front, the reason for choosing these two criteria is that there is no need to know the real Pareto-front and they are produced in accordance with the received Pareto-front.

- ONVG: The ONVG represents the number of optimally non-dominated responses (based on Pareto-front) in a MO problem. Where $|PF_{\text{known}}|$ is the number of vectors in $PF_{\text{known}}$ (known/current Pareto-front).
\[
ONVG \equiv |PF_{\text{known}}|
\]

1. **SP**: The SP numerically represents the spread of the vectors in the \(PF_{\text{known}}\) and measures the distance variance of neighboring vectors in it (as (18)). Where \(d_i = \min_j (|f'_i(x) - f'_j(x)| + |f''_i(x) - f''_j(x)|), i,j=1,\ldots, n, \bar{d} \) is the mean of all \(d_i\), and \(n\) is the number of vectors in \(PF_{\text{known}}\) (\(|PF_{\text{known}}|\)). So that, \(SP = 0\), means that all members are spaced evenly apart in [26].

\[
SP = \sqrt{\frac{\sum_{i=1}^{n} (\bar{d} - d_i)^2}{n-1}}
\]  

4. **Simulation Results**

In this section, the results and analysis are presented in the optimization of two-stage CMOS op-amp. All the results are reported in the form of the values of fitness objective functions, design parameters, design specifications, and TOI. The best, worst, mean, and variance of the values of the objective functions and the TOI are presented for proposed methods in the best run. Figures of the Pareto-front and the design specifications of the two-stage CMOS op-amp including DC gain, Phase Margins, PSRR, and Slew Rate are plotted by the proposed methods. In addition, the Pareto indexes and the runtime of MOLA performance are analyzed in comparison with other proposed algorithms for the best run. All implementations are performed in MATLAB 2016a MathWorks and HSPICE A-2008.3 under a computer system with Intel® Core™ i5-4460U CPU @ 3.20GHz, 4GB RAM, and Windows Enterprise 10. The vector of design parameters that should be determined by the proposed methods is as follows:

\[
X = [W_t, W_1, W_e, W_r, L_t, L_e, L_r, C_e, C_c, I_{bias}]
\]

The details on design parameters for two-stage CMOS op-amp are listed in Table 2. Also, in Table 3 all control parameters of the proposed methods in this paper are presented.
### Table 2. **The Range of Design Parameters**

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>Lower bound</th>
<th>Upper bound</th>
</tr>
</thead>
<tbody>
<tr>
<td>W (µM)</td>
<td>5</td>
<td>40</td>
</tr>
<tr>
<td>L (µM)</td>
<td>0.25</td>
<td>2</td>
</tr>
<tr>
<td>I&lt;sub&gt;in&lt;/sub&gt; (µA)</td>
<td>20</td>
<td>40</td>
</tr>
<tr>
<td>C&lt;sub&gt;C&lt;/sub&gt; (PF)</td>
<td>2</td>
<td>20</td>
</tr>
<tr>
<td>C&lt;sub&gt;L&lt;/sub&gt; (PF)</td>
<td>7</td>
<td>15</td>
</tr>
</tbody>
</table>

### Table 3. **Control Settings**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>NSGA-II</th>
<th>MOPSO</th>
<th>MOIPO</th>
<th>MOGWO</th>
<th>MOLA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Run</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>MaxIt / N&lt;sub&gt;femax&lt;/sub&gt;</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>2000</td>
</tr>
<tr>
<td>nPop</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>1</td>
</tr>
<tr>
<td>nRep</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>nGrid</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>α</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>β</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>γ</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>P&lt;sub&gt;c&lt;/sub&gt;</td>
<td>0.9</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>P&lt;sub&gt;r&lt;/sub&gt;</td>
<td>0.1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>η&lt;sub&gt;ci&lt;/sub&gt;</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>η&lt;sub&gt;ri&lt;/sub&gt;</td>
<td>18</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>C&lt;sub&gt;C&lt;/sub&gt;/c&lt;sub&gt;1&lt;/sub&gt;</td>
<td>—</td>
<td>1.4962</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>C&lt;sub&gt;L&lt;/sub&gt;/c&lt;sub&gt;2&lt;/sub&gt;</td>
<td>1.4962</td>
<td>3.05</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>w</td>
<td>—</td>
<td>0.73</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>w&lt;sub&gt;zoom&lt;/sub&gt;</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>shift1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>shift2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>scale1</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>scale2</td>
<td>—</td>
<td>0.03</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>δ&lt;sub&gt;i&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>e[0,2]</td>
</tr>
<tr>
<td>r&lt;sub&gt;1&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>e[0,1]</td>
</tr>
<tr>
<td>r&lt;sub&gt;2&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>e[0,1]</td>
</tr>
<tr>
<td>D</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>500</td>
</tr>
<tr>
<td>k</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>50</td>
</tr>
<tr>
<td>α&lt;sub&gt;i&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>e[0,1]</td>
</tr>
<tr>
<td>ξ&lt;sub&gt;i&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
</tr>
<tr>
<td>η&lt;sub&gt;ξ2&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>e[0,1]</td>
</tr>
<tr>
<td>τ&lt;sub&gt;ξ2&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>e[0,0.5]</td>
</tr>
</tbody>
</table>

In order to demonstrate the ability of the reinforcement learning method to solve the problem of circuit optimization, the results are compared with several intelligent methods and previous studies.

Tables 4-9 show the best run of the algorithms for this circuit that is generated by the best TOI. In all tables, the bolded responses show the best values in terms of design specifications, objective functions, and TOI in the best run. A solution marked by a sub-line expresses a solution in the desired Pareto-front, which has the best TOI (minimum). MOLA method is able to produce the minimum area and power consumption with the values 72.825 µm² and 0.560 mW, respectively. The algorithms intelligently set values for the C<sub>C</sub> and C<sub>L</sub> that provide C<sub>C</sub> > 0.22C<sub>L</sub>. Additionally, the ability of the MOLA is more specific than other algorithms in the TOI.
The algorithms performance presents an intelligent optimization and trade-off between objectives of the problem. The variety and the number of presented Pareto-front solutions provide a wide range of selection for the circuit designer. According to tables, this superiority, relative to all the Pareto-optimal solutions of algorithms, is achieved with 36.36, 18.18, 18.18, and 9.09% by MOLA, MOGWO, MOPSO, and NSGA-II, respectively. Due to the well-known and widely used of NSGA-II, it was expected to perform better than other algorithms. Although it has not been able to demonstrate its superiority to others, especially the proposed method MOLA; but it has in many cases been able to provide good results than MOPSO, MOIPO, and MOGWO.

Fig. 9 shows the Pareto-fronts in the best run (in terms of TOI criterion) for the proposed methods. Despite the greater spread the Pareto-front of the NSGA-II, it can be argued that MOLA responses have dominated Pareto-front solutions of other algorithms. The HSPICE simulation results obtained from the optimally designed two-stage CMOS op-amp are shown in Figs. 10-13 for the best solution (based on the best TOI value) in the best run. Also, the results obtained from the MOLA method are shown in Figures. A comprehensive comparison is presented in Table 10 between the results of the proposed MOLA algorithm and those of other rival methods along with other studies. Finally, for the performance analysis of Pareto indexes and runtime of MOLA with other assumed algorithms for the best run, Table 11 is provided.
### Table 4. Optimal Design of Parameters, Specifications, Objectives, and TOI for MOGA Method

<table>
<thead>
<tr>
<th>MOLA</th>
<th>Pareto-Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wₐλ₁=Wₐλ₂ (µm/µm)</td>
<td>5.104/1.654</td>
</tr>
<tr>
<td>Wₐλ₂=Wₐλ₃ (µm/µm)</td>
<td>6.8130/0.537</td>
</tr>
<tr>
<td>Wₐλ₃=Wₐλ₄ (µm/µm)</td>
<td>9.221/1.479</td>
</tr>
<tr>
<td>Wₐλ₄=Wₐλ₅ (µm/µm)</td>
<td>25.988/0.735</td>
</tr>
<tr>
<td>Wₑλ₅ (µm/µm)</td>
<td>12.071/0.797</td>
</tr>
<tr>
<td>Cₑ (pF)</td>
<td>7.831</td>
</tr>
<tr>
<td>Cₑ (pF)</td>
<td>8.868</td>
</tr>
<tr>
<td>Iₑₑₑ (mA)</td>
<td>20.037</td>
</tr>
<tr>
<td>DC gain (dB)</td>
<td>72.751</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>2.110</td>
</tr>
<tr>
<td>Phase Margin (deg)</td>
<td>50.596</td>
</tr>
<tr>
<td>Slew Rate (V/µs)</td>
<td>3.017</td>
</tr>
<tr>
<td>Output Swing (V)</td>
<td>2.306</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>104.156</td>
</tr>
<tr>
<td>PSRR dB</td>
<td>82.822</td>
</tr>
<tr>
<td>TOI</td>
<td>0.0526</td>
</tr>
<tr>
<td>Area (µm²)</td>
<td>80.199</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>0.562</td>
</tr>
<tr>
<td>PSRR dB</td>
<td>82.892</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Parameters</td>
</tr>
<tr>
<td>New Iterations</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MOGA</th>
<th>Pareto-Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wₐλ₁=Wₐλ₂ (µm/µm)</td>
<td>6.869/1.62</td>
</tr>
<tr>
<td>Wₐλ₂=Wₐλ₃ (µm/µm)</td>
<td>27.493/1.63</td>
</tr>
<tr>
<td>Wₐλ₃=Wₐλ₄ (µm/µm)</td>
<td>19.379/1.47</td>
</tr>
<tr>
<td>Wₐλ₄=Wₐ₅ (µm/µm)</td>
<td>32.485/0.311</td>
</tr>
<tr>
<td>Wₑλ₅ (µm/µm)</td>
<td>30.681/1.824</td>
</tr>
<tr>
<td>Cₑ (pF)</td>
<td>5.397</td>
</tr>
<tr>
<td>Cₑ (pF)</td>
<td>10.163</td>
</tr>
<tr>
<td>Iₑₑₑ (mA)</td>
<td>20</td>
</tr>
<tr>
<td>DC gain (dB)</td>
<td>74.121</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>3.311</td>
</tr>
<tr>
<td>Phase Margin (deg)</td>
<td>50.274</td>
</tr>
<tr>
<td>Slew Rate (V/µs)</td>
<td>4.095</td>
</tr>
<tr>
<td>Output Swing (V)</td>
<td>2.355</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>80.3413</td>
</tr>
<tr>
<td>PSRR dB</td>
<td>77.867</td>
</tr>
<tr>
<td>TOI</td>
<td>0.1778</td>
</tr>
<tr>
<td>Area (µm²)</td>
<td>234.0919</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>0.573</td>
</tr>
</tbody>
</table>

### Table 5. Optimal Design of Parameters, Specifications, Objectives, and TOI for MOGWO Algorithm

<table>
<thead>
<tr>
<th>MOGWO</th>
<th>Pareto-Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wₐλ₁=Wₐλ₂ (µm/µm)</td>
<td>5.104/1.654</td>
</tr>
<tr>
<td>Wₐλ₂=Wₐ₃ (µm/µm)</td>
<td>6.8130/0.537</td>
</tr>
<tr>
<td>Wₐλ₃=Wₐ₄ (µm/µm)</td>
<td>9.221/1.479</td>
</tr>
<tr>
<td>Wₐλ₄=Wₐ₅ (µm/µm)</td>
<td>25.988/0.735</td>
</tr>
<tr>
<td>Wₑλ₅ (µm/µm)</td>
<td>12.071/0.797</td>
</tr>
<tr>
<td>Cₑ (pF)</td>
<td>7.831</td>
</tr>
<tr>
<td>Cₑ (pF)</td>
<td>8.868</td>
</tr>
<tr>
<td>Iₑₑₑ (mA)</td>
<td>20.037</td>
</tr>
<tr>
<td>DC gain (dB)</td>
<td>72.751</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>2.110</td>
</tr>
<tr>
<td>Phase Margin (deg)</td>
<td>50.596</td>
</tr>
<tr>
<td>Slew Rate (V/µs)</td>
<td>3.017</td>
</tr>
<tr>
<td>Output Swing (V)</td>
<td>2.306</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>104.156</td>
</tr>
<tr>
<td>PSRR dB</td>
<td>82.822</td>
</tr>
<tr>
<td>TOI</td>
<td>0.0526</td>
</tr>
<tr>
<td>Area (µm²)</td>
<td>80.199</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>0.562</td>
</tr>
<tr>
<td>PSRR dB</td>
<td>82.892</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Parameters</td>
</tr>
<tr>
<td>New Iterations</td>
</tr>
</tbody>
</table>

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication in an issue of the journal.
### Table 6. Optimal Design of Parameters, Specifications, Objectives, and TOI for MOIPO Algorithm

<table>
<thead>
<tr>
<th>MOIPO Pareto-Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
<tr>
<td>Design Parameters</td>
</tr>
<tr>
<td>Area (µm²)</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
</tr>
<tr>
<td>DC gain (dB)</td>
</tr>
<tr>
<td>GBW (MHz)</td>
</tr>
<tr>
<td>C (pF)</td>
</tr>
<tr>
<td>Design Specifications</td>
</tr>
<tr>
<td>Area (µm²)</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
</tr>
<tr>
<td>TOI</td>
</tr>
</tbody>
</table>

### Table 7. Optimal Design of Parameters, Specifications, Objectives, and TOI for MOPSO Algorithm

<table>
<thead>
<tr>
<th>MOPSO Pareto-Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
<tr>
<td>Design Parameters</td>
</tr>
<tr>
<td>Area (µm²)</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
</tr>
<tr>
<td>DC gain (dB)</td>
</tr>
<tr>
<td>GBW (MHz)</td>
</tr>
<tr>
<td>C (pF)</td>
</tr>
<tr>
<td>Design Specifications</td>
</tr>
<tr>
<td>Area (µm²)</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
</tr>
<tr>
<td>TOI</td>
</tr>
</tbody>
</table>
Table 8. **OPTIMAL DESIGN OF PARAMETERS, SPECIFICATIONS, OBJECTIVES, AND TOI FOR NSGA-II ALGORITHM**

<table>
<thead>
<tr>
<th>Design Parameters</th>
<th>NSGA-II</th>
<th>Pareto-Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W_{L1} = W_{L2} ) (µm)</td>
<td>10.143/1.046</td>
<td>12.080/1.853</td>
</tr>
<tr>
<td>( W_{L1} = W_{L2} ) (µm)</td>
<td>16.988/0.908</td>
<td>24.704/0.908</td>
</tr>
<tr>
<td>( W_{L1} = W_{L2} ) (µm)</td>
<td>16.164/0.701</td>
<td>16.196/0.779</td>
</tr>
<tr>
<td>( W_{L1} = W_{L2} ) (µm)</td>
<td>29.756/0.324</td>
<td>29.750/0.325</td>
</tr>
<tr>
<td>( W_{L1} = W_{L2} ) (µm)</td>
<td>33.364/0.437</td>
<td>33.364/0.437</td>
</tr>
<tr>
<td>Cc (pF)</td>
<td>11.246</td>
<td>10.948</td>
</tr>
<tr>
<td>Gl (µF)</td>
<td>13.053</td>
<td>10.135</td>
</tr>
<tr>
<td>( I_{bc} ) (µA)</td>
<td>21.4758</td>
<td>20.8225</td>
</tr>
<tr>
<td>DC gain (dB)</td>
<td>70.382</td>
<td>71.024</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>2.511</td>
<td>2.205</td>
</tr>
<tr>
<td>Phase Margin (deg)</td>
<td>57.922</td>
<td>58.471</td>
</tr>
<tr>
<td>Slew Rate (V/us)</td>
<td>2.318</td>
<td>2.160</td>
</tr>
<tr>
<td>Output Swing (V)</td>
<td>2.412</td>
<td>2.413</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>77.201</td>
<td>108.906</td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td>76.172</td>
<td>76.403</td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td>58.421</td>
<td>81.494</td>
</tr>
</tbody>
</table>

Table 9. **STATISTICAL COMPARISON OF OBJECTIVE VALUES AND TOI OF THE METHODS**

<table>
<thead>
<tr>
<th>Methods</th>
<th>NSGA-II</th>
<th>MOPSO</th>
<th>MOIPO</th>
<th>MOGWO</th>
<th>MOLA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (µm²)</td>
<td>99.042</td>
<td>167.392</td>
<td>115.943</td>
<td>158.843</td>
<td>110.401</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>0.353</td>
<td>0.583</td>
<td>0.693</td>
<td>0.697</td>
<td>0.1075</td>
</tr>
<tr>
<td>TOI</td>
<td>0.1075</td>
<td>0.1212</td>
<td>0.1030</td>
<td>0.1163</td>
<td>0.1086</td>
</tr>
<tr>
<td>Best</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area</td>
<td>99.042</td>
<td>100.286</td>
<td>122.1317</td>
<td>85.8733</td>
<td>72.825</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>0.353</td>
<td>0.566</td>
<td>0.748</td>
<td>0.573</td>
<td>0.560</td>
</tr>
<tr>
<td>TOI</td>
<td>0.1075</td>
<td>0.0975</td>
<td>0.1451</td>
<td>0.0710</td>
<td>0.0526</td>
</tr>
<tr>
<td>Worst</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area</td>
<td>167.392</td>
<td>157.572</td>
<td>155.261</td>
<td>234.091</td>
<td>81.563</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>0.353</td>
<td>1.180</td>
<td>0.940</td>
<td>0.674</td>
<td>0.650</td>
</tr>
<tr>
<td>TOI</td>
<td>0.1075</td>
<td>0.2037</td>
<td>0.1606</td>
<td>0.1778</td>
<td>0.0157</td>
</tr>
<tr>
<td>Mean</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area</td>
<td>125.875</td>
<td>131.656</td>
<td>147.807</td>
<td>112.583</td>
<td>75.499</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>0.686</td>
<td>0.861</td>
<td>0.811</td>
<td>0.614</td>
<td>0.625</td>
</tr>
<tr>
<td>TOI</td>
<td>0.1081</td>
<td>0.1280</td>
<td>0.1526</td>
<td>0.0879</td>
<td>0.0585</td>
</tr>
<tr>
<td>Variance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area</td>
<td>536.942</td>
<td>341.846</td>
<td>159.312</td>
<td>1783.500</td>
<td>6.663</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>0.008</td>
<td>0.179</td>
<td>0.004</td>
<td>9.6333E-04</td>
<td>8.5793E-04</td>
</tr>
<tr>
<td>TOI</td>
<td>2.9815E-05</td>
<td>0.0019</td>
<td>2.0063E-05</td>
<td>2.9418E-04</td>
<td>1.7106E-06</td>
</tr>
</tbody>
</table>

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Fig. 9. Pareto-front of the proposed methods

Fig. 10. Bode diagram plotted by the proposed methods
Fig. 11. Positive PSRR of plotted by the proposed methods

Fig. 12. Negative PSRR of plotted by the proposed methods

Fig. 13. Slew Rate of plotted by the proposed methods
### Table 10. COMPARE THE BEST RESULTS WITH PREVIOUS WORKS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>References</th>
<th>Present work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (µm)</td>
<td>0.35</td>
<td>0.25</td>
</tr>
<tr>
<td>DC gain (dB)</td>
<td>75.43</td>
<td>70.441</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>5.776</td>
<td>2.017</td>
</tr>
<tr>
<td>Phase Margin (deg)</td>
<td>66.2</td>
<td>50.181</td>
</tr>
<tr>
<td>slew Rate (V/µs)</td>
<td>10.88</td>
<td>2.231</td>
</tr>
<tr>
<td>Output Swing (V)</td>
<td>-</td>
<td>2.415</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>87</td>
<td>88.187</td>
</tr>
<tr>
<td>PSRR+ (dB)</td>
<td>83.2</td>
<td>72.675</td>
</tr>
<tr>
<td>PSRR- (dB)</td>
<td>110.4</td>
<td>131.910</td>
</tr>
<tr>
<td>Area (µm²)</td>
<td>109.6</td>
<td>210.003</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
<td>0.713</td>
<td>0.701</td>
</tr>
<tr>
<td>TOI</td>
<td>0.1330</td>
<td>0.3908</td>
</tr>
</tbody>
</table>

### Table 11. PARETO AND TIMING PERFORMANCE ANALYSIS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>NSGA-II</th>
<th>MOPSO</th>
<th>MOIPO</th>
<th>MOGWO</th>
<th>MOLA</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP</td>
<td>21.695</td>
<td>27.155</td>
<td>6.197</td>
<td>6.666</td>
<td>0.9305</td>
</tr>
<tr>
<td>ONVG</td>
<td>20</td>
<td>7</td>
<td>16</td>
<td>11</td>
<td>20</td>
</tr>
<tr>
<td>TIME (s)</td>
<td>1248</td>
<td>1456</td>
<td>1356.2</td>
<td>1356.2</td>
<td>1188.86</td>
</tr>
</tbody>
</table>

### 5. Conclusions

In this paper, for the first time, the workability of learning automata verified in the optimal design of analog circuits. The circuit was a two-stage CMOS op-amp as a challenging and complex engineering problem. The optimized circuit provided the following features: simultaneous optimization of area and power consumption, minimizing the TOI, satisfies of design characteristics. The performance of the proposed MOLA method with four rival optimization algorithms NSGA-II, MOPSO, MOIPO, and MOGWO on designed circuit have been investigated comprehensively. Results obtained by MOLA shown the significant improvement of the desired features in terms of the best Pareto-fronts along with suitable evaluation criteria. As a future work we will apply the proposed methodology to optimize more complex analog and digital circuits with particular design
specifications. Also, optimization algorithms and reinforcement learning methods can be combined to make the circuit more efficiently.

References


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