

Low-Power Adder Design for Nano-Scale CMOS

(Short Paper)

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Abstract: A fast low-power 1-bit full adder circuit suitable for nano-scale CMOS implementation is presented. Out of the three modules in a common full-adder circuit, we have replaced one with a new design, and optimized another one, all with the goal to reduce the static power consumption. The design has been simulated and evaluated using the 65 nm PTM models.

Keywords: Nano-Scale CMOS Technology, Static Power Consumption, Adder Subcomponents.

1 Introduction

Adders are important building blocks in arithmetic units [1]. Therefore, any optimization of their speed and power consumption can have considerable impact on power efficiency and speed of the overall system. Some of the classical designs of 1-bit full adder circuits use standard static CMOS and complementary pass-transistor logic circuits [2]. There are some new designs and optimizations on full adder circuits for deep submicron technology [3-7] however they focus on 0.18 or 0.35- μm CMOS technology. These designs have better performance than classical designs, especially those presented in [6] and [7]. Therefore any new design should normally be compared to these new designs.

The migration towards deep submicron technologies has drastically changed the face of low-power design. The static leakage current is now a significant component of the overall power consumption. As a result, special attention must be paid to minimizing the static power. Therefore, in this paper the focus is on static power consumption and suitable techniques are used to reduce leakage power consumption.

It is shown that by placing more than one transistor serially, the static power consumption will be decreased [8]. In this paper, this technique will be used effectively to decrease the leakage power consumption of the 1-bit full adder circuit. Here the focus is on deep sub-micrometer technology, therefore only the optimized versions of 1-bit full adder circuit sub-components specially from leakage power consumption point of view are presented.

2 Adder Subcomponents

A 1-bit full adder can be divided into three main modules [3-7]. This work can be done by extracting the logical equation of 1bit-full adder circuit. Equations (1) and (2) show the logical equations of the full adder outputs.

$$Sum = A \oplus B \oplus C \quad (1)$$

$$C_{out} = A \cdot B + C_{in} \cdot (A \oplus B) \quad (2)$$

By considering H as the XOR of A and B signals the output logical equations changed to Eq. (3) and Eq. (4).

$$Sum = H \oplus C_{in} = H \cdot C'_{in} + H' \cdot C_{in} \quad (3)$$

$$C_{out} = A \cdot H' + C_{in} \cdot H \quad (4)$$

These equations show that the three main part subcomponents of the full adder circuit. The main part of them is an XOR/XNOR circuit that produces the H and H' signals. The other parts are XOR and MUX circuits that work with respect to the Eq. (3) and Eq. (4). The XOR circuit is really a MUX circuit that selects H and H' signals by C_{in} . Then subcomponent II can be implemented by MUX. Fig. 1 shows the full adder circuit subcomponents. The goal is to design modules that minimize the static power consumption while providing enough drive current for the next stages. This can be done by disallowing too few transistors to exist in the path from the power supply to ground. We do an optimization on module I and present a new circuit on module II.

3 Optimization of Module I

Fig. 2 shows the common designs for module I [3-7]. Circuit (c) from [7] has potentially high static power

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consumption at deep submicron because it uses an inverter. In inverter, there is a direct path between power supply and ground with only two transistors. Therefore, inverter is one of the high static power elements. Circuit (a) from [6] does not have sufficient speed and drive power compared to the alternative designs. On the other hand, circuit (b) is an enhanced version of circuit (a) with the following additions: 2 PMOS transistors to increase its speed when the inputs are "00" and 2 NMOS transistors to increase its speed when the inputs are "11" [7]. But this circuit needs larger area. The delay in the "00" case is larger than the "11" case because two PMOS transistors must work, but in case "11" in which two NMOS transistors work. Therefore, the transistors N3 and N4 can be removed. This idea is implemented in circuit (d).

Table 1 shows the HSPICE simulation results for 65nm PTM (Predictive Technology Model) models [9]. The parameter PDP is the power delay product, and the parameter $power^2 \times delay$ is shown to emphasize the power consumption. The power consumption of our optimized circuit is lower than other circuits and its performance is medium. Thus we maintain speed while reducing power consumption. The leakage power consumption (*Leakage Power*) that is presented here is obtained by .op instruction of HSPICE when all inputs are in low logic. The signals frequency of all simulated circuits is 2 GHz and the capacitive load of the outputs is set to 2 fF suggested by the ITRS technology roadmap [10]. Although the gate capacitance is very small but the interconnection capacitance is considerable in nano-meter technologies.

According to Table 1 the leakage power consumption of module I has at least 7% improvement in comparison to the proposed circuit that is presented in [7]. The test configurations as well as the waveforms for the simulation are shown Fig. 3.

Table 1. Module I HSPICE simulation results at 65 nm, $V_{dd}=1.1$ V, $C_L=2$ fF

65 nm Tech.	Comparison of Main Circuits for Module I		
	Circuit (b)	Circuit (c)	Optimized circuit
No. of Tr.	10	8	8
Leakage Power (nW)	135.8	146.9	135.8
Power (μW)	38.498	37.317	36.973
Delay (ps)	39.051	60.227	36.677
PDP (fJ)	1.5033	2.2474	1.3560
$Power^2 \times Delay$	57.8740	83.8662	50.1353

4 Design of Module II

Two of the most common circuits for module II are shown in Fig. 4(a) and Fig. 4(b) [3-7]. However, these circuits are not suitably optimized for deep submicron

CMOS technology. Circuit (a) lacks sufficient drive current at the output and Circuit (b) uses an inverter at its output in order to increase drive current, but this also increases its static power consumption due to the direct path between V_{DD} and GND.

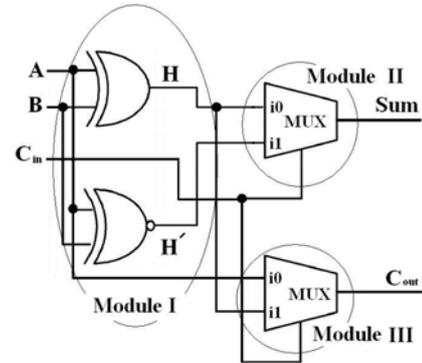


Fig. 1. Subcomponents of a 1-bit full adder

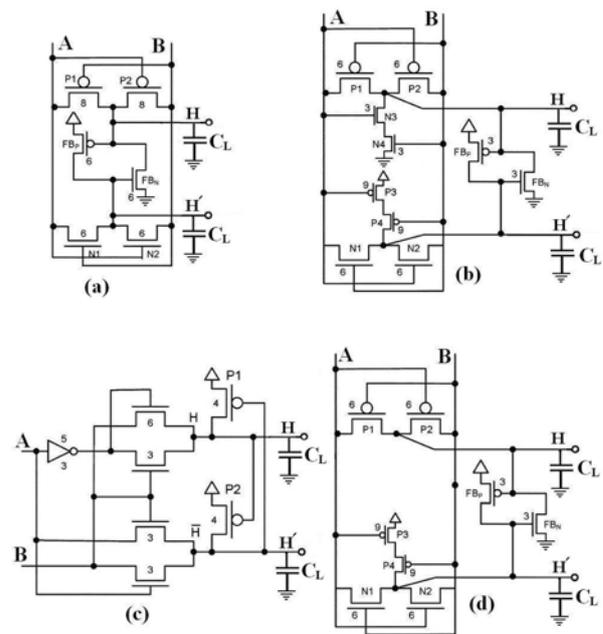


Fig. 2. (a) Circuit in [4-5] (b) circuit in [6] (c) circuit in [7] (d) optimized circuit

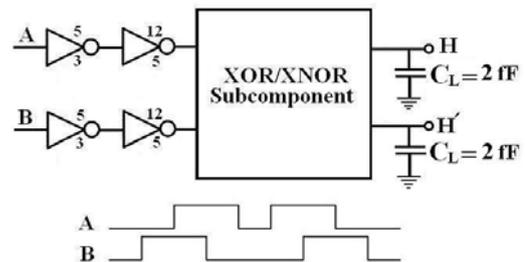


Fig. 3. Simulation configuration for module I

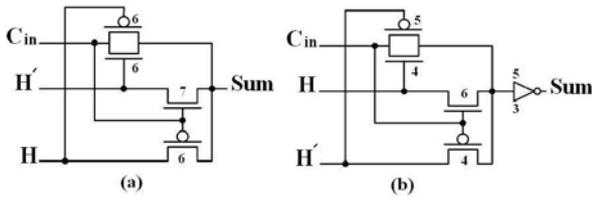


Fig. 4. Commonly used circuits for module II. (a), (b) [3-7]

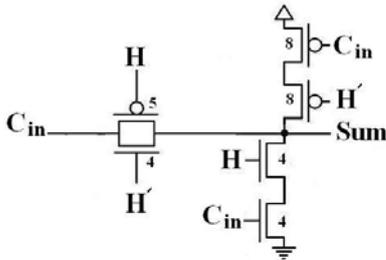


Fig. 5. Proposed circuit for module II

Table 2. Module II HSPICE simulation results at 65 nm, $V_{dd}=1.1$ V, $C_I=2$ fF

65 nm Tech.	Comparison of Main Circuits for Module II		
	Circuit (a)	Circuit (b)	Proposed circuit
No. of Tr.	4	6	6
Leakage Power (nW)	121.0	148.5	108.1
Power (μ W)	23.933	24.609	23.09
Delay (ps)	27.136	42.338	29.821
PDP (fJ)	0.6494	1.0418	0.6885
Power ² ×Delay	15.5420	25.6376	15.8974

At first we propose a useful method for reducing the static power consumption. The main reason for static power consumption is leakage current. On the other hand, it is shown that by placing more than one transistor serially, the leakage current will be decreased [8]. Therefore this technique can reduce static power consumption. However, too many serial transistors can reduce speed and increase dynamic power consumption. Therefore we must select the proper number of serial transistors.

Our proposed circuit, shown in Fig. 5, uses only two serial transistors. These extra transistors in the path from V_{DD} to ground help to decrease the overall static power consumption in deep submicron technology and implement the logical equation for producing the *SUM* output. This circuit also eliminates the drawbacks in previous designs. In this circuit, the input *H* is the selector; if $H = 0$ then $sum = C_{in}$, otherwise $sum = H.C_{in}$.

We performed HSPICE simulations using the PTM 65 nm technology models, and compared the

performance of our proposed circuit to those of the two commonly-used circuits shown in Fig. 4(a) and Fig. 4(b). The simulation test setup is like as module I. The simulation results are shown in Table 2. Both power consumption and delay time show very good improvement in comparison with the circuit in Fig. 4(b). The delay in this new circuit is more than the circuit in Fig. 4(a). The increased delay is a result of increased serial transistors in our circuit. Leakage power consumption of this new circuit shows very good improvement in comparison with other circuits.

5 Simulation Results

Now with these newly designed subcomponents we can have a new design for 1-bit full adder. We select the module III, which is presented in [7] to form this new 1-bit full adder circuit. Fig. 6 shows this new full adder circuit. The test configuration of this circuit is the same as the one used in [7].

This new circuit is compared to another full adder circuits that used from hybrid-CMOS logic style for 1-bit full adder cells [5-7]. Hybrid-CMOS logic style is suitable for deep submicron technology. However the circuits that are proposed up to now are simulated in 0.18 μ m CMOS technology. Our simulation is done in 65 nm PTM technology model with 1.1 V power supply. The capacitive load (like the test setup of module I) is selected to be 2 fF. Fig. 7 shows the full adder circuit which is presented in [7]. The simulation test setup circuit is the same as the one that is used in [7]. As shown in Table 3, there is at least 21% improvement in the overall performance (Power-Delay Product, *PDP*) of the circuit, because both delay and power consumption are reduced. This new full adder circuit has at least 11% improvement in leakage power consumption in comparison with the other circuits.

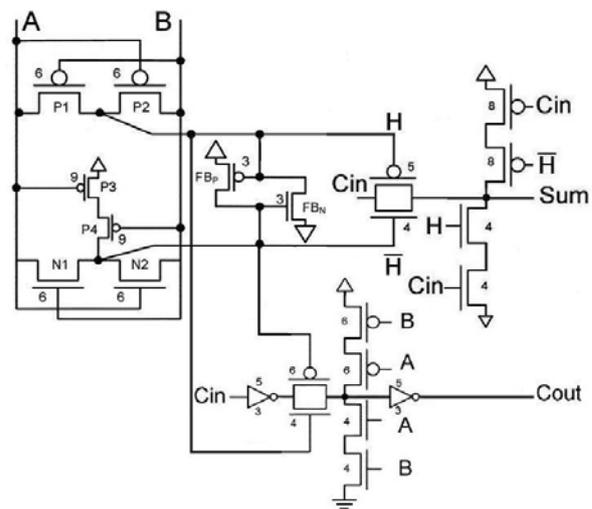


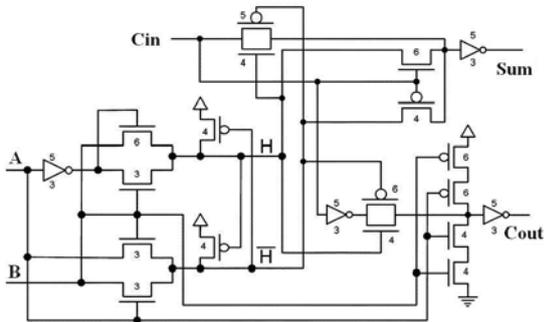
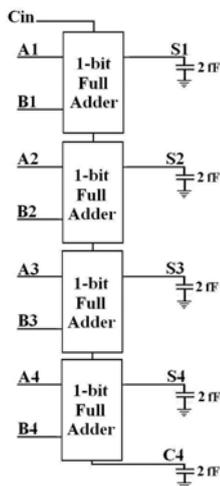
Fig. 6. Proposed 1-bit full adder circuit

Table 3. Full adder HSPICE simulation results at 65 nm, $V_{dd}=1.1$ V, $C_l=2$ fF

65 nm Tech.	Comparison of full adder Circuits			
	Full adder in [5]	Full adder in [6]	Full adder in [7]	Proposed full adder
Leakage Power (nW)	263.2	259.0	281.8	230.3
Power (μW)	93.310	64.039	60.984	63.005
Delay (ps)	133.33	76.88	92.394	61.63
PDP (fJ)	12.4410	4.9233	5.6345	3.8829
Power ² ×Delay	1160.86	315.28	343.61	224.64

Table 4. 4-bit full adder HSPICE simulation results at 65 nm, $V_{dd}=1.1$ V, $C_l=2$ Ff

65 nm Tech.	Comparison of 4-bit full adder Circuits			
	4-bit full adder composed from the adder in[5]	4-bit full adder composed from the adder in[6]	4-bit full adder composed from the adder in[7]	4-bit full adder from the proposed adder
Leakage Power (nW)	536.6	519.7	610.9	405.1
Power (mW)	0.13757	0.13726	0.15333	0.13092
Delay (ps)	148.91	188.29	198.08	169.52
PDP (fJ)	20.4855	25.8446	30.3716	22.1935
Power ² ×Delay	2.8181	3.5474	4.6568	2.9055

**Fig. 7.** Full adder circuit proposed in [7]**Fig. 8.** 4-bit Full adder Test Circuit

6 Adder Chaining

We used our optimized 1-bit full adder in a carry-ripple 4-bit full adder circuit to evaluate it in a realistic operating condition. The 4-bit full adder test circuit is shown in Fig. 8 and the results are presented in Table 4. As shown in Table 4, there is at least 22% improvement in leakage power consumption in comparison with other circuits. This is completely compatible to the main goal of this paper, i.e., its suitability in nano-scale CMOS technology. This goal can be achieved by low leakage power design which is done here. Also there is at least 5% improvement in overall power consumption of our proposed circuit.

7 Conclusion

We present a new design for a 1-bit full adder circuit by optimizing its subcomponents for leakage current reduction. The simulation results show that the adder is suitable for application in ultra deep submicron CMOS technologies. The proposed full adder circuit has acceptable performance in 65nm CMOS technology.

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