A Low-Voltage, Low-Power, Two-Stage Amplifier for Switched-Capacitor Applications in 90 nm CMOS Process

S. H. Mirhosseini* and A. Ayatollahi*

Abstract: A novel low-voltage two-stage operational amplifier employing resistive biasing is presented. This amplifier implements neutralization and correction common mode stability in second stage while employs capacitive dc level shifter and coupling between two stages. The structure reduces the power consumption and increases output voltage swing. The compensation is performed by simple miller method. For each stage an independent common-mode feedback circuits has been used. Simulation results show that power consumption is 2.1 mW at 1 V supply. The dc gain of the amplifier is about 70 dB while its output swing is as high as around 1.2 V.

Keywords: Common-Mode Feedback (CMFB), Switched Capacitor (SC), Operational Transconductance Amplifier (OTA), Operational Amplifier (Op-Amp).

1 Introduction

Rapid growing in technology and science has forced electronic engineers to implement deep submicron technologies in order to enhance the speed and lower the power consumption. The main challenges to achieve these requirements are voltage limitation, noise performance and power reduction.

One of the main elements implemented in the circuits such as data converters, filters and switched capacitor (SC) is operational amplifier (OP-AMP). There are several structures of OP-AMPs but only a few of them are suitable for use in deep submicron processes where low power consumption is a main requirement.

As the high precision in the most applications translates to high gain, so obtaining high gain is of great importance. The first challenge in providing high gain is the small voltage of supply which limits the cascode topology to have enough output voltage swing. Therefore the use of this topology in output stage is not suitable. In addition the small voltage swing decreases the signal to noise ratio of the amplifier [1]. The second problem in the deep submicron process is small transistor's output resistance. In order to increase this resistance one should decrease the bias current of transistor which in turn reduces the speed. Another solution to overcome to the problem is implementing gain boosting [2] to enhance gain in a high speed circuit [3]. To achieve high gain, at least, two cascaded stages are required. Using multi-stages amplifiers (more than two) creates several low frequency poles which decreases the speed of the amplifier and increases power consumption. Implementing common-mode feedback (CMFB) circuit in two stages OP-AMP is another important issue in low voltage applications. To have good common mode stability, two local common-mode feedback sub-circuits are required to regulate the output voltage of each stage [4] since a single-loop common-mode feedback is unstable in two stages OTA. Local common-mode feedback also increases power dissipation. The maximum output swing decreases if the common mode voltage is variable.

Process parameters variations in deep submicron processes are large which limits the optimum design [5]. It is supposed that the best choice for a high gain and high swing circuit with low power consumption is two-stage operational amplifier whose first stage is folded-cascode amplifier [6]. The first stage provides large gain and has a small output swing voltage while the second stage produces a low gain and a high swing voltage. Also, the second stage plays an important role in frequency compensation of amplifier. Although this choice has good advantages for designer, it has some drawbacks.

Outline of this paper is as follows. In section 2, the structure of a commonly used two-stage op-amp is described. In section 3, proposed structure is described and the simulation results are shown in section 4. Finally, conclusion is presented in section 5.

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2 Common Two-Stage Amplifier

To achieve high gain in low voltage processes, two-stage amplifier topology is a best choice. Folded cascaded differential pair has two main advantages of increasing both the output swing and common mode input range [7]. Thus two-stage operational amplifier with a folded cascode as the first stage has many applications requiring high precision and low supply voltage. This structure is shown in Fig. 1.

The first stage has high gain and low swing and the second stage has low gain and high swing. The dc gain

$$A_{dc}=g_{m1}g_{m11}[(r_{o3}||r_{o1})(1+g_{m5}r_{o5})||r_{o9}(1+g_{m7}r_{o7})](r_{o11}||r_{o13}) \quad (1)$$

where, g_m and r_o is transistor trans-conductance and output resistance respectively.

The voltage swing of the first stage is expressed as:

$$V_{o1swing}=2\times[V_{DD}-(\Delta V_3+\Delta V_5+\Delta V_7+\Delta V_9)] \quad (2)$$

where, ΔV is overdrive-voltage of related transistor. This stage is used for compensation and amplification as well. The gain is miller multiplication coefficient for the compensation capacitor. It is obvious that using multi-stages amplifies has many advantages. These amplifies have high gain and high output voltage swing, however, their speed is less than that of the one stage amplifiers such as cascode, folded cascode or telescopic amplifiers [8]. In addition, these amplifiers consume more power. Furthermore, the two-stage amplifiers require two common mode feedback circuits.

All mentioned drawbacks are important; however as two-stage amplifier is used in a low voltage process such as 90nm CMOS, some drawbacks are more important. If the second stage is connected directly to the first stage, the output voltage swing will be:

$$V_{outswing}=2\times\left(V_D-\left(V_{out1_{bias}}-V_{th11}\right)\right) \quad (3)$$

where, $V_{out\,swing}$ is output voltage swing of amplifier, $V_{out1_{bias}}$ and V_{th11} is output dc voltage of first stage and threshold voltage of M_{11} respectively**.** Cascoding transistors in the first stage's output results in a high value of $V_{out1_{bias}}$. So swing of second stage output is limited for a low voltage application [9].

3 Proposed Amplifier

In request to a voltage level shifter which increases the voltage swing of second stage, a capacitive level shifter is preferred to source follower for its lower power consumption. However for this structure it is required to charge the coupling capacitor with an appropriate and constant voltage. To do this, the capacitor is connected to a constant voltage during common mode adjusting time. This coupling capacitor is placed between first stage's output and second stage's input as shown in Fig. 2. In this figure, the dc voltage of capacitor affects the bias of second stage.

As it mentioned above, the coupling capacitor is charged in common mode adjusting time. In this time, top plate is charged with first stage CMFB and bottom plate is charged to V_B. As it is shown in Fig. 1, two switches, two resistors and input transistor of second stage determine the voltage of capacitor's bottom plate. When the op-amp is in common mode adjusting period, the transistor's drain current is given by:

$$I_D=\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_B-V_{th})^2 \quad (4)$$

where, μ_n is electron mobility, C_{ox} and $\frac{W}{L}$ is gate oxide capacitance of transistor and aspect ratio respectively and V_B is the voltage between two resistors. It is known that the drain current of output transistor is fixed by the bias circuit, so V_B is to be charged with respect to bias voltage. This is done by two resistors.A large coupling capacitance connected to node B is another important issue which needs special consideration. In this case, the bias of node B is fixed in a long time constant due to high resistors R_{b1} and R_{b2}. However this is done once in startup time of amplifier. It can be easily shown that the output dc voltage is:

$$V_{o,DC}=\frac{R_{b1}+R_{b2}}{R_{b1}}V_B. \quad (5)$$

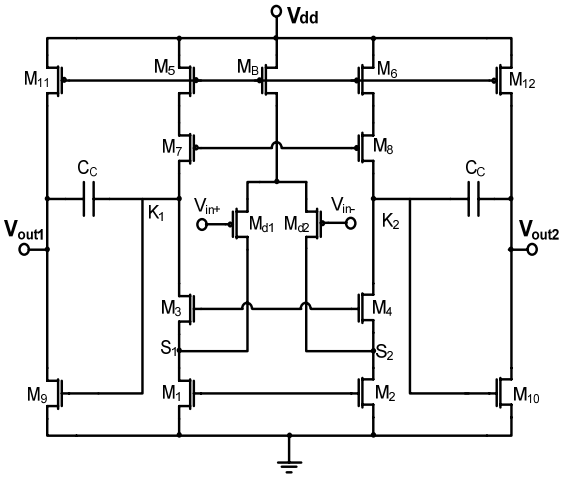

Fig. 1 Two-stage Miller compensated operational transconductance with folded first stage.

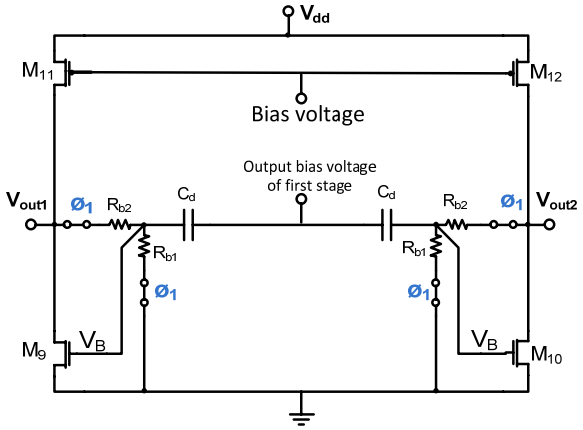

Fig. 2 Capacitive coupling between two stages amplifier and 2'nd stage CMFB.

It means that the dc output voltage is proportional to VB**.** It is clear that this structure acts as second stage CMFB**.** Using this simple structure has two main advantages. Firstly, in contrast to the conventional switched capacitors which use capacitive CMFBs and therefore occupies large area, this simple CMFB does not use capacitor. Secondly, this CMFB charges the coupling capacitors which are used as a level shifter with appropriate voltage.

Although the above topology has many advantages which were explained but it has many drawbacks. The first drawback is that only the fraction of the first stage output is amplified by the second stage. This is due to this fact that there is a miller capacitance between second stage input and output. So:

$$v_b = \frac{C_{coupling}}{C_{coupling}+C_p} \times v_{o_{stage1}} \quad (6)$$

where C_p is given by:

$$C_p \approx C_{gs_{9,10}} + g_{mo_{9,10}} R_L C_{gd_{9,10}} \quad (7)$$

and $C_{coupling}$ is coupling capacitor. This decreases the amplifier gain by factor of $\frac{C_{coupling}}{C_{coupling}+C_p}$. Since the gain of two-stage amplifier implemented in 90nm CMOS process is limited to about 70dB, it is necessary to eliminate the effect of miller capacitor. The best solution is to use neutralization method as it is shown in Fig. 3.

The second drawback is produced by simple second stage CMFB since this simple CMFB works only in small period of common mode adjusting period. The half-circuit part of amplifier in common mode is shown in Fig. 4. This circuit shows common mode half circuit in amplification phase, C_f and C_s is feedback capacitor respectively. M_D is one of input differential pare transistor, M_C is control transistor in first stage common mode feedback loop and M_o is one of output stage transistor. Careful consideration of this figure shows existence of positive feedback in common mode of amplifier. To stabilize the amplifier in common mode, the common mode loop gain (CMLG) should be less than unity:

$$CMLG = \frac{g_{mo} R_L}{g_{mc} r_{o2}} \leq 1 \quad (8)$$

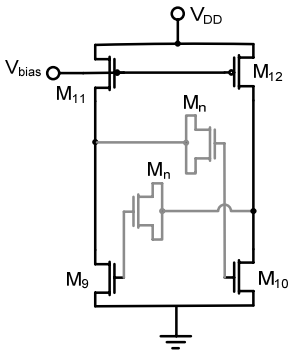

Fig. 3 Use neutralization method for eliminate the effect of Capacitor miller effect.

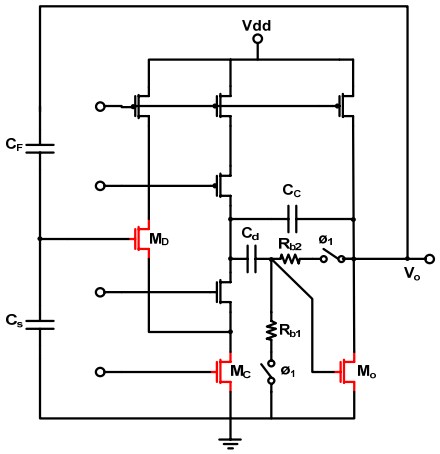

Fig. 4 Common mode half circuit.

In the above equation, g_{mo} is trans-conductance of M_o,$R_L$is output resistance of amplifier while g_{mc} and r_{o2} are trans-conductance and output resistance of M_c, respectively. The loop gain in common mode is around unity, so it is unreliable and should to be reduced to appropriate value. Figure 5 shows the proposed circuit whose loop gain is less than unity.

The widths of transistors are expressed as follows:

$$W_{M_{oc1,2}} = K \times W_{M_{od}} \quad (9\text{-a})$$

$$W_{M_{on1,2}} = \sigma \times W_{M_{c1,2}} \quad (9\text{-b})$$

As can be seen in Fig. 5, two transistors M_{C1} and M_{C2} sample and scale the input transistors' currents of the second stage and feedback their summed into their inputs. So only common mode parts of bias current is fed back to the second stage with no effect on differential mode parts of bias current. It can be proved that:

$$I_o = \frac{I}{\left(1-K\frac{2}{\sigma}\right)} \quad (10\text{-a})$$

$$A_{V_{cm}} = \left(1-K\frac{2}{\sigma}\right) \times \frac{g_{mo} R_L}{g_{mc} r_{o2}} \quad (10\text{-b})$$

where I_o is bias current of stage 2, I is bias current of $M_{op1,2}$ and $A_{V_{cm(stage2)}}$ is common mode gain of second stage. As it is seen in the above equations, the common

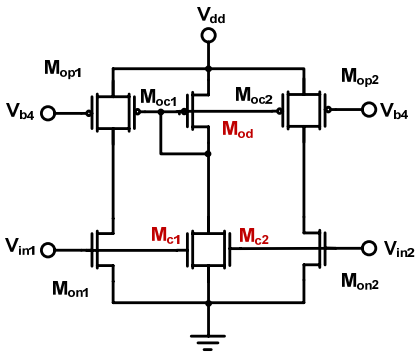

Fig. 5 Proposed circuit for attenuate common mode gain.

mode gain of second stage decreases if $\left(1\text{-}K\frac{2}{\sigma}\right)<1$. Also, for $\sigma \gg 1$ the power consumption of second stage is approximately the same as that of when common structure is used for the second stage.

From (10-b), it can be seen that by applying this new structure and choosing $\left(1\text{-}K\frac{2}{\sigma}\right)<1$, the loop gain of amplifier is less than unity and amplifier is stable in common mode. The final schematic of amplifier is shown in Fig. 6.

4 Citations and References

Figure 7 show the proposed two-stage amplifier in Multiplying-DAC-subtract configuration called MDAC. This circuit is one of most important circuit block in pipelined ADC, where $\emptyset_1$ and $\emptyset_2$ are 100MHz nonoverlap clock, V_{cmi} is input common mode voltage and V_{DAC+} and V_{DAC-} are related to prior stage result.

The simulated results for the amplifier in 90nm CMOS process with 1 V supply as shown in Fig. 7 are presented in Figs. 8 to 11. These results are obtained with HSPICE Ver. 2007.09. The proposed amplifier operates in switched capacitor application as it shown in Fig. 7. The amplifier's dc gain is about 69.6 dB as it is clear from Fig. 9 and its phase margin is around 57.3 degrees at β=1.

As it is seen from Fig. 10, the unity-gain bandwidth is about 416 MHz. It is important to note that the frequency compensation is performed by simple miller method. The common mode gain of amplifier is about 30 dB.The simulated FFT output voltage is presented in Fig. 11. For this amplifier, the SFDR and THD are 73.37 dB and -73.19 dB respectively.

The simulated step response of proposed OPAMP is shown in Fig. 9. The slew rate is about 130 V/us. Table 1 shows the main parameters of the amplifier and comparison with other work.

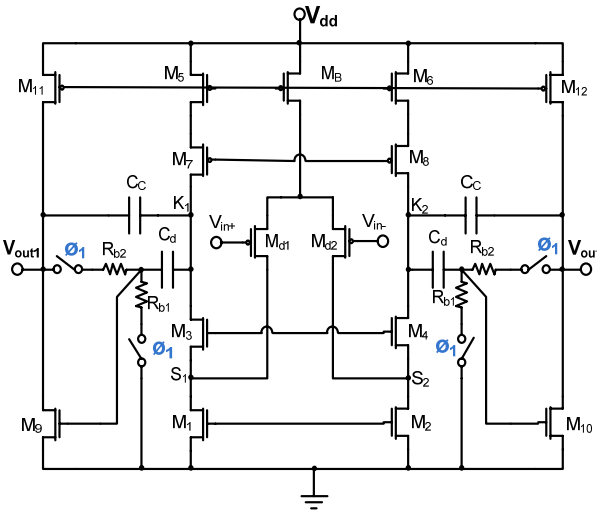

Fig. 6 Final proposed amplifier circuit.

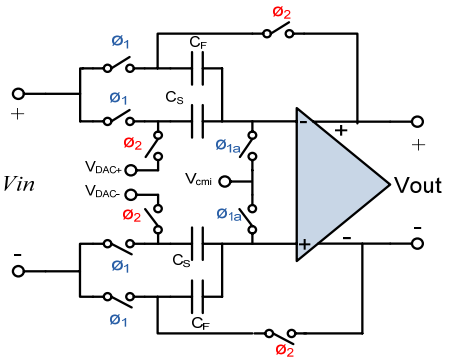

Fig. 7 Switched capacitor circuit MDAC with proposed two stage amplifier.

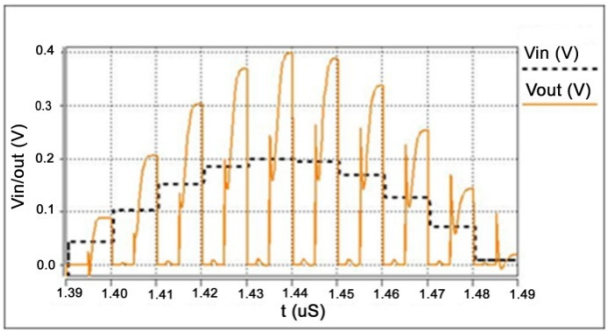

Fig. 8 Gain 2 in switch capacitor application with Latency.

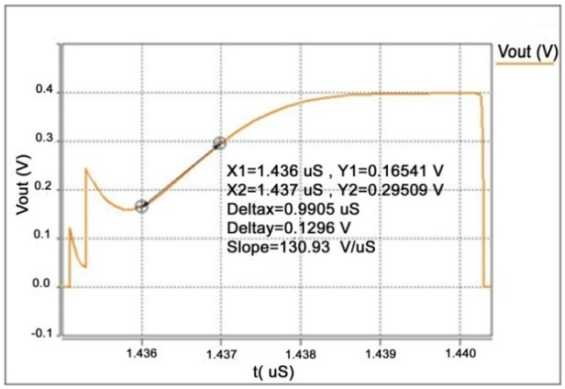

Fig. 9 Simulated op-amp step response (β=0.5).

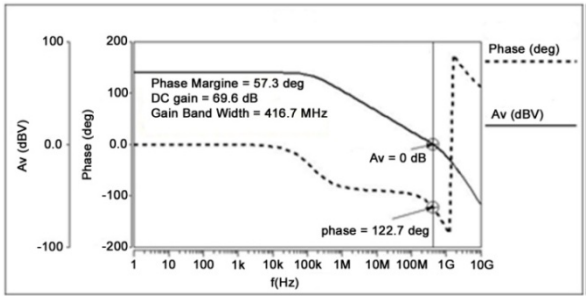

Fig. 10 Frequency response of the proposed OPAMP.

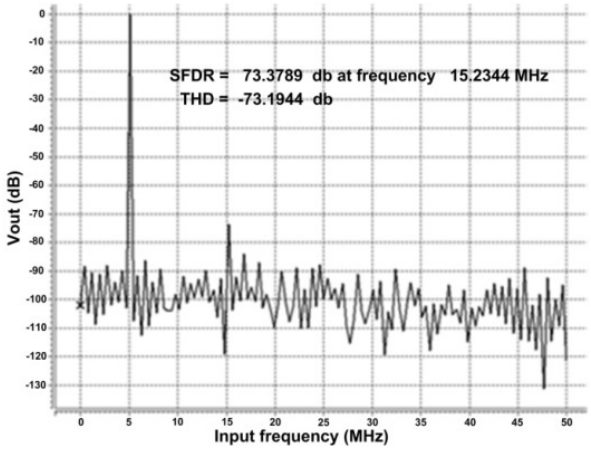

Fig. 11 256 point FFT performance of the Switch capacitor circuit (gain 2) with using proposed op-amp.

Table 1 Performance comparison of different OP-MPs.

Parameter	This work	Ref[10]	Ref[11]	Ref[12]
Process	*90 nm*	*90 nm*	*90 nm*	*180 nm*
Power supply(Vdd)	*1.0 V*	*1.0 V*	*1.2 V*	*1.8 V*
Power Consumption	*2.1 mW*	*34 mW*	*20 mW*	*6mW*
Open loop gain	*69.6 dB*	*74 dB*	*70 dB*	*72.2 dB*
Unity-gain frequency	*416.7 MHz*	*1000 MHz*	*2500 MHz*	*1100 MHz*
Gain margin @1pF(β=1)	*-10 dB*	-	-	-
Phase margin @1pF (β=1)	*57.3°*	-	*60°*	*58°*
Slew Rate	*130 V/us*	-	*2.5 V/ns*	-
Load	*1p F*	-	*300 fF*	*10pF*
Output voltage swing (Vp-p)	*1.2 V*	*1.5 V*	*0.5V*	*2 V*
Input CMR	*0.8 V*	-	-	-
Settling time (0.05%)	*3.8 nS*	-	-	-
SFDR	*73.37 dB*	-	-	-
THD	*-73.19 dB*	-	-	

5 Conclusion

In this paper, a two-stage folded cascode amplifier with 1V supply for use in pipelined ADC in 90 nm CMOS process was presented. It was shown that by employing resistive biasing in second stage and capacitive dc level shifter and with simple miller compensation, the proposed op-amp has large unit-gain bandwidth, good phase margin, fast-settling behavior and large output voltage swing.

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