

Application of Neural Space Mapping for Modeling Ballistic Carbon Nanotube Transistors

R. Yousefi*, K. Saghafi** and M. K. Moravvej-Farshi***

Abstract: In this paper, using the neural space mapping (NSM) concept, we present a SPICE-compatible modeling technique to modify the conventional MOSFET equations, to be suitable for ballistic carbon nanotube transistors (CNTTs). We used the NSM concept in order to correct conventional MOSFET equations so that they could be used for carbon nanotube transistors. To demonstrate the accuracy of our model, we have compared our results with those obtained by using open-source software known as FETToy. This comparison shows that the RMS errors in our calculated I_{DS} , under various conditions, are smaller than the RMS errors in I_{DS} values calculated by the existing analytical models published by others.

Keywords: Carbon Nanotube Field Effect Transistor, Neural Network, Neural Space Mapping.

1 Introduction

Carbon nanotubes (CNTs), with exceptional electronic and optical properties, have become of great interest for future electronic applications. Some of these properties such as symmetric band structure, direct bandgap, and near ballistic transport make them attractive for circuit implementations [1]. Reaching the physical limitation in scaling MOS transistors [2], carbon nanotube field effect transistors (CNTFETs) which can be scaled down to 10nm and shorter are potential candidates for replacing the conventional MOSFETs [3]. Schottky barrier CNTFETs (SB-CNTFETs) and MOSFET-like CNTFETs (MOSCNTs) are the two major alternatives. In a SB-CNTFET, source and drain Schottky contacts are formed on both sides of metal oxides semi-conducting nanotube. By varying the SB height and modulating the gate bias, one can modulate the flow of carriers in the nanotube [4]. MOSCNTs, on the other hand, have channel-dominated behavior. By designing a local gate contact at the channel midpoint, in such

transistors, reduced electrostatic coupling with the metallic contacts can be achieved [5]. While tunneling is the dominant mechanism responsible for current flow in SB-CNTFETs [4], thermionic emission is the dominant mechanism for current flow in MOSCNTs [6].

From a circuit designer's point of view, circuit simulation and evaluation using CNTFETs are challenging because the developed exact models for CNTFETs such as FETToy [6, 7] are mainly numerical, using self-consistent techniques to solve the equations. Hence, the commercially available circuit solvers, such as SPICE [8], cannot benefit from such models. So far, many research works have been devoted to removing the self-consistent loop. Fregonese et al., in their most recent report, have introduced an analytical equation in order to remove the charge integral for increasing simulation speed [9], while some other research groups have introduced analytical models to calculate the potential at the top of the barrier directly [10-16]. Accuracy of these analytical models, however, depends on the biasing conditions and values of the physical parameters used.

In this paper, by using the neural space mapping (NSM) concept [17] we present a SPICE-compatible modeling technique for ballistic carbon nanotube transistors. In this approach, unlike the conventional approach of using a Neural network (NN), we have used NNs in order to modify a known coarse model, such as the conventional MOSFET equations [18], so that the accuracy of the resulting model is such that the ensuing device characteristics are in excellent agreements with

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those obtained by FETToy, for a wide range of gate to source bias voltages, V_{GS} , as well as the values for physical parameters such as the source Fermi level, E_F , tube diameter, d , oxide thickness, t_{ox} . Such an excellent accuracy demonstrates that this method is capable of being applied to any new structure with a well defined coarse model.

2 Modeling

As we have pointed out in Section 1, we are going to compare our results to those obtained from the FETToy which is an exact but not a SPICE compatible model. Hence, we need to briefly introduce its drain current formula, given by [6]:

$$I_{DS} = \frac{4qk_B T}{h} \times \left(\ln \left[1 + \exp \left(\frac{E_F - U_{SCF}}{k_B T} \right) \right] - \ln \left[1 + \exp \left(\frac{E_F - U_{SCF} - qV_{DS}}{k_B T} \right) \right] \right) \quad (1)$$

where q , k_B , T , h , E_F , V_{DS} , and U_{SCF} are electronic charge, the Boltzmann constant, temperature, plank's constant, source Fermi energy level, drain to source bias voltage and the potential energy at the top of the barrier, respectively. The latter, in turn, can be defined in terms of the drain-source and gate-source bias voltages (V_{DS} and V_{GS}), terminal capacitances (C_S , C_D , and C_G), as well as the channel charge densities including the inherent charges, N_0 , and those injected from the source, N_1 , and the drain, N_2 :

$$U_{SCF} = -q \left[\left(\frac{C_D}{C_T} V_{DS} + \frac{C_G}{C_T} V_{GS} \right) + \frac{q(N_1 + N_2 - N_0)}{C_T} \right] \quad (2)$$

where $C_T = C_S + C_D + C_G$ is the total capacitance. The gate capacitance, for a coaxial structure, which is related to transistor physical parameters, is given by [7]:

$$C_G = \frac{2\pi\epsilon_0\epsilon_{ox}}{\ln(1 + 2t_{ox}/d)} \quad (3)$$

where d is the carbon nanotube diameter, and t_{ox} and ϵ_{ox} are the gate oxide thickness and permittivity, respectively. The aforementioned charge densities in Eq. (2) are also given by:

$$N_0 = \frac{8}{3\pi a_{cc} V_{CC}} \int_0^{+\infty} \left[1 + e^{\left(\frac{\sqrt{E^2 + E_B^2} - E_F - E_B}{k_B T} \right)} \right]^{-1} dE \quad (4)$$

$$N_1 = \frac{4}{3\pi a_{cc} V_{CC}} \int_0^{+\infty} \left[1 + e^{\left(\frac{\sqrt{E^2 + E_B^2} + U_{SCF} - E_F - E_B}{k_B T} \right)} \right]^{-1} dE \quad (5)$$

$$N_2 = \frac{4}{3\pi a_{cc} V_{CC}} \int_0^{+\infty} \left[1 + e^{\left(\frac{\sqrt{E^2 + E_B^2} + U_{SCF} + qV_{DS} - E_F - E_B}{k_B T} \right)} \right]^{-1} dE \quad (6)$$

where E_B , is the first conducting band at the mid-gap (i.e. $E_G/2$), and a_{cc} , and V_{CC} are carbon-carbon bond length and energy, respectively. Solving Eq. (2) and Eqs. (4)-(6), iteratively, results in self-consistent solutions for U_{SCF} , which in turn can be used in Eq. (1) for calculating I_{DS} .

After this brief introduction of FETToy model, we present our SPICE compatible analytical model with sufficient accuracy. In this new model, we have modified a well known "level 1" MOSFET model in Spice [18] with Neural Space Mapping (NSM) concept [17]. Unlike conventional neural networks, NSM does not require a large number of data points. Hence, the number of times that one needs to simulate the complicated fine model, for training NNs, reduces considerably. The modified coarse model for the drain current can be written in the general form of:

$$I_{DS} = \begin{cases} K [A V_{DS} V_{DSsat} - B V_{DS}^2] & \text{for } V_{GS} \geq V_{TH} \\ & \text{and } V_{DS} \leq V_{DSsat} \\ K V_{DSsat}^2 \left[1 + \frac{V_{DS} - V_{DSsat}}{V_A} \right] & \text{for } V_{GS} \geq V_{TH} \\ & \text{and } V_{DS} > V_{DSsat} \end{cases} \quad (7)$$

where $V_{DSsat} = V_{GS} - V_{TH}$, K , is assumed constant, V_{TH} , and V_A are the threshold and Early voltages, respectively. In this paper, to be able to fit the model I_{DS} to that of a CNTFET with a nearly linear characteristic in triode region, we had to define A and B such that while the resulting model fits the exact model with a sufficient accuracy, the current and its slope are both continues at $V_{DS} = V_{DSsat}$. For an optimized model A and B are found to be:

$$A = 2(1 - V_{DSsat}) \quad (8a)$$

$$B = (1 - 2V_{DSsat}) + (V_{DS} - V_{DSsat})(2V_A - 1)/V_A \quad (8b)$$

In order to predict values of the parameters K , V_{TH} , and V_A , we have proposed a NSM model consisting of three neural networks, as illustrated in Fig. 1. The predicted values of these parameters are such that the coarse model output equals the FETToy's output.

All NNs used in the proposed model are multi-layer feed-forward perceptrons (MLPs) with only one hidden layer. It has already been proven that MLPs with only one hidden layer, with a proper training and selection of a correct number of neurons, are capable of learning any arbitrary function with some discontinuities and any accuracy [19]. According to [19, 20] we have selected 25 neurons, for all NNs. We have trained all NNs and used them to make our selections, in order to predict the appropriate values for the parameters used in Eq. (7).

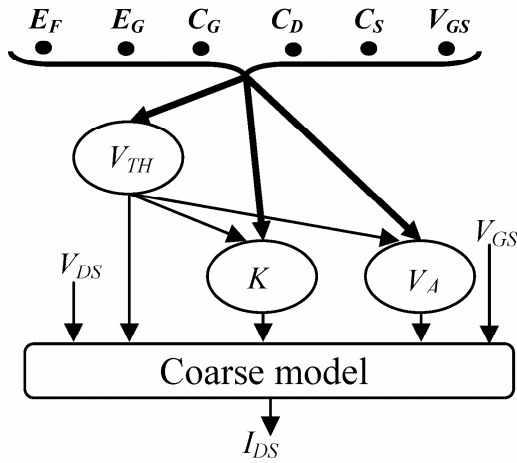


Fig. 1 The proposed NSM model, consisting of three NNs used to predict values of V_{TH} , K , and V_A .

3 Results and discussions

In order to evaluate the accuracy of our model for different values of gate-source and drain-source biases and also for different values of the physical parameters such as d , t_{ox} , C_G , C_D , and E_F , we have compared the results obtained from the proposed NSM model with those of FETToy. Then the resulting root mean squared (RMS) errors were compared with those generated from a similar comparison made between the model presented in [16] and FETToy. To make this comparison meaningful, first, we have used the values for the parameters same as those used in [16]; i.e., $T=300$ K, $C_D=C_S=6$ aF- μm^{-1} , $\epsilon_{ox}(\text{SiO}_2)=3.9$, $t_{ox}=1.5$ nm, $E_F=-0.32$ eV, and $d=1$ nm. The gate capacitance according to Eq. (3) becomes $C_G \approx 160$ aF- μm^{-1} . Fig. 2 illustrates the comparison made between $I_{DS}-V_{DS}$ characteristics for CNTFETs for a range of gate-source voltages $0.4\text{V} \leq V_{GS} \leq 1\text{V}$ with steps $\Delta V_{GS}=0.2$ V. In this figure, lines represent the results obtained using NSM, while bullets and triangles indicate the results obtained by the analytical model of [16] and those of FETToy, respectively.

The illustrations in Fig. 3 demonstrate comparison made for various CNTFETs, under constant $V_{GS}=1\text{V}$, CNT diameters is varied in the range of $0.5\text{nm} \leq d \leq 3\text{nm}$ with steps of $\Delta d=0.5\text{nm}$. Other physical parameters are kept the same as those for CNTFET of Fig. 2.

Fig. 4 illustrates the comparison made for various values of the source Fermi levels in the range of $-0.8\text{eV} \leq E_F \leq -0.2\text{eV}$ with steps of $\Delta E_F=0.2\text{eV}$, while other parameters are kept the same as those in Fig. 2.

A further comparison is made by varying C_G , while keeping the remaining parameters the same as those used for Fig. 2. Fig. 5 illustrates this comparison for various gate capacitances in the range of $100 \text{ aF-}\mu\text{m}^{-1} \leq C_G \leq 500 \text{ aF-}\mu\text{m}^{-1}$, varied by steps of $\Delta C_G=100 \text{ aF-}\mu\text{m}^{-1}$.

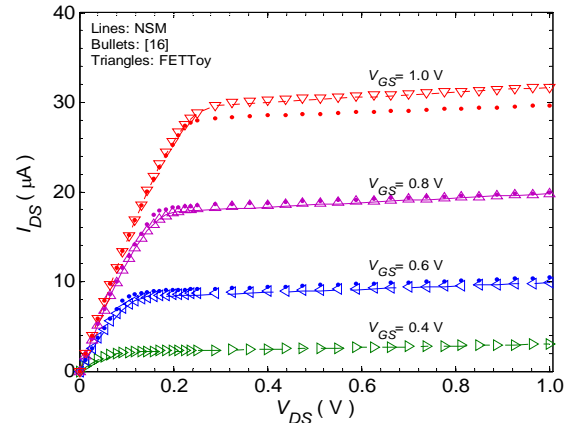


Fig. 2 Comparison of $I_{DS}-V_{DS}$ characteristics obtained by proposed NSM model with those of Ref [16] and FETToy for CNTFETs with $d=1\text{nm}$, $C_D=C_S=6$ aF- μm^{-1} , $t_{ox}=1.5\text{nm}$, $\epsilon_{ox}=3.9$ and $E_F=-0.32\text{eV}$, at $T=300\text{K}$, for various V_{GS} .

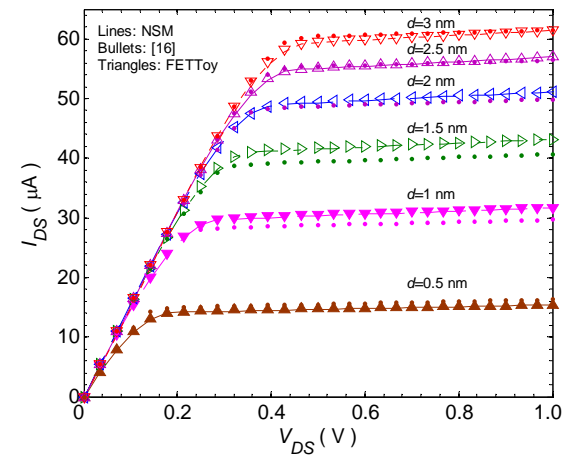


Fig. 3 Comparison of $I_{DS}-V_{DS}$ characteristics obtained by proposed NSM model with those of Ref [16] and FETToy for CNTFETs for $V_{GS}=1\text{V}$ for various d values. Other parameters are same as those of Fig. 2.

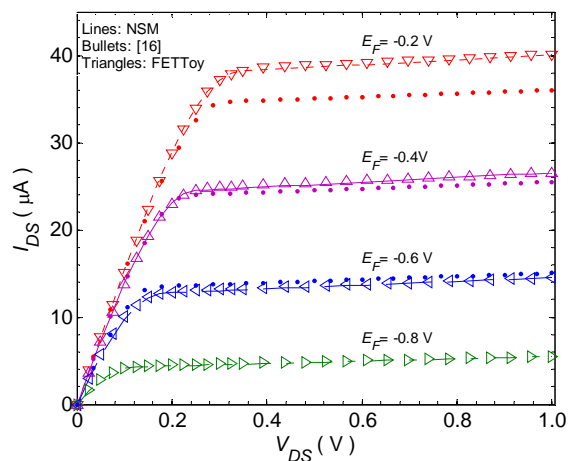


Fig. 4 Comparison of $I_{DS}-V_{DS}$ characteristics obtained by proposed NSM model with those of Ref [16] and FETToy for CNTFETs for $V_{GS}=1\text{V}$ and various E_F values. The remaining physical parameters are same as those of Fig. 2.

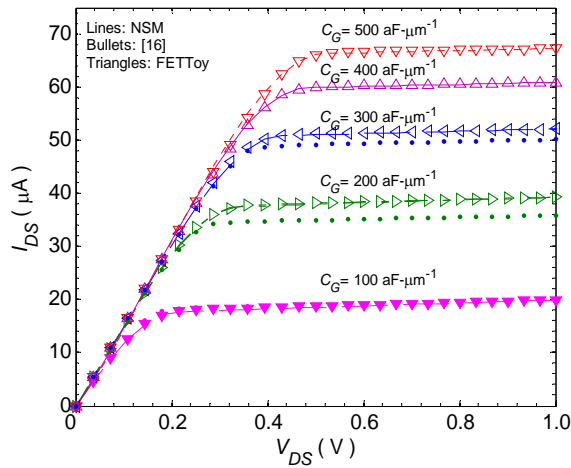


Fig. 5 Comparison of I_{DS} - V_{DS} characteristics obtained by the proposed NSM model with those of Ref [16] and FETToy, for CNTFETs and various C_G values. Other parameters are same as those of Fig. 2.

In Figs. 3-5, like in Fig. 2, lines, bullets, and triangles represent the simulation results obtained by NSM, model presented in [16], and FETToy. The comparisons, illustrated in Figs. 2-5, demonstrate excellent agreements between the results obtained from the proposed NSM model and those obtained by FETToy. They also demonstrate higher accuracy for NSM model, developed in this paper, with respect to that presented in [16]. Furthermore, results of these comparisons are summarized in Table 1. It demonstrates the normalized root mean squared (RMS) values of errors obtained from comparisons made between results of FETToy and those obtained from the analytical model of [16] and NSM model, separately. The normalization was done by the average of the FETToy model outputs.

Table 1 Comparison of the normalized root-mean-squared (RMS) errors for I_{DS} calculated from the proposed NSM model with respect to FETToys, for variables used in Fig. 2 and 3, with those of [16].

| Variable | | | | Normalized RMS Error in I_{DS} (%) | |
|---------------------|----------|------|------|--------------------------------------|------|
| Name | Symbol | Size | Unit | [16] | NSM |
| CNT Diameter | d | 0.5 | nm | 6.3 | 1.1 |
| | | 1 | | 5.2 | 0.57 |
| | | 1.5 | | 7.2 | 0.38 |
| | | 2 | | 3.9 | 0.39 |
| | | 2.5 | | 2.6 | 0.46 |
| Source Fermi level | E_F | -0.2 | eV | 8.9 | 0.5 |
| | | -0.4 | | 2.3 | 0.7 |
| | | -0.6 | | 5.2 | 1.4 |
| | | -0.8 | | 2.6 | 1.9 |
| Gate-Source Voltage | V_{GS} | 0.4 | V | 2.9 | 2.5 |
| | | 0.6 | | 5.1 | 1.9 |
| | | 0.8 | | 2.1 | 0.9 |
| | | 1.0 | | 5.2 | 0.57 |

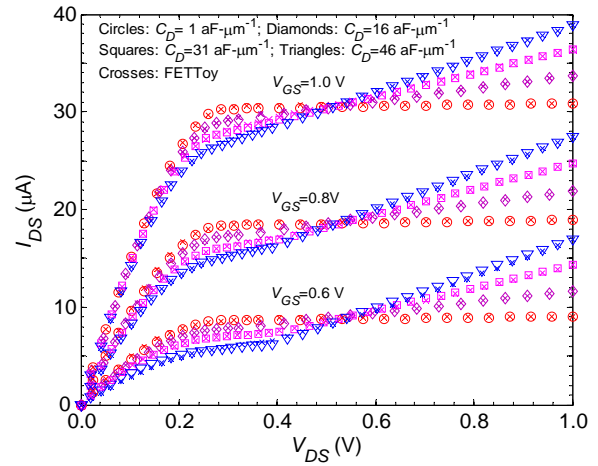


Fig. 6 Illustration of the channel length modulation by showing the dependence of I_{DS} - V_{DS} characteristics on C_D for various V_{GS} . The remaining physical parameters are the same as those in Fig. 2.

A further comparison is made to demonstrate how accurate the NSM model for short channel CNTFETs works. In this regard, we have varied C_D in a wide range, and simulated the device I_{DS} - V_{DS} characteristics for various V_{GS} , in each case. As an example, Fig. 6 shows I_{DS} - V_{DS} characteristics of CNTFETs with various drain capacitances in the range of $1 \text{ aF-}\mu\text{m}^{-1} \leq C_D \leq 46 \text{ aF-}\mu\text{m}^{-1}$ and $V_{GS} = 0.6, 0.8, \text{ and } 1.0 \text{ V}$. Other parameters are kept the same as those of Fig. 2. As seen in this figure, for a given V_{GS} , as C_D increases beyond a certain value, the familiar short channel effect known as channel length modulation roles up in I_{DS} - V_{DS} characteristics. In other words, the larger the C_D , the greater is the current slope in the saturation region, and hence the smaller becomes its corresponding parameter known as Early voltage, V_A . This is due to the fact that when C_D increases the drain control on the channel is enhanced, and hence the channel modulation becomes more pronounced. The result shown in this figure also demonstrates the excellent agreements that exist between NSM and FETToy, for long channel CNTFETs.

To evaluate how the proposed model, FETToy and Ref. [16] operate in the subthreshold region, the I_{DS} - V_{GS} characteristics of them are drawn in Fig. 7 for various values of the drain-source voltages, while other parameters are kept the same as those in Fig. 2. The subthreshold region in logarithmic scale is also superimposed. This figure demonstrates higher accuracy for the proposed model with respect to that presented in Ref. [16] in the subthreshold region.

Accuracy of the NSM model is indebted to three well adjusted fit parameters V_A , V_{TH} , and V_{DSsat} . Dependence of V_A on V_{GS} and C_D has just been demonstrated, indirectly in Fig. 6. Fig. 8 illustrates the parameter V_A as a function of C_D for CNTFETs with various C_G . While $V_{GS} = 1 \text{ V}$ and the remaining physical parameters are kept the same those of Fig. 2. As seen

from this figure, the channel modulation can also be enhanced by decreasing the size of the gate capacitance, C_G . Hence, in order to counter act the effect of channel length modulation for short channel CNTFETs one needs to increase C_G , through decreasing the oxide thickness, t_{ox} , and/or using an alternative gate material with higher dielectric constant. Above all, for a coaxial structure, in which C_G is greater than other structures, the short channel effect is minimized.

Next, we illustrate variation of another important adjustable model parameter, V_{TH} , with the gate oxide thickness, t_{ox} , CNT diameter, d , and V_{GS} , in Fig. 9. Fig. 9(a), as an example, illustrating V_{TH} as a function of t_{ox} , for three different diameters, $d=1, 2$, and 3 nm, biased at $V_{GS}=1$ V, shows that for a given t_{ox} , V_{TH} is a decreasing function of nanotube diameter, d . In contrast, for a given d , it is an increasing function of the oxide thickness.

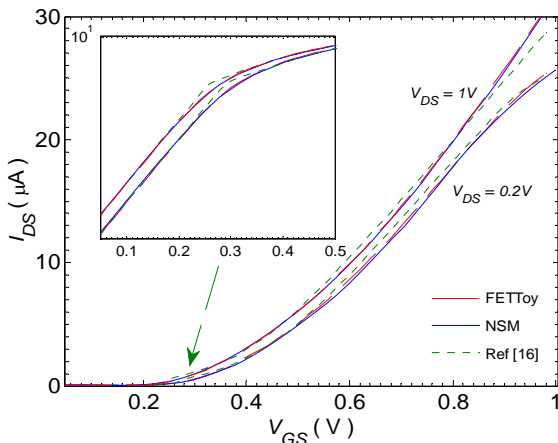


Fig. 7 Comparison of $I_{DS}-V_{GS}$ characteristics obtained by the proposed model with those of Ref [16] and FETToy, for CNTFETs with various V_{DS} values. Other parameters are same as those of Fig. 2.

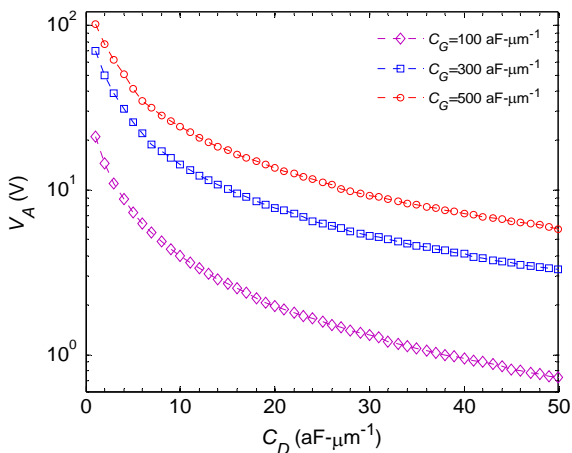


Fig. 8 Dependence of the adjustable model parameter V_A , known as the Early voltage, on C_D for various C_G values. Other physical parameters are the same as those in Fig. 2.

Fig. 9(b) shows variation of V_{TH} with t_{ox} while V_{GS} varies, and the remaining parameters are kept the same as those of Fig. 2.

Finally, we have calculated variations of the third adjustable model parameter, K , with t_{ox} , d , while the remaining physical parameters are kept the same those of Fig. 2. Fig. 10 illustrates an example for such variations. As one can be observe from this figure, for a given d , K increases with t_{ox} . Whereas, for a given t_{ox} , it is a decreasing function of d . At the first glance, one might feel that this contradicts the results shown in Fig. 3. However, a careful look at Eq. (7) together with Figs. 3, 9(a), and 10 reveals that this is not the case. An increase in d , in fact, decreases K and V_{TH} , both at the same time. On the other hand as seen from the second line in Eq. (7) I_{DS} , in saturation, is a linear function of K , while it decreases by V_{TH} , more or less in a parabolic manner.

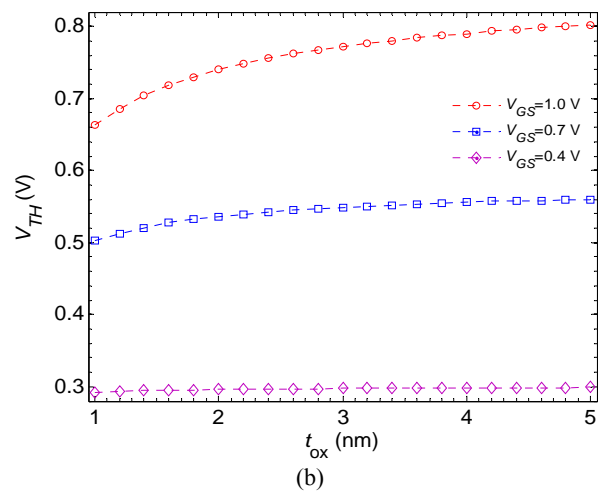
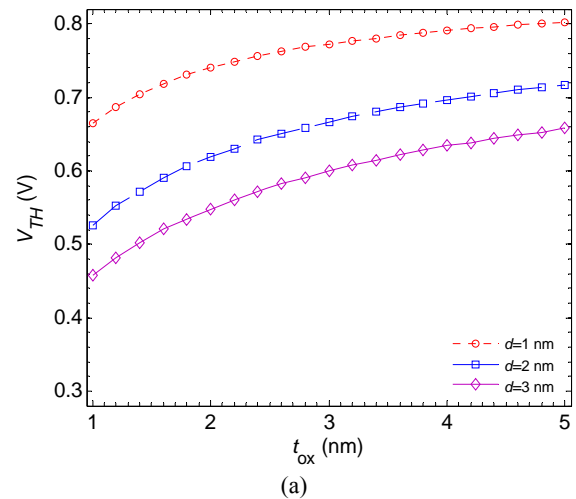


Fig. 9 Dependence of V_{TH} on t_{ox} for various (a) CNT diameters, d ; and (b) V_{GS} . Other parameters, in each case, are the same as those of Fig. 2.

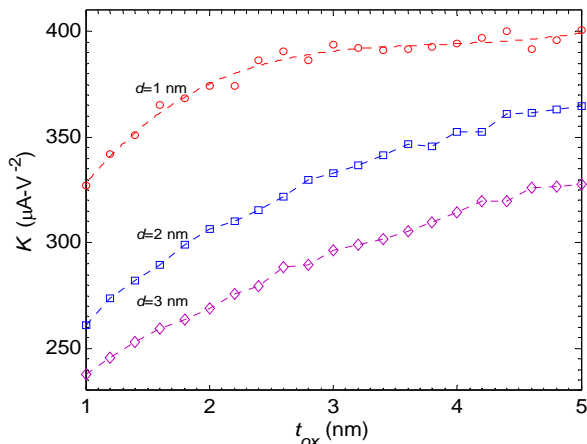


Fig. 10 Variation of adjustable model parameter, K , as a function of oxide thickness, t_{ox} , for various CNT diameters, d . The remaining parameters are the same as those of Fig. 2.

4 Conclusions

This paper presents a Neural-Space-Mapping (NSM), SPICE-compatible, modeling technique for carbon nanotube field effect transistors, at their ballistic limit. We have used the NSM concept to modify a well known "level 1" MOSFET model in Spice. The ensuing model not only is suitable for carbon nanotube transistors, such as MOSCNT, but also is SPICE compatible. Using the new developed model, we have studied $I_{DS}-V_{DS}$ characteristics of CNTFETs of various diameters, gate and drain capacitances under various V_{GS} biases, in details. We have also studied the CNTFETs channel length modulation, as a short channel effect. To demonstrate the accuracy of our developed model, we have compared our calculated I_{DS} with those evaluated by the analytical model of [16] and also with an exact numerical model known as FETToy [6]. Via this comparison we have demonstrated that the resulting RMS errors from our model are smaller than RMS errors from the model presented in [16]. Finally, model parameters, V_A , V_{TH} , and K and their dependence on various parameters were demonstrated.

The main advantage of the proposed NSM model in comparison to an exact self-consistent numerical model such as FETToy is direct calculation from the proposed formula without any numerical simulation. This makes the model compatible for circuit simulator such as Spice.

References

- [1] Neophytou N., Lundstrom M. and Guo J., "3D Electrostatics of Carbon Nanotube Field-Effect Transistors", *Comp Elec*, Vol. 3, pp. 277–280, 2004.
- [2] Frank D. J., Dennard R. H., Nowak E., Soloman P. M., Taur Y. and Wong H. P., "Device scaling limits of Si MOSFETs and their application dependencies", *Proc IEEE*, Vol. 89, No. 3, pp. 259–288, Mar. 2001.
- [3] Léonard F. and Tersoff J., "Multiple functionality in nanotube transistors", *Phys Rev Lett*, Vol. 88, No. 25, pp. 258302–258305, Jun. 2002.
- [4] Heinze S., Tersoff J., Martel R., Derycke V., Appenzeller J. and Avouris P., "Carbon nanotubes as Schottky barrier transistors", *Phys Rev Lett*, Vol. 89, pp. 106801–106804, 2002.
- [5] Guo J., Datta S. and Lundstrom M. S., "A numerical study of scaling issues for Schottky-Barrier carbon nanotube transistors", *IEEE Trans Electron Dev*, Vol. 51, No. 2, pp. 172–177, 2004.
- [6] Rahman A., Guo J., Datta S. and Lundstrom M., "Theory of ballistic nanotransistors", *IEEE Trans Electron Dev*, Vol. 50, No. 9, pp. 1853–1864, 2003.
- [7] FETToy matlab code: www.nanohub.org.
- [8] <http://www.eecs.berkeley.edu/IPRO/Software/>.
- [9] Fregonese S., d'Honinckthun H. C., Goguet J., Maneux C., Zimmer T., Bourgoin J. P., Dollfus P. and Galdin-Retailleau S., "Computationally Efficient Physics-Based Compact CNTFET Model for Circuit Design", *IEEE Trans Electron Dev*, Vol. 55, pp. 1317–27, 2008.
- [10] Raychowdhury A., Mukhopadhyay S. and Roy K., "A circuit compatible model of ballistic carbon nanotube field-effect transistors", *IEEE Trans Computer-Aided Design of Integrated Circuit and System*, Vol. 23, No. 10, pp. 1411–1420, Oct. 2004.
- [11] Balijepalli A., Sinha S. and Cao Y. u., "Compact Modeling of Carbon Nanotube Transistor for Early Stage Process-Design Exploration", *ACM ISLPED*, pp. 27–29, August 2007.
- [12] Paul B. C., Fujita S., Okajima M. and Lee T., "Modeling and analysis of circuit performance of ballistic CNFET", *43rd Design Automation Conference*, pp. 717–722, July 2006.
- [13] Jimenez D., Cartoixa X., Miranda E., Sune J., Chaves F. A. and Roche S., "A Simple drain current for Schottky-Barrier carbon nanotube field effect transistors", *Nanotechnology*, Vol. 18, pp. 025201–025206, 2007.
- [14] Sinha S., Balijepalli A. and Cao Y. u., "A Simplified Model of Carbon Nanotube Transistor with Applications to Analog and Digital Design", *Proc 9th International Symposium on Quality Electronic Design IEEE*, San Jose, USA, pp. 502–507, Mar. 2008.
- [15] Kazmierski T. J., Zhou D. and M Al-Hashimi B., "Efficient circuit-level modelling of ballistic CNT using piecewise non-linear approximation of mobile charge density", *EDAA*, Munich, Germany, pp. 146–151, March 2008.
- [16] Hashempour H. and Lombardi F., "Device Model for Ballistic CNFETs Using the First Conducting Band", *IEEE Design & Test of Computers*, Vol. 25, No. 2, pp. 178–186, March–April 2008.

- [17] Cheng Q., "Advances in implicit and output space technology", *Phd Thesis*, Department of Electrical and Engineering, McMaster University, Canada, 2004.
- [18] Tsividis Y., *Operation and Modeling of the MOS Transistor*, 2nd ed, USA: Oxford University Press, 2003.
- [19] Haykin S., *Neural Network*, Prentice-Hall, 1994.
- [20] Melster N., Shoham M. and M. Manevitz L., "Approximating Functions by Neural Networks: A Constructive Solution in the Uniform Norm", *Neural Networks*, Vol. 9, No. 6, pp. 965-978, 1996.



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