Gate Leakage Aware Optimal Design of Modified Hybrid Nanoscale MOSFET and Its Application to Logic Circuits

A. K. Rana*, N. Chand* and V. Kapoor*

Abstract: With the explosive growth in portable computing and wireless communication during last few years, power dissipation has become critical issue. Under such condition gate leakage has been recognized as a dominant component of power dissipation. This work proposes a modified hybrid MOSFET (MHMOS) i.e. gate-to-source/drain non-overlap MOSFET in combination with high-k layer/interfacial oxide as gate stack to reduce the gate leakage current. The extended S/D in the non-overlap region is induced by fringing gate electric field through high-k dielectric and SiO_2 dual spacer. Compact analytical model and Sentaurus simulation have been used to study the gate leakage behaviour of MHMOS. A good agreement is observed between analytical and Sentaurus simulation results. It is found that MHMOS structure has reduced the gate leakage current to great extent as compared to conventional overlapped MOSFET structure. Further, degradation in drive current caused by the utilization of high-k gate dielectric has been improved by the use of dual spacer.

Keywords: Hybrid MOSFET (HMOS), Gate Tunneling Current, Analytical Model, Spacer Dielectrics, DIBL, Subthreshold Slope.

1 Introduction

Since the invention of Si-based metal-oxide-silicon field effect transistor (MOSFET), there has been an unprecedented evolution in semiconductor industry. Nowadays very large scale integrated circuits (VLSIs) using complementary-MOS (CMOS) technology have been widely used as a main controlling unit everywhere in our life such as manufacturing, communication, healthcare, etc., which has become inevitable tools for living [1]. The progress of VLSIs has been accomplished by device scaling in accordance with Moore's Law. MOSFET down scaling requires very thin gate oxide to minimize the short channel effects [2-3]. Under such circumstances, the gate leakage current has become dominant leakage current component [4]. Thus, to reduce the gate leakage current in present era of integrated circuits, new CMOS compatible device structures are needed as a method to contain/reduce the gate leakage current especially for low power battery-operated portable applications [5].

Iranian Journal of Electrical & Electronic Engineering, 2011.
Paper first received 20 Dec. 2010 and in revised form 6 March 2011.
* The Authors are with the Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, Hamirpur (H.P)-177005, India.
Emails: ashwani_paper@yahoo.com, nar@nitham.ac.in, kapoor@nitham.ac.in.

In the past, various techniques have been proposed to control the gate leakage currents. The work in [6] presents an approach to reduce I_{sub}, but not I_{gate}. The impact of I_{gate} on delay is discussed in [7], but its impact on leakage power is not addressed. In [8], the authors presented circuit-level techniques for gate leakage minimization. In each of these reports, extensive SPICE simulations were performed to obtain estimates of gate leakage. In [9], authors addressed various leakage mechanisms including gate leakage and presented circuit level technique to reduce the leakage. However, this can be extremely time-consuming, especially for large circuits. In [10], the authors examine the interaction between I_{gate} and I_{sub}, and their state dependencies. This work applies pin reordering to minimize I_{gate}. In [11], Lee et al., developed a method for analyzing gate oxide leakage current in logic gates and suggested pin reordering to reduce it. Sultania et al., in [12], developed an algorithm to optimize the total leakage power by assigning dual T_{ox} values to transistors. In [13], Sirisantana and Roy use multiple channel lengths and multiple gate oxide thickness for reduction of leakage. Mohanty et. al. [14] have presented analytical models and a data path scheduling algorithm for reduction of gate leakage current. In [15], conventional offset gated MOSFET structure has been widely used to reduce subthreshold leakage but gate

leakage reduction has not been addressed in the literature so far. Thus, the general problems of gate leakage reduction techniques are the need for additional devices (e.g. sleep transistors) and the reduction of only one component of leakage. Moreover, transistor level approaches are not applicable for standard cell designs and require long calculation time. Further, gate level DVT-/DTOCMOS methods do not offer the best possible solution as the number of gate types limits the improvement.

To mitigate this problem, hybrid MOSFET (HMOS) structure is proposed to reduce the gate leakage current significantly because gate leakage current through the source/drain overlap region has been identified as the principal source of power dissipation in VLSI chips especially in sub-1V range [16]. The use of High-k as gate dielectric, further, reduces the gate leakage current by increasing the physical thickness of the gate dielectric through which carrier tunnel. The extended S/D region in the non-overlap region has been created by adopting the high-k material as a spacer. An effective and compact model has been developed for analyzing the gate tunneling current of HMOS by considering the NSE (nano scale effect) effect that are difficult to ignore at nano scale regime. The NSE effect include (i) the non-uniform dopant profile in poly-gate in vertical direction resulted due to low energy ion implantation, (ii) additional depletion layer at the gate edges due to gate length scaling down and (iii) gate oxide barrier lowering due to image charges across the Si/SiO_2 interface. We, also, adopted advanced physical models in the simulation (Sentaurus simulator) [17] to see other device characteristics such as DIBL (drain induced barrier lowering), SS (subthreshold slope), on current and off current.

The rest of the paper is organized as follows. Section 2 presents the gate current model for modified HMOS. The device design and structure of HMOS and modified HMOS is presented in Section 3. Section 4. presents the Sentaurus simulation set up for analysis. The results and discussion are presented in Section 5. Section 6 utilizes the modified HMOS to estimate and reduce the gate leakage current. Finally, conclusions and future directions are summarized in Section 7.

2 Anlytical Gate Current Model

As MOSFET shrinks, the current transport in gate dielectric is mainly contributed by the electron and hole tunneling from one energy-band to another. In high-k gate dielectric, there is inelastic trap assisted tunneling where electron first tunnel to deep lying traps, become released from the trap state and subsequently tunnel to gate under the influence of applied electric field. The energy band diagram in inversion condition of a hybrid MOSFET is given in Fig. 1.

The analytical model developed by us in [18] is applied to modified hybrid MOSFET and for brevity, total gate leakage current (I_g) is given by

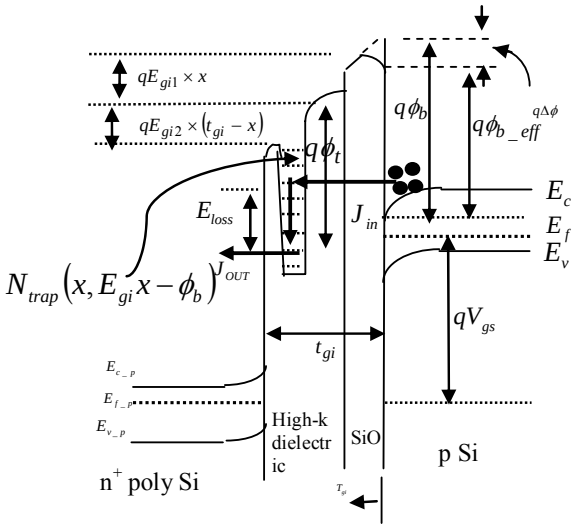


Fig. 1 Energy band diagram showing the two step inelastic trap assisted tunneling through hybrid MOSFET.

$$I_g = I_{gc} = J_{ITAT\_ch} \times L_g \quad (1)$$

$$J_{ITAT} = \frac{q}{A_g}\sigma_t N_{trap}\left(x, qE_{gi}x - \phi_{b\_eff}\right).P_{ITAT}\left(x, E, E_{gi}\right) \quad (2)$$

where P_{ITAT} can be expressed as

$$P_{ITAT} = \frac{J_1\left(\phi_{b\_eff}, x, E_{gi1}\right).J_2\left(\phi_t, t_{gi} - x, E_{gi2}\right)}{J_1\left(\phi_{b\_eff}, x, E_{gi1}\right) + J_2\left(\phi_t, t_{gi} - x, E_{gi2}\right)} \quad (3)$$

J_1 and J_2 are the uniform current densities and are taken from Ashwani et al. [18]. Here, I_{gc} is the gate tunneling current through channel region and J_{ITAT_ch} is the inelastic trap-assisted tunneling current density through channel region, x is the distance from the Si–high-k dielectric interface, $N_{trap}(x, E)$ is the sheet trap density in cm^2 at a distance x and having the energy level with respect to the conduction band edge of gate dielectric, $O_t(x, E)$ is the electron occupancy of the traps at a distance of x and the energy of E, σ_t is the capture cross section of the traps and is assumed to be constant irrespective of the position and energy level of the traps, A_g is the gate tunneling area, Φ_t is the barrier height of the gate insulator trap states, E_{gi} is the electric field in the gate insulator, E_{gi1} is the electric field over a distance x of the trap relative to the interface in the gate insulator and E_{gi2} is the electric field over a distance t_{gi}- x relative to the interface in the gate insulator, ϕ_b is the interface barrier height of composite gate dielectric i.e. combination of interfacial oxide and high-k gate dielectric. It is taken as the average of barrier height of interfacial oxide and high-k gate layer. So

$$\phi_b = \frac{\left(\phi_{b\_ox} + \phi_{b\_hk}\right)}{2} \quad (4)$$

where ϕ_{b_hk} is the barrier height of high-k gate layer and ϕ_{b_ox} is the barrier height of oxide layer. ϕ_{b_eff} is the effective barrier height, given as below,

$$\phi_{b\_eff} = \phi_b - \Delta\phi \quad (5)$$

$$\Delta\phi = \sqrt{\frac{qE_{gi}}{4\pi\varepsilon_{eff}}} = \sqrt{\frac{qV_{gi}}{4\pi\varepsilon_{eff}T_{gi}}} = \left(\frac{2q^3 N_{DTC(ch)}\phi_{b\_eff}}{16\pi^2\varepsilon_{eff}^3}\right)^{1/4} \quad (6)$$

The $\Delta\phi$ is the reduction in the barrier height at the high-k/SiO_2/Si interface from Φ_b so that barrier height becomes ϕ_{b_eff}. This reduction in barrier height is due to image charges across the interface. This barrier reduction is of great interest since it modulates the gate tunneling current. $N_{DTC(Ch)}$ is the effective density of carrier in channel and ε_{eff} is the equivalent dielectric constant of composite gate dielectric. We have found the equivalent dielectric constant of the composite gate dielectric in terms of the oxide thickness by considering the MOSFET as parallel plate capacitor with two dissimilar dielectrics.

$$\varepsilon_{eff} = \left[\frac{t_{ox}}{\varepsilon_{ox}t_{gi}} + \frac{t_{gi} - t_{ox}}{\varepsilon_{hk}t_{gi}}\right]^{-1} \quad (7)$$

where ε_{eff}, ε_{ox} and ε_{hk} are the dielectric constants of the equivalent dielectric, interfacial oxide, and the high-k gate dielectric respectively, t_{gi} is the total thickness of the gate dielectric, and t_{ox} is the thickness of interfacial oxide.

3 Device Design

The cross-section of HMOS and modified HMOS for the analysis of the gate tunneling current characteristics, is shown in Fig. 2.

The MOSFET has n^+ poly-Si gate of physical gate length (L_g) of 35 nm, gate dielectric of 1.0 nm EOT (equivalent oxide thickness) - 0.3 nm interfacial oxide and 0.7 nm EOT of high-k gate dielectric. The buffer oxide of 0.3 nm under high-k spacer has been taken to minimize the stress between spacer and substrate. Here L_{no} represents the non-overlap length between gate to source/drain. The source/drain extension region are created with the help of fringing gate electric field by inducing an inversion layer in the non overlap region. The spacer consist of 10 nm oxide spacer and 10 nm high-k HfO_2 spacer to induce the inversion layer in the non-overlap region. The halo doping around the S/D also reduces short-channel effects, such as the punch through current, DIBL, and threshold voltage roll-off, for different non-overlap lengths.

4 Simulation Set Up

Figure 3 shows the Santaurus simulator schematic of modified HMOS. The doping of the silicon S/D region is assumed to be very high, $1x10^{20}$ cm^{-3}, which is close to the solid solubility limit and introduces negligible silicon resistance.

The dimension of the silicon S/D region is taken as 40 nm long and 20 nm high. This gives a large contact area resulting in a small contact resistance. The doping concentration in silicon channel region is assumed to be

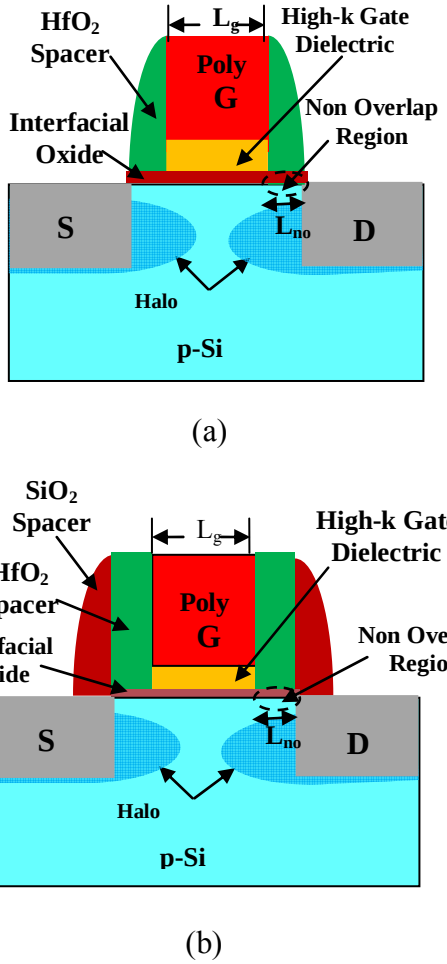


Fig. 2 Schematic cross-section of proposed (a) hybrid MOSFET [18] and (b) modified hybrid MOSFET.

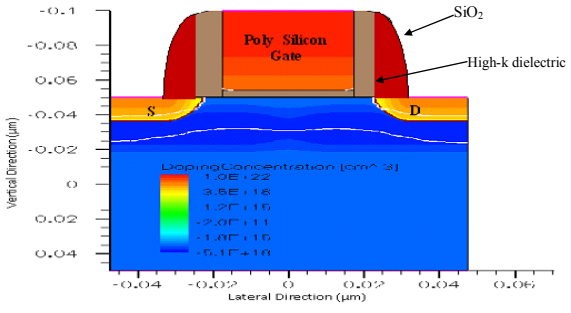


Fig. 3 Sentaurus schematic cross-section of modified HMOS.

graded due to diffusion of dopant ions from heavily doped S/D region with a peak value of $1x10^{18}$ cm^{-3} and $1x10^{17}$ cm^{-3} near the channel. The poly-silicon doping has been taken to be $1x10^{22}$ cm^{-3} at the top and $1x10^{20}$ cm^{-3} at bottom of the polysilicon gate i.e. interface of oxide and silicon. The MOSFET was designed to have V_{th} of 0.25 V. We determined V_{th} by using a linear extrapolation of the linear portion of the I_{DS}-V_{GS} curve at low drain voltages. The operating voltage for the

devices is 1.0 V. The simulation study has been conducted in two dimensions, hence all the results are in the units of per unit channel width.

The simulation of the device is performed by using Santaurus design suite [20], with drift-diffusion, density gradient quantum correction and advanced physical model being turned on.

Figure 4 plots the variation of vertical electric along the channel direction with HfO_2 and SiO_2 as dual spacer in the non-overlap region for different gate dielectrics i.e. SiO_2, Si_3N_4 and HfO_2. It is clear from figure that the magnitude of vertical electric field is almost constant with change of gate dielectric. The fringing electric field is a strong function of dielectric constant of spacer material instead of dielectric constant of gate dielectric material. However, result shows that reasonable vertical electric field is obtained under non-overlap region by HfO_2 high-k spacer compared to the oxide spacer to induce the inversion layer. This implies that the on-state current of the high-k spacer non-overlapped gate to S/D MOSFET can be significantly larger than that of the oxide spacer MOSFET. It also shows that vertical electric field magnitude decreases significantly with the distance of non-overlap region from the gate edge thereby limiting the non-overlap length (L_{no}).

Figure 5 plots the electron concentration along channel for three different spacer such as HfO_2 (k = 22) /SiO_2, Si_3N_4 (k = 7.5)/SiO_2 and SiO_2 (k = 3.9) in the non-overlap region. Electron concentration below the spacer increases as the dielectric constant of the spacer material increases. This is due to the fact that electron concentration under the spacer strongly depends on the intensity of vertical fringing field. At Vgs = 1.0 V, electron concentration more than $2.7x10^{19}$ cm^{-3} is induced under the dual spacer which can act as extended source/drain region.

It is observed from the Fig. 6 that electron concentration below the dual spacer also remains

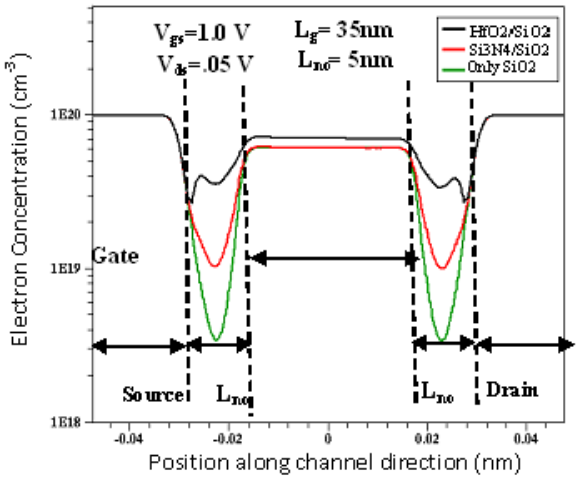


Fig. 5 Electron concentration along channel for different high-k dual spacer in the non-overlap region.

constant with the change of dielectric constant of gate dielectric. This is due to that fact that vertical fringing field remains constant with the change of dielectric constant of dielectric.

5 Result And Discussion

Computation have been carried out for a n-channel nanoscale modified hybrid MOSFET (HMOS) to estimate the gate tunneling current. The interfacial oxide thickness and EOT for high-k gate dielectric have been taken to be 0.3 nm and 0.7 nm respectively with a combined EOT of 1.0 nm. This model is computationally efficient and easy to realize.

The comparision between the simulated data and the model data for gate tunneling current is presented in Fig. 7. The figure shows the gate tunneling current versus gate bias for modified HMOS with HfO_2/SiO_2 dual spacer above the non-overlap region at an

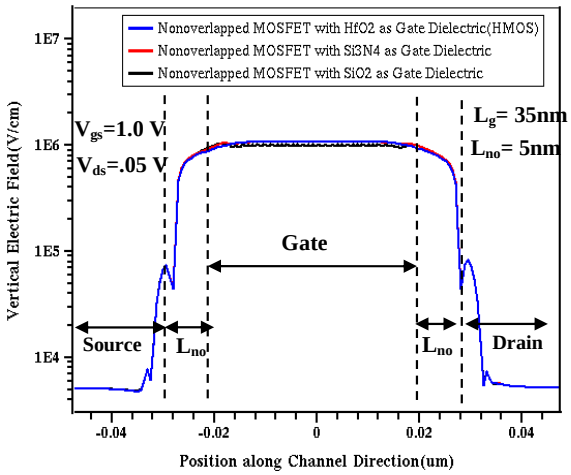


Fig. 4 Vertical electric field along channel with HfO_2 spacer in the non overlap region for different gate dielectrics *i.e.*SiO_2, Si_3N_4 and HfO_2.

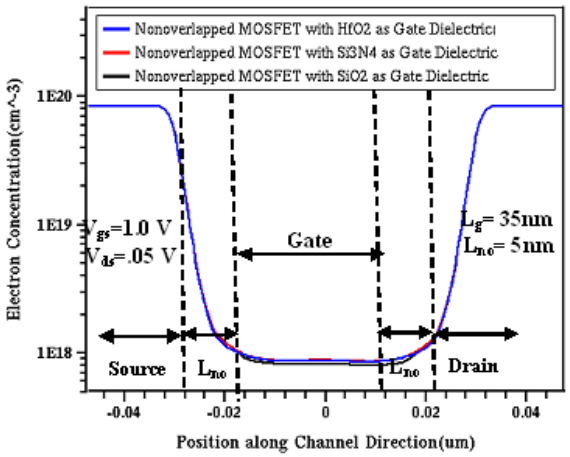


Fig. 6 Electron concentration along channel with HfO_2 and SiO_2 dual spacer in the non overlap region for different gate dielectrics i.e. SiO_2, Si_3N_4 and HfO_2.

equivalent oxide thickness (EOT) of 1 nm and non-overlap length of 5 nm. It is shown in Fig. 6 that analytical result calculated by our model has better agreement with the simulated results certifying the high accuracy of the propsed analytical modelling. The simulation for modified HMOS with HfO_2 as high-k gate dielectric has been carried out with $t_{HfO2} = 3.95$ nm, $t_{interfacial\_oxide} = 0.3$ nm. $\phi_{b\_hk}(HfO_2) = 1.5$ ev [19], $m_{hk} = 0.18m_o$ [19], $\sigma_t = 9.3\times10^{-16}$ cm^2 [20], $N_{trap} = 7.67\times10^{12}$ cm^{-2} [20]. The trap position (x_t) is extracted to be $0.35\, t_{HfO2}$ in the inelastic tunneling model by comparing the magnitude of J_{ITAT} with that of direct tunneling current of MOS capacitors with gate oxides of 3.95 nm. The fitting parameters E_{loss} and $\alpha_{(ch)}$ have been taken to 0.35 eV, 0.63 respectively to fit the model with the simulated value.

Figure 8 shows the variation of gate tunneling current with gate bias for different gate dielectrics of HMOS. It is observed that gate leakage current decreases significantly for HMOS compared to overlapped conventional structure. This is because gate-to-S/D overlap region is absent in our designed HMOS, so gate tunneling (leakage) current is reduced to greater extent. The reduction is significant with the increase of dielectric constant of gate dielectric of HMOS. This is because vertical electric field responsible for carrier tunneling decreases as the physical thickness of gate insulator increases with increase in dielectric constant(k). The simulation for HMOS with Si_3N_4 high-k gate dielectric has been carried out with $t_{Si_3N_4} = 1.35$ nm, $t_{interfacial\_oxide} = 0.3$ nm. $\phi_{b\_hk}(Si_3N_4) = 2.0$ ev [19], $m_{hk} = 0.20\ m_o$[19], $\sigma_t = 3\times10^{-13}$ cm^2 [21], $N_{trap} = 3\text{x}10^{11}$cm^{-2} [22]. The trap position (x_t) is extracted to be 0.29 t_{Si3N4} in the inelastic tunneling model by

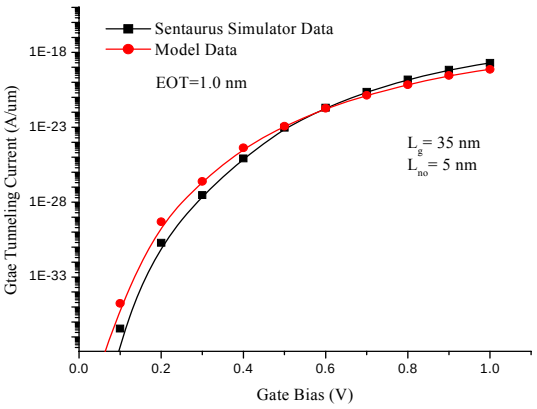


Fig. 7 Comparison of analytical model data with Sentaurus simulated data for modified HMOS with equivalent oxide thickness (EOT) of 1.0 nm and gate-to-S/D non-overlap length (L_{no}) of 5 nm.

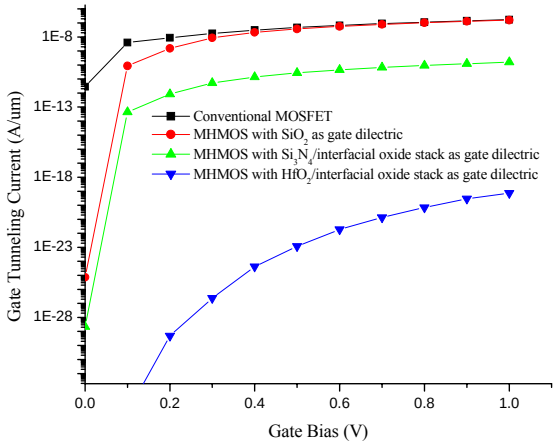


Fig. 8 Gate tunneling current vs gate bias for modified HMOS with different gate dielectrics e.g. SiO_2, Si_3N_4 and HfO_2.

comparing the magnitude of J_{ITAT} with that of direct tunneling current of MOS capacitors with gate oxides of 1.35 nm. The fitting parameters E_{loss} and $\alpha_{(ch)}$ has been taken to 0.23 eV, and 0.71 respectively to fit the model with the simulated value.

Figure 9 plots the gate tunneling current with gate bias for HfO_2 based high-k modified HMOS and overlapped HfO_2 based high-k conventional MOSFET at an EOT of 1.0 nm. It is observed that gate leakage current decreases significantly for HfO_2 based high-k HMOS as compared to overlapped HfO_2 based high-k conventional MOSFET especially at low gate bias range. At low gate bias, channel is about to form so that gate leakage current is mainly due to carrier tunneling through gate-to-S/D overlap region. The gate-to-S/D overlap region is absent in our designed HfO_2 based high-k HMOS, so gate tunneling (leakage) current is reduced to greater extent. However, at higher gate bias range the gate tunneling (leakage) current is mainly due to the carrier tunneling through the channel region to the gate. Due to this reason, gate tunneling current is almost same for both structure.

Figure 10 shows the variation of DIBL and SS for modified HMOS with different gate dielectrics e.g. SiO_2, Si_3N_4 and HfO_2 at an EOT of 1.0 nm. It is observed in Fig. 9 that DIBL is maximum (73.42 mV/V) for overlapped gate-to-S/D MOSFET structure (conventional MOSFET).

It is due to the fact that the effect of fringing field on channel is maximum. Due to this decrease in gate control, the drain electrode is tightly coupled to the channel and the lateral electric field from the drain reaches a larger distance into the channel. Consequently, this electrically closer proximity of drain to source gives rise to higher drain-induced barrier lowering (DIBL) in overlapped gate-to-S/D MOSFET structure. In non-overlapped gate-to-S/D MOSFET structure, DIBL improves because lateral electric field

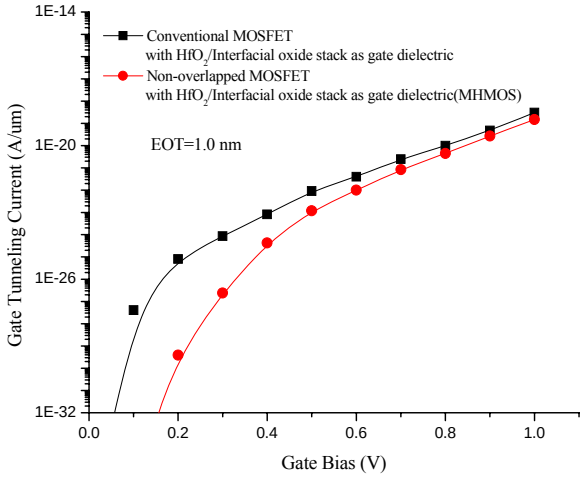


Fig. 9 Gate tunneling current vs gate bias for HfO_2 based high-k modified HMOS and overlapped HfO_2 based high-k conventional MOSFET at an EOT of 1.0 nm.

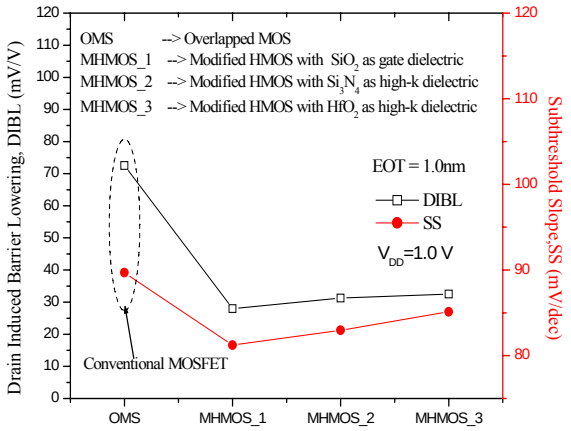


Fig. 10 DIBL, SS for modified HMOS with different gate dielectrics e.g. SiO_2, Si_3N_4 and HfO_2.

from the drain reaches a smaller distance into the channel. This is due to increase in metallurgical gate length as compared to conventional MOSFET structure in the same physical gate length. For modified HMOS, with SiO_2 (HMOS_1), with Si_3N_4 (HMOS_2) and HfO_2(HMOS_3) as gate dielectric, DIBL degrades due to increased coupling of lateral electric field from the drain into the channel because of slightly enhanced fringing field. It is also shown in Fig. 9 that subthreshold characteristic improves for non-overlapped gate-to-S/D MOSFET structure (MHMOS) compared to overlapped gate-to-S/D conventional MOSFET structure. But, for MHMOS with Si_3N_4 (HMOS_2) and HfO_2 (HMOS_3) gate dielectric, SS degrades due to increased the depletion capacitance in the subthreshold equation.

Figure 11 represents the on and off current behavior of modified HMOS with different gate dielectrics e.g SiO_2, Si_3N_4 and HfO_2. It is observed in figure that on current slightly degrades and off current slightly improves with increase in dielectric constant of gate dielectric due to increase in threshold voltage (V_{th}).

Figure 12 shows the impact of modified HMOS over off and on current. It is observed in figure that on current improves with the introduction of dual spacer. The improvement is because of the slight decrease in threshold voltage due to slight reduction in gate fringing field. The slight decrease in threshold voltage (V_{th}), in turn, slightly degrades the off current for both modified HMOS (MHOS_2 i.e. modified HMOS with Si_3N_4 as gate dielectric and MHMOS_3 modified HMOS with HfO_2 as gate dielectric).

The impact of modified HMOS on DIBL and SS is plotted in Fig. 13. It is observed in figure that DIBL and SS improves for both modified HMOS i.e. MHOS_2 (modified HMOS with Si_3N_4 as gate dielectric) and MHMOS_3 (modified HMOS with HfO_2 as gate

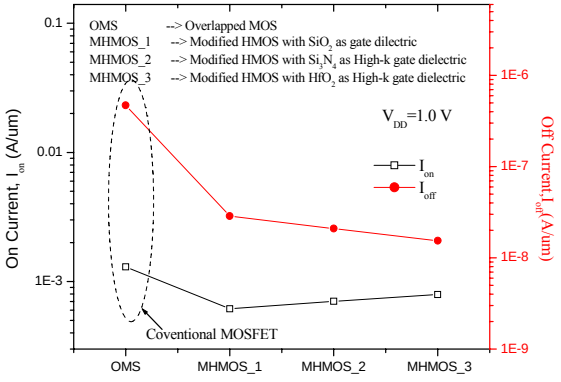


Fig. 11 On and off current of modified HMOS with different gate dielectrics e.g. SiO_2, Si_3N_4 and HfO_2 at an EOT of 1.0 nm.

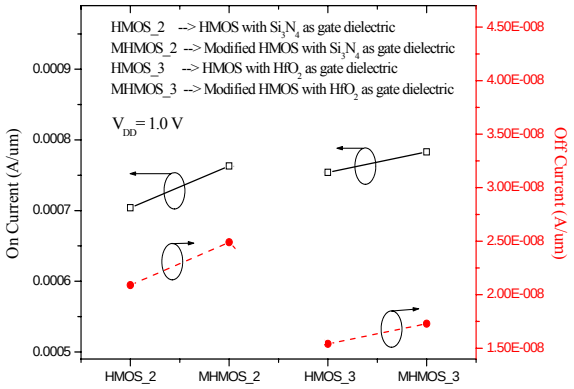


Fig. 12 Impact of modified HMOS over off and on current with EOT of 1.0 nm.

dielectric) due to slightly reduced coupling of lateral electric field from the drain into the channel.

Figure 14 shows the minimum subthreshold swings reported in the literature for Bulk CMOS, fully depleted SOI, FINFET, carbon nanotube FET, nano-wire based FET, impact-ionization based MOS, nano-electro-mechanical switches (NEMS) with CMOS and HMOS. It can be observed that HMOS has better subthreshold in CMOS compatible category. But, it is degraded in comparison to other reported devices i.e. FDSOI, FINFET, CNFET NWFET, IMOS and NEMS.

Similarly, on and off current as shown in Fig. 15 degrade to small extent but our HMOS device show much improved gate leakage characteristics in CMOS compatible technology with acceptable DIBL, SS, on and off currents.

6 Application of Modified HMOS to an Inverter

This section deals with the application of proposed modified HMOS to logic Inverter to analyze, estimate and reduce the gate leakage current in nanoscale MOSFET. We calculated the total gate leakage (tunneling) current for each device by summing all components as:

$$I_g[\text{MOSFET}] = I_{gso} + I_{gdo} + I_{gcs} + I_{gcd} \quad (8)$$

where all the currents are in Ampere/µm. The width (W_N) of all n-MOS devices have been taken to be 1 µm to eliminate the narrow width effect whereas it (W_P) is 2 µm for all p-MOS devices to maintain the symmetry.

The leakage current of a logic gate is calculated from all components for each p-MOS and n-MOS device in the logic gate. Thereafter, the total gate leakage current calculated by summing the components is given below

$$I_g[n] = I_{gso}[n] + I_{gdo}[n] + I_{gcs}[n] + I_{gcd}[n] \quad (9)$$

where n represents the particular device within a gate.

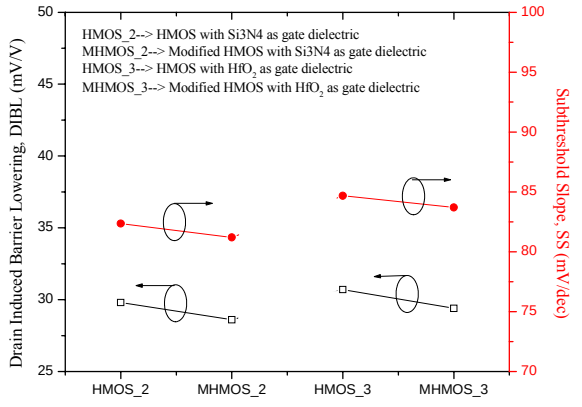


Fig. 13 Impact of modified HMOS on DIBL and SS with EOT of 1.0 nm.

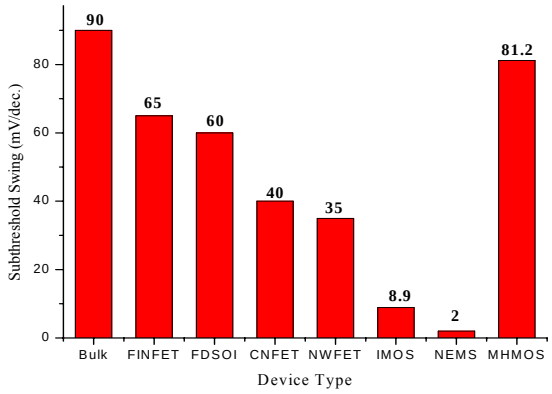


Fig. 14 Comparison of minimum subthreshold swings reported in the literature [23, 24] and HMOS.

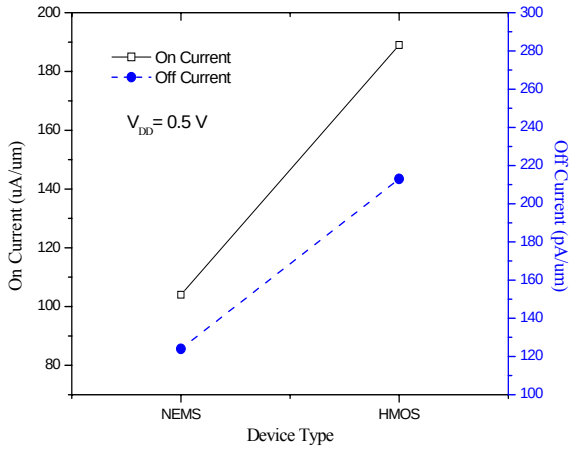


Fig. 15 Comparison of on and off current for NEMS [23,24] and modified HMOS for V_{DD} of 0.5 V.

Total gate leakage current for logic gate (I_{gate}) is then calculated by summing the gate currents over all the devices in each gate:

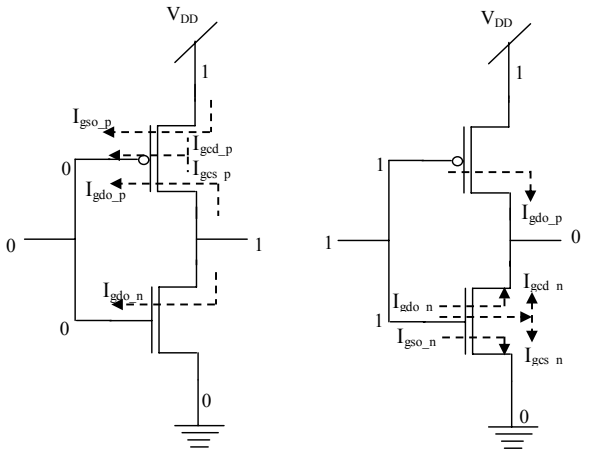
$$I_g = \Sigma_n I_g[n] \quad (10)$$

Estimating gate leakage for an inverter is crucial as it is not only present in SRAM but also works as buffer in the routing (switch and connection block) and in the logic block. By knowing the states of the transistors in inverters, our gate leakage compact models [18] can be used.

Thus, gate leakage current in an inverter circuit for each of the possible input combinations can be calculated as below

$$I_g(\text{input} = \text{"0"}) = (I_{gso\_p} + I_{gdo\_p} + I_{gc\_p} + I_{gcd\_p}) \times W_P + I_{gdo\_n} \times W_N \quad (11)$$

and



(a) With input "0" (b) With input "1"

Fig. 16 Gate leakage current paths in various switching state of inverter for different inputs. High logic level is indicated by "1" while low logic level is indicated by "0".

$$I_g(\text{input} = \text{"1"}) = (I_{gso\_n} + I_{gdo\_n} + I_{gcs\_n} + I_{gcd\_n}) \times W_N + I_{gdo\_p} \times W_P \quad (12)$$

where, the subscript n denotes the gate leakage component for n-MOSFET and p denotes the gate leakage component for p-MOSFET. Thus, average gate leakage current in inverter circuit is given by

$$\overline{I_g}(\text{inverter}) = \frac{I_g(\text{input} = \text{"0"}) + I_g(\text{input} = \text{"1"})}{2} \quad (13)$$

Figure 17 plots the gate leakage current for conventional, HMOS and modified HMOS structures in each input pattern. Figure also shows the comparison of the analytical result and simulated result in Sentaurus for inverter at normal temperature. The analytical results match the simulated results closely. It is observed that both HMOS and modified HMOS reduces the gate leakage current to great extent as compared to the conventional inverter. The reason is obvious due to increase in physical thickness of gate dielectric and elimination of source/drain-to-gate overlap region in MOSFET structure. Similar analysis can be applied to NAND gate, NOR gate etc.

7 Conclusion

In summary, gate leakage aspect of 35 nm modified HMOS has been analysed with simplified and compact analytical gate current model including nanoscale effect (NSE). A significant gate leakage reduction is demonstrated by HMOS as well by modified HMOS using HfO_2 as gate dielectric. Excellent short channel effects (SCE) are, also, demonstrated for 35 nm MHMOS. Further, short channel effects (SCE) are improved by the use of modified HMOS. These results suggest that modified HMOS is a promising candidate for the future low leak VLSI application.

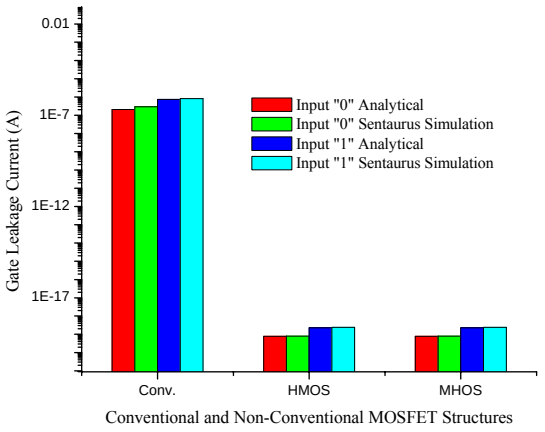


Fig. 17 Inverter gate leakage current with input vector "0" and "1" calculated by using analytical model and Sentaurus simulator.

References

[1] Kahng D., "A historical perspective on the development of MOS transistors and related devices," *IEEE Transaction on Electron Devices*, Vol. 23, No. 7, pp. 655-657, 1976.

[2] Ono M., Saito M., Yoshitomi T., Fiegna C., Ohguro T. and Iwai H., "A 40 nm gate length nMOSFETs", *IEEE Transaction on Electron Devices*, Vol. 42, No. 10, pp.1822-1830, 1995.

[3] Taur Y., Buchanan D. A., Chen W., Frank D. J., Ismail K. E., Lo S. H., Sai-Halasz G. A., Viswanathan R. G., Warn H. J. C., Wind S. J. and Wong H. S., "CMOS scaling into the nanometre regime", *Proceeding IEEE*, Vol. 85, No. 4, pp. 486-504, 1997.

[4] International Technology Roadmap for Semiconductors, *http: //public.itrs.net/Files /2001 ITRS /Home.html.*

[5] Taur Y., "CMOS Design Near the Limits of Scaling," *IBM J.R&D*, Vol. 46, No. 2/3, pp. 213-222, Mar./May 2002.

[6] Sirisantana N., Wei L. and Roy K., "High Performace Low-Power CMOS Circuits Using Multiple Channel Length and Multiple Oxide Thickness," *in Proc. of IEEE ICCD*, pp. 227-232, 2000.

[7] Choi C. -H., Nam K. Y., Yu Z. and Dutton R. W., "Impact of gate direct tunneling current on circuit performance: A simulation study", *IEEE Trans. Electron Devices*, Vol. 48, No. 12, pp. 2823-2829, 2001.

[8] Hamzaoglu F. and Stan M., "Circuit-Level Techniques to Control Gate Leakage for sub 100nm CMOS", *Proc. ISLPED*, pp. 60-63, 2002.

[9] Roy K., Mukhopadhyay S. and Meimand H. M., "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer

CMOS Circuits", *Proceedings of the IEEE*, Vol. 91, No. 2, pp. 305-327, 2003.

[10] Lee D., Blaauw D. and Sylvester D., "Analysis and Minimization Techniques for Total Leakage Considering Gate Oxide Leakage," *in Proc. Of ACM/IEEE DAC*, pp. 175-180, 2003.

[11] Lee D., Blaauw D. and Sylvester D., "Gate Oxide Leakage Current Analysis and Reduction for VLSI Circuits," *IEEE Transactions on VLSI Systems*, Vol. 12, No. 2, pp. 155-166, 2004.

[12] Sultania A. K., Sylvester D. and Sapatnekar S. S., "Tradeoffs Between Gate Oxide Leakage and Delay for Dual T_{ox} Circuits", *in Proceedings of Design Automation Conference*, pp. 761-766, 2004.

[13] Sirisantana N. and Roy K., "Low-power Design using Multiple Channel Lengths and Oxide Thicknesses", *IEEE Design & Test of Computers*, Vol. 21, No. 1, pp. 56-63, 2004.

[14] Mohanty S. P. and Kougianos E.,"Modeling and Reduction of Gate Leakage during Behavioral Synthesis of Nano CMOS Circuits", *In Proceedings of the 19th IEEE International Conference on VLSI Design (VLSID)*, pp. 83-88, 2006.

[15] Lee H., Lee J. and Shin H., "DC and AC Characteristics of Sub-50-nm MOSFETs with Source/Drain-to-Gate Non-overlapped Structure", *IEEE Transactions on Nanotechnology*, Vol. 1, No. 4, pp. 219-225, 2002.

[16] Ghani T., Mistry K., Packan P., Thompson S., Stettler M., Tyagi S. and Bohr M., "Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors", *Tech. Dig. VLSI Sym.*, pp. 174-175, 2000,

[17] ISE TCAD: *Synopsys Santaurus Device simulator*.

[18] Rana A. K., Chand N. and Kapoor V., "Analysis and application of Hybrid MOSFET Structure for Low Gate Leakage", *Journal of Engineering and Applied Sciences*, Vol. 6, No. 1, pp. 39-46, 2011.

[19] Tyagi H. K. and George P. J., "Tunneling currents through ultra thin $HfO_2/Al_2O_3/HfO_2$ triple layer gate dielectrics for advanced MIS devices", *J Mater Sci: Mater Electron,* Vol. 19, No. 8/9, pp. 902-907, 2008.

[20] Chen S. Y., Chen H. W., Chiu F. C., Liu C. H., Hsieh Z. Y., Huang H. S. and Hwang H. L., "Interfacial and Electrical Characterization of HfO_2-Gated MOSCs and MOSFETs by C-V and Gated-Diode Method", *ECS Trans.*, Vol. 16, No. 5, pp. 131-138, 2008.

[21] Vishnyakov A. V., Novikov Y. N., Gritsenko V. A. and Nasyrov K. A., "The charge transport mechanism in silicon nitride: Multi-phonon trap ionization", *Solid State Electronics,* Vol. 53, No. 3, pp. 251-255, 2009.

[22] Sekine K., Saito Y., Hirayama M. and Ohmi T., "Highly Robust Ultrathin Silicon Nitride Films Grown at Low-Temperature by Microwave-Excitation High-Density Plasma for Giga Scale Integration", *IEEE Transactions on Electron Devices*, Vol. 47, No. 7, pp. 1370-1374, 2000.

[23] Kam H., Lee D. T., Howe R. T. and King T.-J., "A new nano-electro-mechanical field effect transistor (NEMFET) design for low-power electronics", *IEDM Tech. Digest*, pp. 463-466, 2005.

[24] Dadgour H. F. and Banerjee K., "Design and analysis of hybrid NEMS –CMOS circuit for ultra low power applications", *Design Automation Conference (DAC)*, pp 306-311, 2007.

Ashwani K. Rana was born in Kangra, H.P., India in 1974. He received his B.Tech degree in Electronics and Communication Engineering from National Institute of Technology, Hamirpur, India in 1998 and M.Tech degree in VLSI Technology from Indian Institute of Technology, Roorkee, India in 2006. He is currently pursuing the Ph.D degree in nano devices from National Institute of Technology, Hamirpur, India. Presently he is with Department of Electronics and Communication Engineering, National Institute of Technology, Hamirpur, India, as an Assistant Professor. His research interest include modeling of semiconductor devices, low power high performance VLSI circuit design and emerging integrated circuit technologies. He has more than 10 publications in International/National Journal & conferences and guided more than 10 M.Tech students in these areas. He is member of ISTE.

Narottam Chand received his PhD degree from IIT Roorkee in Computer Science and Engineering. Previously he received MTech and BTech degrees in Computer Science and Engineering from IIT Delhi and NIT Hamirpur respectively. Presently he is working as Head, Department of Computer Science and Engineering, NIT Hamirpur. He also served as Head, Institute Computer Centre, NIT Hamirpur from February 2008 to July 2009. He has coordinated different key assignments at NIT Hamirpur like Campus Wide Networking, Institute Web Site, Institute Office Automation. His current research areas of interest include mobile computing, mobile ad hoc networks and wireless sensor networks. He has published more than 50 research papers in International/National journals & conferences and guiding six PhDs in these areas. He is member of ISTE, CSI, International Association of Engineers and Internet Society.

Vinod Kapoor was born at Mandi town in Himachal Pradesh, India. He received his BE Degree in Electronics&Communication Engineering from National Institute of Technology (formerly Regional Engineering College), Durgapur, West Bengal, in the year 1987 and Masters Degree in Electronics & Control from Birla Institute of Technology & Science, Pilani (Rajasthan) in the year 1996. He did his Ph. D. from Kurukshetra University, Kurukshetra in the field of Optical Fiber Communication in Sept.2006. He also obtained his MBA degree with specialization in Human Resources Management in the year 2002. He is presently Professor in the Department of Electronics & Communication Engineering NIT Hamirpur, India. He has coordinated different key assignments at NIT Hamirpur like Training & Placement Officer, Chief Warden (Hostels), organizing short term courses. His research interest includes optical fiber communication and optoelectronics/nano devices. He has published more than 15 research papers in International/National journal & conferences and guiding four Ph.Ds in these areas. He is member of ISTE, IETE and IE.