A Highly Linear LNA with Noise Cancellation for 5.8-10.6 GHz UWB Receivers

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Abstract: This paper presents a new ultra-wideband LNA which employs the complementary derivative superposition method in noise cancellation structure. A pMOS transistor in weak inversion region is utilized for simultaneous second- and third-order distortion cancellation. Source-degeneration technique and two shunt inductors are added to improve the performance at high frequencies. The degeneration inductor resonates at $f_T/2$ and realizes a new input matching technique that widens the bandwidth with decreasing it's quality factor and input capacitance, while flattens the input resistance and also improves the 1dB Compression Point. The shunt inductors resonate at the center frequency of the band and improve the effective bandwidth of noise/distortion cancellation technique. This LNA has been designed in a 0.18 μm CMOS process and consumes 8.3 mA from 1.8 V power supply. The chip area is 0.55 mm^2. The noise figure and voltage gain are 4.48-5.18 dB and 13 dB, respectively. S_{11} is lower than -13.5 dB over 5.8–10.6 GHz and IIP_3 is 14.5–17.5 dBm, IIP_2 is 14–15.5 dBm. This technique improves IIP3 more than 9 dB.

Keywords: ultra-wideband (UWB), low-noise amplifier (LNA), noise cancellation, distortion cancellation, input matching.

1 Introduction

Ultra wideband communication is of great interest due to an endless demand for high data rate portable devices. The large 3.1-10.6 GHz bandwidth available for UWB standards makes a good candidate for high resolution positioning systems. Since a large WiFi interferer in the middle of the UWB band (5 GHz) exist, the band of operation is usually divided into lower-band (3.1-4.85 GHz) and upper-band (5.8-10.6 GHz) [1]. Since the large interferer makes it challenging to utilize the whole bandwidth in UWB systems, designing an LNA as the first block of each receiver for the whole bandwidth doesn't seem to be the best idea. Limiting the design to only upper band of UWB can relax the challenges for 50Ω input matching over the bandwidth, and may provide better noise and linearity performance while the power consumption is minimized.

As the CMOS technology scales down, the noise and the bandwidth of the LNA can be improved [2]. However, the linearity will degrade due to nonlinear output conductance, mobility degradation, velocity saturation, and poly-gate depletion. Therefore, using a linearization technique is inevitable in LNA circuits at high data rate [3], while noise cancellation scheme could be incorporated to achieve lower noise figure.

The noise cancellation techniques in [1, 4, 5] improve the LNA noise figure by cancelling the channel thermal noise of CG transistor through adding CS-stages band subtracting the two outputs, while their IIP3 is lower than 0 dBm. Often for linearity improvement in UWB LNAs, the derivative superposition and post-distortion cancellation techniques employ additional transistor's nonlinearity [3, 6, 7] or an active nonlinear resistor [3, 8] to cancel out the nonlinearity terms of the main device, while the additional transistor degrades the noise figure and shrinks the bandwidth. Also, input matching is degraded in derivative superposition methods. A broadband LNA topology is proposed in [2] for simultaneous noise and distortion cancellation which is suitable for improving both noise figure and linearity while the input matching is degraded.

In this paper, a two-stage UWB noise and distortion cancellation LNA is introduced with new input matching network. In the proposed LNA a pMOS transistor in CS-stage is employed for simultaneous second- and third-order distortion cancellation, similar to complementary derivative superposition techniques in CS and CG topologies. In addition, two additional

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inductors are used, which extends the effective bandwidth for input matching and noise/distortion cancellation.

The reminder of this paper is organized as follows. Section 2 presents the new input matching technique which is appropriate for noise cancellation topologies. Section 3 describes the noise cancellation criteria and the method for solving the problem of parasitic in high frequency. Section 4 gives an analytical description of the gain and distortion cancellation by using frequency dependent analysis. Finally, section 5 presents the simulation results and section 6 concludes the paper.

2 UWB Input Matching Analysis

Two typical topologies for LNA input matching are presented in Fig. 1(a) and Fig. 1(b), namely inductor degeneration common-source LNA (CS-LNA) and common-gate LNA (CG-LNA), respectively. In Table 1, $Z_{in}(\omega)$, the input impedance seen from R_S, and the input matching network's quality factor, Q_{match}, are listed. For simplicity all parasitics and body effects, except gate-to-source parasitic capacitors, are ignored.

Considering the inverse relationship between Q_{match} and bandwidth, the relatively high Q_{match} of ordinary CS-LNA leads to impractical UWB matching requirement and smaller NF compared to that of CG-LNA [8]. In CG-LNA the parallel resonant network results in low Q_{match} which is proportional to C_{gs}. This capacitor decreases as technology scales, leading to wider bandwidth. The CG-LNA has also better linearity and lower power consumption [8, 9].

A new input matching technique for noise cancellation topologies is proposed in Fig. 1(c). This technique employs the properties of CS-LNA and CG-LNA to expand the bandwidth of input matching. In this topology, L_{in} resonates in center frequency of band, resonating out parasitic capacitors. For proper cancellation of parasitic capacitors, the inductor L_{new} resonates in the half of transit frequency ($f_T/2$). Hence, C_{gs2} decreases with the frequency dependent factor A (as defined in Table 1), which leads to lower capacitance and better input matching. The calculated Q_{match} in Table 1 is low enough for UWB application. For example, $C_{gs1}+C_p$=0.12 pF and C_{gs2}/A=0.14 pF yield $Q_{match}(f$ = 8 GHz) = 0.33 and BW = 24.5 GHz (all parameters like C_{gs1}, C_p, and etc. defined in Fig. 1(c)).

For ordinary noise cancellation and LNA's input matching design, $R_S=1/g_{m1}$ but in new technique, $R_S=1/g_{m1}||(g_{m2}L_{new}/C_{gs2}+R(\omega))$. Considering this equation, the required g_{m1} is reduced. Therefore, the mean-squared channel thermal noise current, which is given by Eq. (1) and the bias current, are decreased. With low bias current, the load resistor can be larger, which in turn compensates the gain degradation due to g_{m1} decrement in proposed LNA.

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f = 4kT\frac{\gamma}{\alpha}g_m\Delta f \quad (1)$$

$R_{in}=1/g_{m1}||(g_{m2}L_{new}/C_{gs2}+R(\omega))$ is the simplified equation for input resistance. As frequency increases, g_{m1} is degraded and hence $1/g_{m1}$ ascends. $R(\omega)$ is a decreasing function of frequency and hence it compensates the bad effect of higher frequency on g_{m1}.

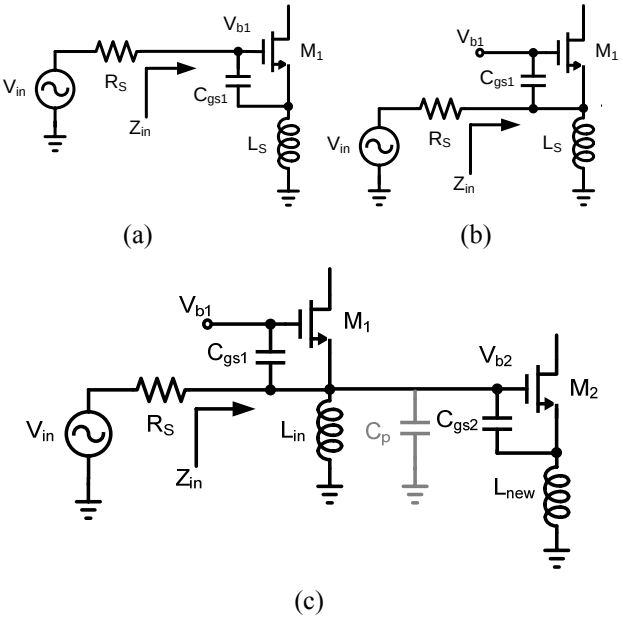


Fig. 1 (a) Typical inductor degeneration common-source LNA, (b) Typical common-gate LNA, (c) Noise cancellation LNA with new input matching technique.

Table 1 CS-LNA and CG- LNA versus noise cancellation LNA with new input matching technique

Topology	$Z_{in}(\omega)$ seen from R_S	Q_{match}
CS-LNA	$\frac{g_{m1}L_s}{C_{gs1}}+j\omega L_s+\frac{1}{j\omega C_{gs1}}$	$\frac{1}{2\omega C_{gs1}R_S}$
CG- LNA	$\frac{1}{g_{m1}}\|\| j\omega L_s \|\| \frac{1}{j\omega C_{gs1}}$	$\frac{\omega C_{gs1}R_S}{2}$
Noise cancellation LNA with new input matching technique	$\frac{1}{g_{m1}}\|\|sL_{in}\|\|\frac{1}{j\omega(C_{gs1}+C_p)}\|\|(\frac{g_{m2}L_{new}}{C_{gs2}}+j\omega L_s+\frac{1}{j\omega C_{gs2}})$	$\frac{\omega(C_{gs1}+C_p+{}^{C_{gs2}}\!/_{A})R_S}{2}, A>1$

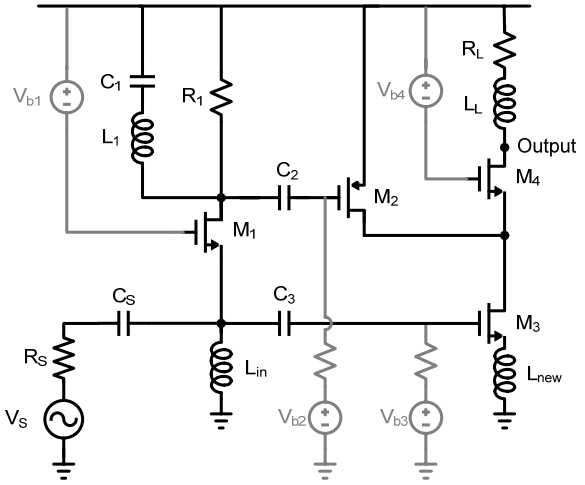


Fig. 2 Complete LNA schematic.

3 UWB Noise Cancellation Analysis

Noise cancellation in broadband LNA is an effective technique to improve the NF [4, 2, 5, 10].The complete schematic of the proposed LNA, with additional L_1 and L_{new} inductors, is depicted in Fig. 2 which is similar to that in [2, 5].

Accurate noise analysis at high frequency requires taking into account the parasitic capacitances at various nodes. The power spectral density of output noise voltage due to R_S is:

$$S_{R_S}(s)=4KTR_S\left|\frac{g_{m3}}{sL_{new}\left(sC_{gs3}+g_{m3}\right)+1}+\frac{1+g_{m1}r_{o1}}{1+r_{o1}/Z_1}g_{m2}\right|^2 \times\left|\frac{Z_X \parallel \frac{1}{g_{m1}}}{Z_S+\left(Z_X \parallel \frac{1}{g_{m1}}\right)}\right|^2 \times|Z_L|^2 \quad (2)$$

where $Z_N= sL_{new}+(1/sC_{gs3})+g_{m3}L_{new}/C_{gs3}$, $Z_L=R_L+sL_L$, $Z_X=(1/sC_X)||sL_{in}||Z_N$, $Z_S=R_S+(1/sC_S)$, $Z_1=R_1||(1/sC_1+sL_1)$, $Z_T=Z_S||(1/g_{m1})||(r_{o1}Z_S/(Z_1+Z_S))||Z_N$ and also refer to Fig. 3 for definition of parasitic capacitor, C_X. The noise factor is the noise contributed by the elements normalized to the noise contributed by R_S, $F=V^2_{n,out}/S_{Rs}(s)$.

By ignoring $r_{o2,3}$ and considering only thermal noise of resistors and channel thermal noise current of MOSFETs, we have:

$$F_{R_1}=\frac{\frac{4KT}{R_1}\left|Z_1\right|^2 g_{m2}^2\left|Z_L\right|^2}{S_{R_S}(s)} \quad (3)$$

$$F_{M_1}=4\mathrm{KT}\frac{\gamma}{\alpha}g_{m1}\frac{\left|Z_T\right|^2}{\left|Z_s \parallel Z_X\right|^2}\times \quad (4)$$

$$\frac{\left|Z_1 g_{m2}-\left(Z_s \parallel Z_X\right)\frac{g_{m3}}{sL_{new}\left(sC_{gs3}+g_{m3}\right)+1}\right|^2\left|Z_L\right|^2}{S_{R_S}(s)}$$

$$F_{M_2}=\frac{4KT\frac{\gamma}{\alpha}g_{m2}\left|Z_L\right|^2}{S_{R_S}(s)} \quad (5)$$

$$F_{M3}=\frac{4KT\frac{\gamma}{\alpha}g_{m3}\left|Z_L\right|^2}{S_{R_S}(s)} \quad (6)$$

where the noise parameter in MOSFET is γ, $\alpha=g_m/g_{d0}$ and $g_{d0}\approx g_m+g_{mb}$ [2, 11].

The effect of the CG transistor M_4 and load resistor on the noise and frequency response is neglected [9]. The noise factor of circuit is summarized by $F=1+F_{R1}+F_{M1}+F_{M2}+F_{M3}$. At frequencies well below f_T, the noise factor of LNA is revealed in Eq. (7), considering only thermal noise of resistors and channel thermal noise current of MOSFETs.

$$F=1+\frac{g_{m2}^2R_1}{R_L^{-2}R_s^{-1}\times\left(R_s \parallel R_{in}\right)^2\times A_v^2}+ \frac{\frac{\gamma}{\alpha}\left(g_{m1}\left(\frac{1}{1+g_{m1}R_S+\frac{R_S+R_1}{r_o}}\right)\left(R_1g_{m2}-\left(R_s \parallel \frac{g_{m3}L_{new}}{C_{gs3}}\right)g_{m3}\right)^2+g_{m2}+g_{m3}\right)}{R_L^{-2}R_s^{-1}\times\left(R_s \parallel R_{in}\right)^2\times A_v^2} \quad (7)$$

$$R_{in}=\frac{R_1+r_{o1}}{1+g_{m1}r_{o1}} \parallel \frac{g_{m3}L_{new}}{c_{gs3}} \quad and \quad (8)$$

$$A_v=-\left(g_{m3}+g_{m2}\left(\frac{1+g_{m1}r_{o1}}{1+\frac{r_{o1}}{R_1}}\right)\right)\times R_L$$

The Noise Figure contours are plotted by varying g_{m2} and g_{m3} in Fig. 4, using Eq. (7).The dash line stands for 8 mA constant current consumption of M_2 and M_3, assuming 0.16 V for overdrive voltage. Intercept point of dash line and NF contours represent the optimum bias point with minimum current consumption for a given NF.

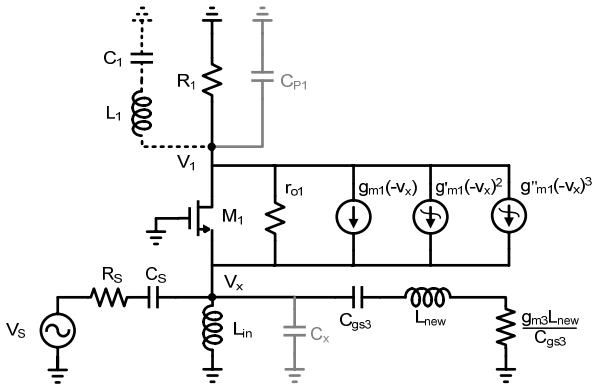


Fig. 3 Common-gate schematic for distortion and noise analysis.

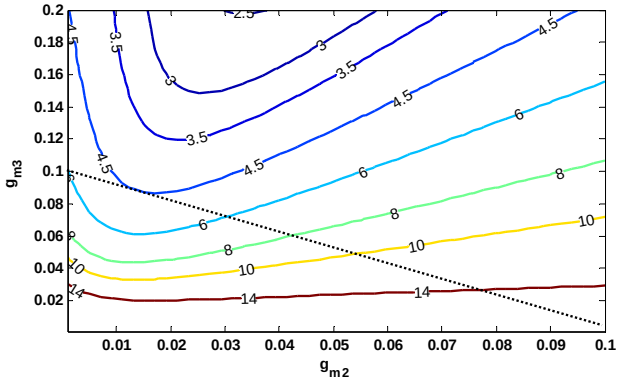


Fig. 4 NF contours with different g_{m2}, g_{m3} at g_{m1}=10 mA/V, C_{gs}=180 fF, L_{new}=220 pH, R_1=200 Ω, $g_{m1}r_{o1}$=54, γ/α=1.8/0.78

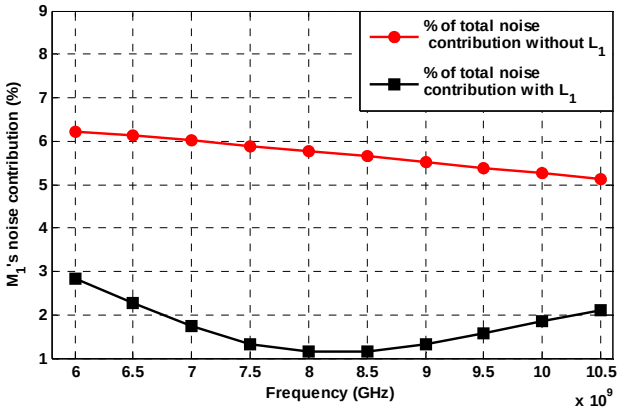


Fig. 5 Simulated noise contribution of M_1 with and without L_1.

The optimized value for noise cancellation is not equal to $g_{m2}\times R_1=g_{m3}\times(R_S||g_{m3}L_{new}/C_{gs3})$ due to frequency dependent nature of Z_1 and Z_{in} in drain and source of M_1, as shown in Fig. 3. Parasitic capacitors C_X, C_{gs3}/A, and C_1 at high frequency cause the impedance to roll off, giving rise to partial noise cancellation. By using inductor L_1 in parallel with R_1 (see dash line in Fig. 3), parasitic capacitors are compensated by L_{in} and the shunt inductor L_1. Thus, the effective bandwidth of noise cancellation is extended. Up to this point the size and bias of M_1, M_2, and M_3 with the values of R_1, L_1, and L_{in} are chosen. These values determine the effect of noise cancellation and hence the Noise Figure of this LNA.

To display the effectiveness of this noise cancelling technique, inductors L_{in} and L_1 are determined such that they resonate with capacitors C_X, C_{gs3}, and C_1 at the center frequency of band, while L_{new} is neglected. The percentage of M_1's channel thermal noise current contributed to total output noise is simulated and compared to that of noise cancelling case with and without L_1, as shown in Fig. 5. Clearly, adding L_1 significantly decreases the noise contribution of M_1's channel thermal noise current.

With this technique, Noise Figure, IIP3, and voltage gain are improved. The effectiveness of adding this inductor in NF improvement is shown in Fig. 5. The importance of this inductor and its value in IIP3 and voltage gain will be discussed in the next section.

4 UWB Distortion Cancellation and Gain Analysis

The distortion of the LNA output voltage in Fig. 2 is caused by the nonlinear drain current of CS and CG transistors, considering resistors R_1 and R_L linear. The nonlinear transconductance, g_m and the nonlinear drain conductance, g_{ds} lead to nonlinear drain current.

The distortion due to g_{ds} is negligible when small shunt resistor is used [2]. The nonlinear small signal drain current is expressed by power series as

$$i_{ds}=g_m\times v_{gs}+\frac{g'_m}{2!}\times v_{gs}^{\,2}+\frac{g''_m}{3!}\times v_{gs}^{\,3}+\cdots \tag{9}$$

For distortion analysis, we employ the schematic of CG-stage shown in Fig. 3. As described in previous section, C_{P1} and C_X are the parasitic capacitors. C_S is the input coupling capacitor. The equivalent input impedance of M_3 is also modeled by the RLC network of C_{gs3}, L_{new}, and $g_{m3}L_{new}/C_{gs3}$. To examine the frequency dependent distortion analysis, we assume that C_{P1} and C_X account for the bandwidth limiting capacitances and employ Volterra series for the CG-stage. To reduce the complexity, the linearity analysis will be limited up to the third-order and the memory-less Taylor series applied to CS-stages [2]. By denoting:

$$V_X=A_1(s)\circ V_S+A_2(s_1,s_2)\circ V_S^{\,2}+A_3(s_1,s_2,s_3)\circ V_S^{\,3} \tag{10}$$

Volterra series kernels are derived by solving some KCL, where $Z_X=(1/sC_X)||sL_{in}||(sL_{new}+(1/sC_{gs3})+g_{m3}L_{new}/C_{gs3})$, $Z_S=R_S+(1/sC_S)$, and $Z_1=R_1||(1/sC_{P1})||(sL_1+1/sC_1)$, The second-order interaction operator is $\overline{A_1(s_1)A_2(s_2,s_3)}$. The Volterra series kernels are derived as:

$$A_1(s)=\frac{Z_1(s)+r_{o1}}{H(s)} \tag{11}$$

$$A_2(s_1,s_2)=\frac{\frac{1}{2}g'_{m1}r_{o1}Z_S(s_1+s_2)A_1(s_1)A_1(s_2)}{H(s_1+s_2)} \tag{12}$$

$$A_3(s_1,s_2,s_3)=-Z_S(s_1,s_2,s_3)r_{o1}\times \frac{(-g'_{m1}\overline{A_1(s_1)A_2(s_2,s_3)}+\frac{1}{6}g''_{m1}A_1(s_1)A_1(s_2)A_1(s_3))}{H(s_1+s_2+s_3)} \tag{13}$$

$$H(s)=Z_S(s)(1+g_{m1}r_{o1})+\left(Z_1(s)+r_{o1}\right)\left(1+\frac{Z_S(s)}{Z_X(s)}\right) \tag{14}$$

while the V_{out} is expressed by Eq. (15) with amplified V_1 and V_{gs3} as:

$$V_{out}=(-(g_{m2}(-V_1)+\frac{g'_{m2}}{2!}(-V_1)^2+\frac{g''_{m2}}{3!}(-V_1)^3)+(g_{m3}V_{gs3}+\frac{g'_{m3}}{2!}V_{gs3}^{\,2}+\frac{g''_{m3}}{3!}V_{gs3}^{\,3}))\times Z_L(s) \tag{15}$$

where $Z_L(s)$ is the output impedance and also

$$V_1=\frac{Z_1(s)(1+g_{m1}r_{o1})}{Z_1(s)+r_{o1}}A_1(s)\circ V_S+\frac{-Z_1(s_1,s_2)}{Z_x(s_1,s_2)\,||\,Z_s(s_1,s_2)}A_2(s_1,s_2)\circ {V_S}^2$$

$$+\frac{-Z_1(s_1+s_2+s_3)}{Z_x(s_1+s_2+s_3)\,||\,Z_s(s_1+s_2+s_3)}A_3(s_1,s_2,s_3)\circ {V_S}^3 \qquad (16)$$

$$V_{out}=(-(g_{m2}(-V_1)+\frac{g'_{m2}}{2!}(-V_1)^2+\frac{g''_{m2}}{3!}(-V_1)^3)+$$
$$(g_{m3}V_{gs3}+\frac{g'_{m3}}{2!}{V_{gs3}}^2+\frac{g''_{m3}}{3!}{V_{gs3}}^3))\times Z_L(s) \qquad (17)$$

Eq. (15) results in fundamental, second-order, and third-order V_{out} expressions as follows:

$$V_{out,fund}=((\frac{1}{L_{new}(s)(c_{gs3}(s)+g_{m3})+1}A_1(s)\circ V_S)\times g_{m}$$
$$+(\frac{Z_1(s)\times(1+g_{m1}r_{o1})}{Z_1(s)+r_{o1}}A_1(s)\circ V_S)\times g_{m2})\times Z_L(s) \qquad (18)$$

$$V_{out,2ed}=((\frac{A_2(s_1,s_2)\circ {V_S}^2}{L_{new}(s_1+s_2)(c_{gs3}(s_1+s_2)+g_{m3})+1})g_{m3}+$$
$$(\frac{-Z_1(s_1+s_2)A_2(s_1,s_2)\circ {V_S}^2}{Z_X(s_1+s_2)\,||\,Z_S(s_1+s_2)})g_{m2}+(\frac{A_1(s)\circ V_S}{L_{new}(s)(c_{gs3}(s)+g_{m3})+1})^2\frac{g'_{m3}}{2!}$$
$$-(\frac{Z_1(s)(1+g_{m1}r_{o1})\times A_1(s)\circ V_S}{Z_1(s)+r_{o1}})^2\frac{g'_{m2}}{2!})\times Z_L(s) \qquad (19)$$

$$V_{out,3rd}=((\frac{A_3(s_1,s_2,s_3)\circ {V_S}^3}{L_{new}(s_1+s_2+s_3)(c_{gs3}(s_1+s_2+s_3)+g_{m3})+1}g_{m3}+$$
$$\frac{-Z_1(s_1+s_2+s_3)A_3(s_1,s_2,s_3)\circ {V_S}^3}{Z_x(s_1,s_2,s_3)\,||\,Z_s(s_1,s_2,s_3)}g_{m2})+(\frac{A_1(s)\circ V_S}{L_{new}(s)(C_{gs3}(s)+g_{m3})+1})^3\frac{g''_{m3}}{3!}$$
$$+(\frac{Z_1(s)(1+g_{m1}r_{o1})A_1(s)\circ V_S}{Z_1(s)+r_{o1}})^3\frac{g''_{m2}}{3!}$$
$$+\frac{\overline{A_1(s)A_2(s_1,s_2)}\circ {V_S}^3}{(L_{new}(s)(c_{gs3}(s)+g_{m3})+1)(L_{new}(s_1+s_2)(c_{gs3}(s_1+s_2)+g_{m3})+1)}g'_{m3}+$$
$$\frac{Z_1(s)\times(1+g_{m1}r_{o1})}{Z_1(s)+r_{o1}}A_1(s)\frac{-Z_1(s_1+s_2)}{Z_x(s_1+s_2)\,||\,Z_s(s_1+s_2)}A_2(s_1,s_2)\circ {V_S}^3(-g'_{m2}))$$
$$\times Z_L(s) \qquad (20)$$

4.1 Gain Analysis

CS topology with source degeneration inductor has L_{new} as the frequency-dependent feedback element while $\beta=\omega L_{new}$. The feedback path is between the output current and the gate-source voltage [3]. For simplicity, we examine these effects with frequency-dependent analysis, using Eq. (18) that displays $V_{out,fund}$ as the voltage gain. The g_{m3}'s factors are affected by L_{new}'s feedback, decreasing the voltage gain. Fig. 6 illustrates the magnitude of this factor by varying frequency and L_{new}.

In the left side of dash line for all frequency and L_{new}, the magnitude is higher than 0.75. With L_{new}<0.225 nH criteria, the voltage gain degradation is tolerable. In contrast, g_{m2}'s factor increases the gain

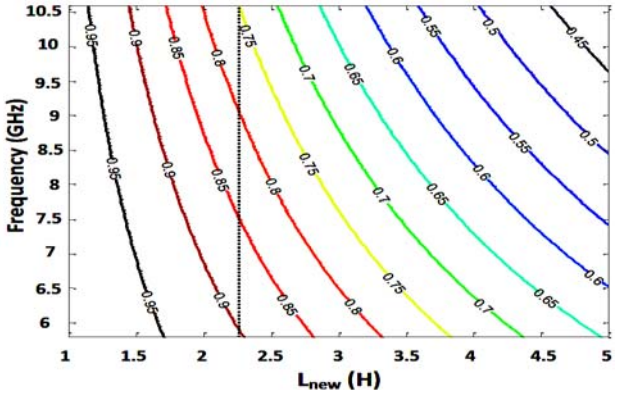


Fig. 6 The magnitude of $\frac{1}{L_{new}(s)(c_{gs3}(s)+g_{m3})+1}$ factor.

when L_1 resonates in the band of interest. The shunt-peaking inductor, L_L, in series with the load resistor, R_L, boosts the gain of the LNA at high frequency while this topology matches the output to 50 Ω, without using an output buffer for measurement.

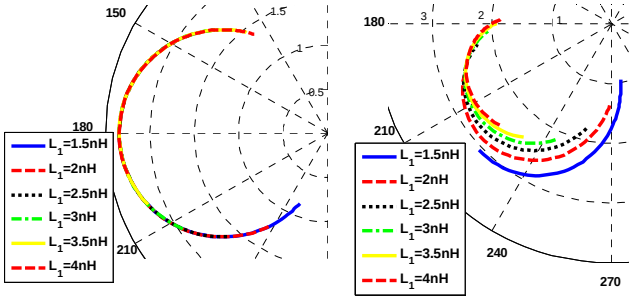
4.2 Distortion Analysis

Previous designs in [6, 7] utilize a pMOS transistor as an auxiliary FET in weak inversion for simultaneous second- and third-order distortion cancellation in complementary derivative superposition method for wideband LNAs, providing acceptable bandwidth. In this work by modifying the complementary derivative superposition method in noise cancellation structure, a pMOS transistor is also used for the same reason as shown in $V_{out,2ed}$. The effect of using pMOS transistor in CS-stage for second-order distortion cancellation is obvious due to the negative sign added to g'_{m2}'s factors. Note that pMOS transistor also reuses the bias current of M_3. In this circuit, we partially cancel the second-order distortion, and concentrate on full cancellation of third-order distortion.

Each term in Eq. (20) contributes to the third-order distortion of V_{out}. The first term is the M_1's distortion and at low frequencies, the ratio of g_{m3} and g_{m2}'s factors are reduced to $(R_s||(g_{m3}L_{new}/C_{gs3}))/R_1$, which cancels out in the same way as the M_1's channel thermal noise current is cancelled in Section 3. The second term in Eq. (20) that is due to third-order distortion of M_2 and M_3 can be cancelled by biasing these two transistors in the weak and strong inversion regions, respectively, with different g''_m's polarity. These two cancellations criteria are formulated as:

$$\frac{g_{m3}}{g_{m2}}=\frac{R_1}{R_S\,||\,\frac{g_{m3}L_{new}}{C_{gs3}}} \quad and \quad \frac{g''_{m3}}{g''_{m2}}=-\frac{R_1}{(1/g_{m1})} \qquad (21)$$

$Z_1(s_1+s_2)$ in the third-term of Eq. (20) is zero in two tone test, when the frequency space between two tones is resonance frequency of C_1 and L_1's resonant tank, which acts as a harmonic trap network. For this application, IM2 is effective in relatively low frequency, and resonant tank decreases both $Z_1(s_1+s_2)$ and third-



(a) (b)

Fig. 7 (a) the ratio of g''_{m3}/g''_{m2} without L_{new} and (b) the ratio of g''_{m3}/g''_{m2} with L_{new} over the bandwidth.

term of Eq. (20). Because of the same polarity of g'_{m2} and g'_{m3} factors, the value of the third-term in Eq. (20) can be substantial because g'_{m2} and g'_{m3} are fixed, once M_2 and M_3 are designed to satisfy Eq. (21) However, the size of M_1 can be decreased because of new input matching technique such that $A_2(s_1,s_2)$ is diminished by lowering g'_{m1}.

In the next step, high frequency effects are considered to deconvolve Eq. (20). In this case, g''_{m3} and g''_{m2} are frequency dependent, and for better distortion cancellation the criteria can be formulated as

$$\frac{g''_{m3}}{g''_{m2}} = -\frac{\left(\frac{Z_1(s)\times(1+g_{m1}r_{o1})}{Z_1(s)+r_{o1}}A_1(s)\circ V_S\right)^3}{\left(\frac{A_1(s)\circ V_S}{L_{new}(s)\left(c_{gs3}(s)+g_{m3}\right)+1}\right)^3} \qquad (22)$$

For proper distortion cancellation and extending the bandwidth of this cancellation, the ratio in Eq. (22) should have constant amplitude and phase π over the entire bandwidth. In this topology, adding two inductors, L_{new} and L_1, provides two degrees of freedom for improving the linearity. By plotting Eq. (22) with and without L_{new} and by varying L_1 in Fig. 7, the effect of this technique is revealed.

Taking into account the input matching condition and the contours in Fig. 6, L_{new} is chosen to be 0.22 nH. The inductor L_1, which resonates with parasitic capacitors in V_1, decreases the noise contribution of CG-stage. The proper value for this inductor forces it to resonate in the center of the required band. From Fig. 7, the inductance value must be higher than 2 nH. We choose 2 nH due to area constrain.

5 Simulation Results

The post-layout simulation of the proposed LNA in Fig. 2 is designed with a RF CMOS of 0.18µm. Fig. 8 shows the input and output return losses. This figure illustrates that the new input matching strongly decreases the input return loss. Figs. 9 and 10 show the voltage gain and noise figure, respectively. Note that the effect of L_1 is obvious because of Low noise figure in resonance frequency of L_1. For linearity analysis IIP3 and IIP2 are shown in Fig. 11. IIP3 in Fig. 11 is obtained by varying two frequency tones with 200 MHz spacing, and for IIP2 measurement 1 GHz spacing frequency is used. In Fig. 12 spacing is swept while one of the input tones is in the center frequency. Fig. 13 and Fig. 14 show, respectively, IIP3 and 1dB compression point with sweeping input power. In all figures, post-layout simulation is compared with pre-simulation results. Also, Fig. 15 shows layout of proposed LNA.

Finally, the performance of the proposed LNA is compared in Table 2 with simulation results of prior designs to exhibit the benefits of the proposed circuit in high frequency. All transistors size and other component values are reported in Table 3.

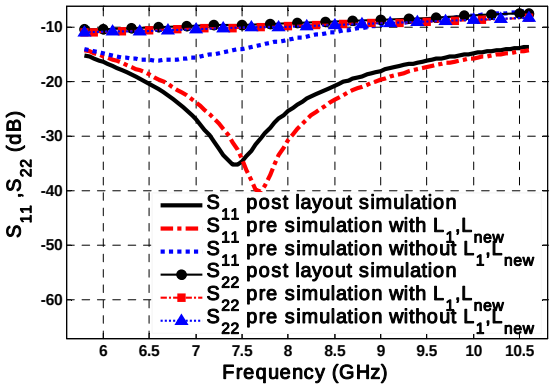


Fig. 8 Simulated S-parameters, S_{11},S_{22} and Voltage Gain.

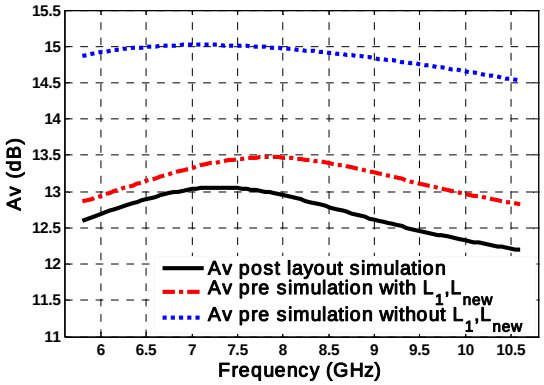


Fig. 9 Simulated Voltage Gain.

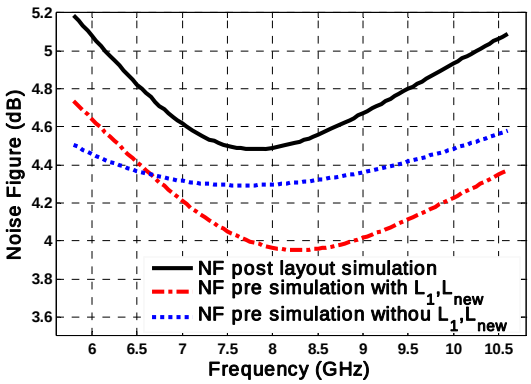


Fig. 10 Simulated Noise Figure.

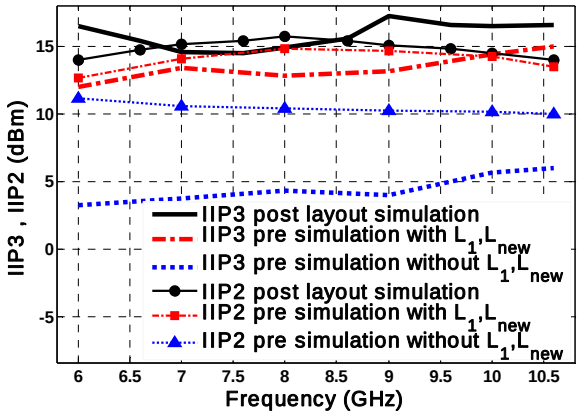


Fig. 11 Simulated IIP3 and IIP2 versus intermodulation frequency.

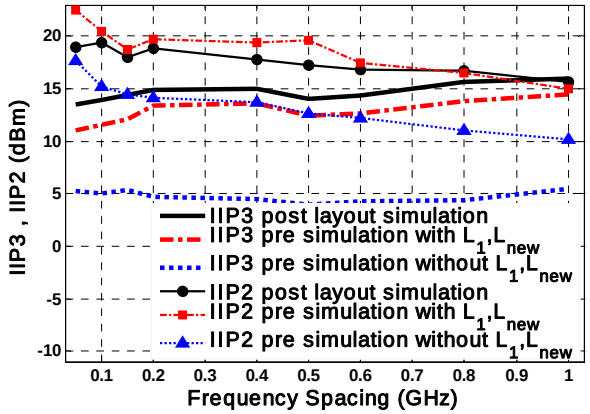


Fig. 12 Simulated IIP3 and IIP2 versus frequency spacing.

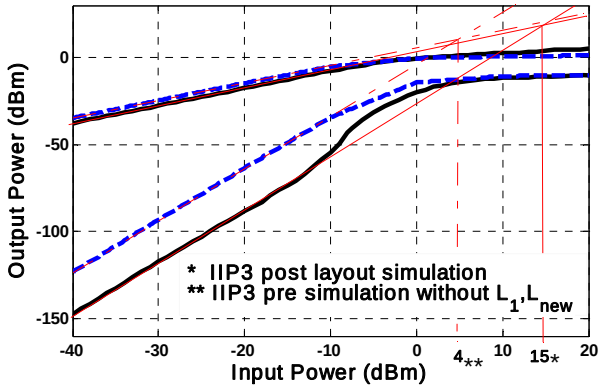


Fig. 13 simulated IIP3 in 8 GHz.

6 Conclusion

A highly linear LNA with noise cancellation for 5.8–10.6 GHz UWB receivers has been designed in a 0.18 µm CMOS technology. A new input matching technique is examined. The Volterra series kernels prove that additional inductors, which are added for input matching and noise cancellation, can be optimized to improve the distortion cancellation in the above bandwidth. The proposed circuit incorporates pMOS with nMOS in the common-source stages to realize simultaneous cancellation of second- and third-order distortion. Simulation results show that the maximum gain is13dB and noise figure is below 5.2 dB over the upper-band of UWB. The input matching provide S_{11}<-13.5 dB while S_{22}<-7.5 dB, S_{12}<-34.5 dB. The IIP3 and IIP2 of linear LNA are over 14 dBm, while consumes only 15 mW from1.8 V supply. The chip area is 0.55 mm^2.

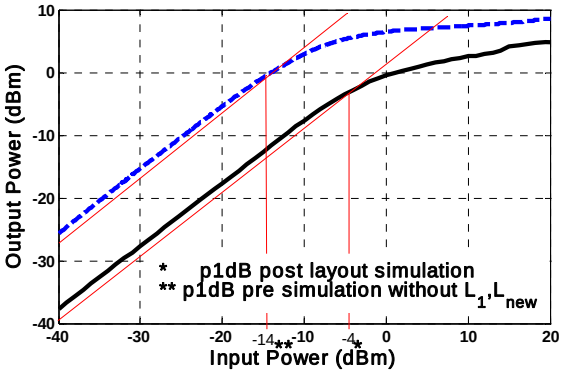


Fig. 14 Simulated 1-dB compression point in 8 GHz.

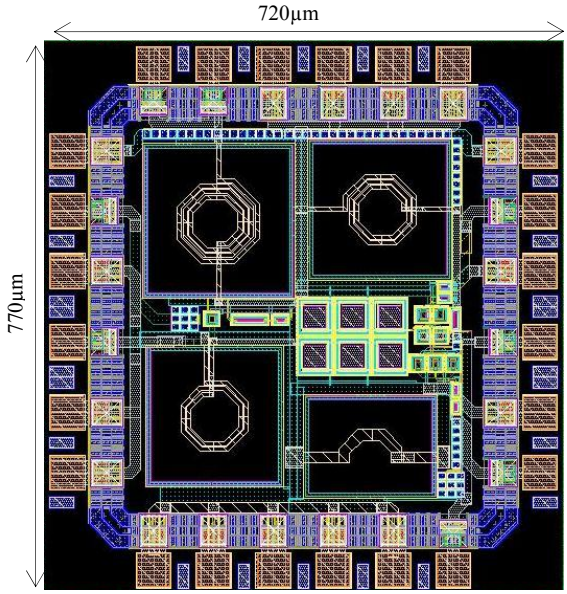


Fig. 15 Layout of proposed LNA.

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Table 2 Simulation Results Comparison with prior works

Ref	Frequency band [1)] (GHz)	NF (dB)	Gain (dB)	S_{11} (dB)	IIP3 (dBm)	IIP2 (dB)	Power (mW)	Supply voltage (V)	Area (mm^2)	Technology
This Work	5.8-10.6	4.48-5.18	13[2)]	<-13.5	+15	+16	15	1.8	0.55	0.18µm
[1]	4.7-11.7	2.88-3	12.4	<-11.9	-3	-	13.5	1.2	-	0.13 µm
[10]	0.2-5.2	2.6-3.3	16.6[2)]	<-13	0	+20	21	1.2	0.009[3)]	65nm
[4]	3.1-10.6	3.8-4.3	11	<-12	-6.2	-	20	1.8	0.59	0.18µm
[8]	1.5-8.1	3.4-6	11.8	<-9	+14.1	+23	2.62	1.3	0.58	0.13 µm
[2]	0.8-2.1	2.25-2.4	14.5[2)]	<-8.5	+16	-	17.4	1.5	0.65	0.13 µm

[1)] 3 dB BW except this work and [4] [2)] A_V [3)] Active area

Table 3 Device Dimension

$\mathbf{M_1}$	(7.02µm/0.18µm)×5	$\mathbf{C_2,C_3}$	3pF
$\mathbf{M_2}$	(7.02µm/0.18µm)×20	$\mathbf{C_1,C_S}$	15pF
$\mathbf{M_3}$	(7.02µm/0.18µm)×33	$\mathbf{L_1}$	2nH
$\mathbf{M_4}$	(7.02µm/0.18µm)×20	$\mathbf{L_{in}}$	0.7nH
$\mathbf{R_1}$	200Ω	$\mathbf{L_L}$	0.9nH
$\mathbf{R_L}$	80Ω	$\mathbf{L_{new}}$	0.22nH

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