A Sub-µW Tuneable Switched-Capacitor Amplifier-Filter for Neural Recording Using a Class-C Inverter

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***Abstract*— A two stage sub-µW Inverter-based switched-capacitor amplifier-filter is presented which is capable of amplifying both spikes and local field potentials (LFP) signals. Here we employ a switched capacitor technique for frequency tuning and reducing of 1/f noise of two stages. The reduction of power consumption is very necessary for neural recording devices; however, in switched capacitor (SC) circuits OTA is a major building block that consumes most of the power. Therefore an OTA-less technique utilizing a class-C inverter is employed that significantly reduces the power consumption. A detailed analysis of noise performance for the inverter-based SC circuits is presented. A mathematical model useful for analysis of such SC integrators is derived and a good comparison is obtained between simulation and analytical technique. With a supply voltage of 0.7V and using 0.18 µm CMOS technology, this design can achieves a power consumption of about 538 nW. The designed amplifier-filter has the gains 18.6 dB and 28.2 dB for low pass only and cascaded filter, respectively. By applying different sampling frequencies, the filter attains a reconfigurable bandwidth.**

Keywords- Amplifier-filter, Inverter-based switched-capacitor circuit,noise analysis, neural recording.

I. INTRODUCTION

Recent studies in brain-machine interfaces has showed that using local field potentials (LFPs) is necessary especially when chronically implanted microelectrodes functionality decays for recording unit-spike activity [1]. Multi-channel microprobes have the capability of recording both spike trains and LFPs. Spike signals have bandwidths of 200 Hz to 5 KHz and amplitude levels up to ±500 µV, while LFPs bandwidth is 10 Hz to 100 Hz and their amplitudes reaches up to ±5mV [2]. Because of their different characteristics it is difficult to have a stand-alone, small-scale system for simultaneously record them. For the simultaneous recording of both neural signals, the amplifier must have a high dynamic range, which can be limited by the noise performance of an ADC [3].

For recording of this signals, a new architecture that uses a two-stage amplifier structure as shown in fig. 1, has been introduced in [3]. The first stage is a low-pass SC biquad filter with the amplification of 10 times for LFPs and the second stage is a band-pass SC biquad filter with an additional

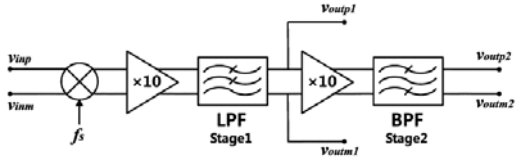


Fig. 1. The proposed system architecture for neural recording in [3]

amplification of 10 times for spikes recording. Each stage bandwidth is reconfigurable by using different sampling clock frequencies. To reduce the 1/f noise it uses the chopper modulation at high frequencies. In their design, operational transconductance amplifier (OTA) is used as an active feedback element in the SC biquad filters.

However, OTA consumes most of the power in SC circuits, and it is difficult to design low-voltage and low-power OTAs in scaled CMOS technologies [4]. This paper uses the architecture shown in fig. 1, but instead of OTA a class-C inverter is applied which enables the design of low-voltage and low-power filters. With this technique the power consumption can be reduced by about 120 times less than that of [3].

The inverters firstly used in SC circuits by [5, 6] and because of their attractive properties for designing low-voltage and low-power circuits, again attract attentions [7-10]. The effect of non-idealities such as finite DC-gain and parasitics is considered for the delta-sigma $(\Delta\Sigma)$ modulators [4]. Although the intrinsic noise of inverters has discussed, but a detailed analysis of entire noise in an inverter-based SC integrator (which is an important block in many SC circuits) does not exist. This paper presents a detailed analysis of entire noise in an inverter-based SC integrator due to both switches and inverter intrinsic noise. In addition, this paper also provides design guidelines to minimize noise in an inverter-based SC integrator. A mathematical model useful for analysis of such integrators is derived and a good comparison is obtained between simulation and analytical technique.

Principle operation of SC circuits that uses a class-C inverter instead of OTA is explored in section II and a detailed analysis of noise is presented in section III. In section IV the design procedure of the circuit is explained. The simulation

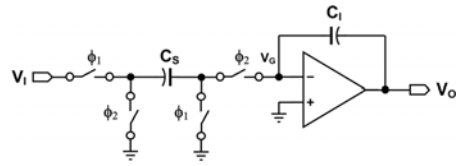
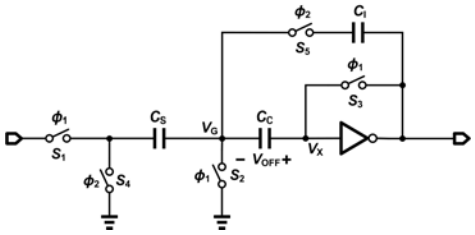
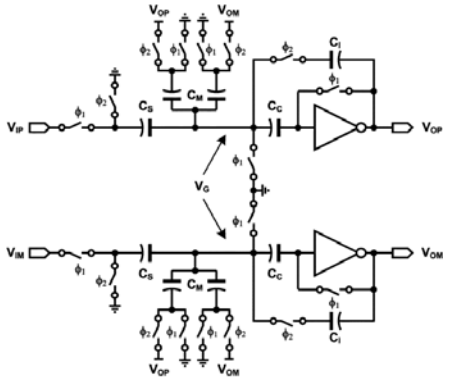


Fig. 2. Typical SC integrator using OTA.



(a)



(b)

Fig. 3. Proposed inverter-based SC integrator in [4]. (a)Single-ended. (b) Pseudo-differential.

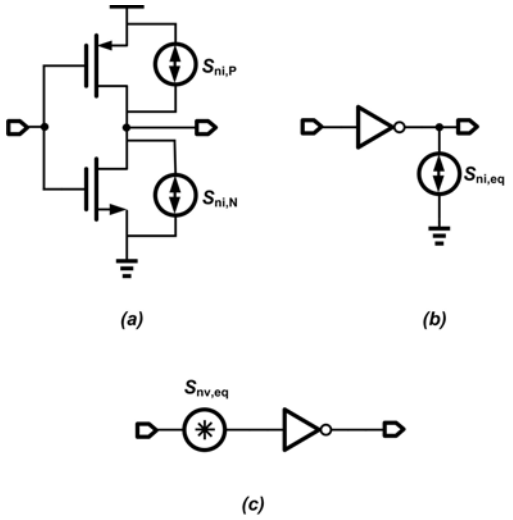


Fig. 4. A simple inverter with (a) device nosies, (b) equivalent output-reffered current and (c) equvalent input-reffered voltage noise sources.

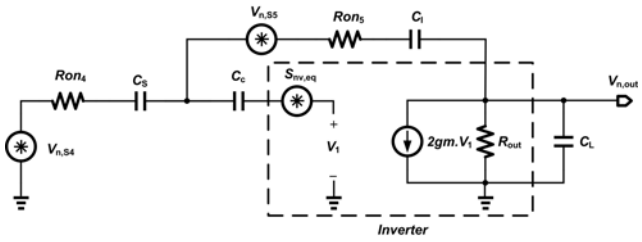


Fig. 5. Equivalent circuit of the integrator under integrating phase.

results is presented in section V, and finally the section VI provides the conclusion.

II. Operation of Inverter-based SC Circuits

A. Inverter-based SC Integrators

Figure 2 illustrates a typical SC integrator that uses an OTA as an active element to perform a negative feedback. It has two non-overlapping phase clocks: sampling (ϕ_1) and integrating phase (ϕ_2). In sampling phase, input signal (v_I) is sampled to sampling capacitor (C_S) and during the ϕ_2 phase the charge is transferred from C_S to integrating capacitor (C_I). Due to the feedback configuration, the node V_G forms a virtual ground.

Instead of using an OTA, a simple logic inverter can be used as an active element in SC circuits. In [4] an structure for inverter-based SC integrator was proposed that uses an auto-zeroing technique to form a virtual ground, as shown in Fig. 3(a). During the sampling phase ϕ_1, the offset voltage of inverter (V_{OFF}) is sampled in C_C. In the ϕ_2 phase, due to the negative feedback, V_X should be equal to V_{OFF}; therefore V_G can form a virtual ground.

Figure 3(b) shows the pseudo-differential inverter-based SC integrator, with common mode feedback (CMFB), proposed in [4]. During the ϕ_1 phase, the CMFB capacitors (C_M) are discharged and during the ϕ_2 phase they form a common mode feedback loop whose gain is defined by C_M/C_I ratio. In the design of differential low-pass-filter (LPF) and band-pass-filter (BPF) biquads we use this architecture that will be explained more in section IV.

B. Class-C Inverters

According to the used supply voltage, the push-pull inverters are classified into class-AB and class-C inverters. If the supply voltage (V_{DD}) is chosen so as to $V_{DD} > V_{TN} + V_{TP}$ in which V_{TN} and V_{TP} are the threshold voltages of NMOS and PMOS transistors, respectively, the inverter behaves as a class-AB amplifier. In this case, the static short circuit current is much more than that of class-C inverters in which V_{DD} is chosen lower than the sum of transistors threshold voltages, namely $V_{DD} < V_{TN} + V_{TP}$. Class-C inverters have much more DC-gain than class-AB inverters; however, the gain-bandwidth product of class-AB inverters is much better [4].

The class-C inverter is a suitable case for low voltage and low power design especially in the above mentioned application, where the signal frequencies are not so high. We use class-C inverters in SC LPF and BPF biquads that will be described in section IV.

III. NOISE ANALYSIS

A. Inverter intrinsic noise

The power spectral density (PSD) of the thermal noise current in an MOS transistor can be expressed [11] as

$$S_{ni,therm}(f) = 4kT\gamma gm, \left[\mathrm{A}^2/\mathrm{Hz}\right] \quad (1)$$

where γ is 2/3 and 1/2 for transistors operating in saturation and weak inversion mode, respectively. Assuming, for the simple class-c inverter shown in fig. 4(a), both transistors has the same transconductance gm . The equivalent PSD of thermal current noise ($S_{ni,eq}(f)$) is the sum of NMOS and PMOS current noise PSDs, i.e. $S_{ni,N}(f)$ and $S_{ni,P}(f)$ (fig. 4(b)).

$$S_{ni,eq}(f) = S_{ni,N}(f) + S_{ni,N}(f) = 4kTgm, \left[\mathrm{A}^2/\mathrm{Hz}\right] \quad (2)$$

Therefore, the input-referred voltage PSD noise of the inverter ,denoted by $S_{nv,eq}(f)$ (fig. 4(c)), is given by

$$S_{nv,eq}(f) = \frac{kT}{gm}, \left[V^2/\mathrm{Hz}\right]. \quad (3)$$

It is noteworthy to mention the flicker noise has much lower effect than thermal noise due to aliasing of thermal noise and the used auto-zeroing technique, cancels out the low frequency flicker noise [12].

B. Analysis of noise in an inverter-based SC Integrator

Analysis of entire noise in an inverter-based SC integrator requires both sampling (ϕ_1) and integrating (ϕ_2) phases to consider. In addition, there are two different noise sources in each phase: inverter intrinsic noise and on-resistance thermal noise of switches.

1) Integrating phase

Figure 5 shows the equivalent circuit of the integrator under integrating phase. R_{out} denotes the output resistance of inverter and the C_L accounts both the parasitic and the next stage capacitors.

a) Effect of inverter intrinsic noise

Firstly, we analyze the effect of inverter intrinsic noise at the integrator output while neglecting the on-resistance of two switches S_4 and S_5.

It is evident that V_1 is equal to the voltage division of $V_{n,out}$ across C_S and C_I plus $V_{n,eq}$ (i.e. $V_1 = V_{n,eq} + V_{out}\left[C_I/(C_I+C_S)\right]$). Applying the KCL at the output node and assuming large enough R_{out} , the transfer function $H(s)$ can be derived as

$$H_1(s) = \frac{V_{n,out}(s)}{V_{n,eq}(s)} = \frac{G_0}{1+s\left(\frac{C_{out}G_0}{2gm}\right)} \quad (4)$$

where the DC gain $G_0 = 1 + \frac{C_S}{C_I}$ and the output capacitance $C_{out} = C_L + \frac{C_I C_S}{C_I + C_S}$.

Therefore, the total integrated noise power can be expressed as

$$\overline{V_{n,out_1}^2} = \int_0^\infty \overline{V_{n,eq}^2(f)}\left|H_1(j2\pi f)\right|^2 df = \frac{kT}{2}\frac{G_0}{C_{out}}. \quad (5)$$

Equation (5) indicates that increasing C_S and C_I so that the ratio of them (also G_0) remains unchanged, cause the lower output-referred noise due to the intrinsic inverter noise.

a) Effect of on-resistance thermal noise of switches

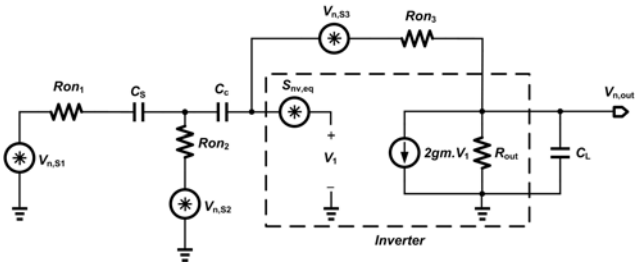
The two switches that appear ON in this phase (i.e. S_4 and S_5) are modeled as Ron_4 and Ron_5 . Each one generates a white noise PSD equal to $4kTRon$ (fig. 5). Since, the noise sources are uncorrelated, the transfer function from each one to the output can be find separately to find the contribution of each one on the entire output noise power. Hereafter, it is assumed both switches have the same Ron for simplicity.

The Transfer functions from V_{n,S_5} and V_{n,S_4} approximately can be expressed as (6) and (7) respectively.

$$H_2(s) = \frac{V_{out}(s)}{V_{n,S_5}} \approx \frac{1}{1 + 2C_L\frac{C_I + C_S}{C_I C_S} + 4RonC_L s} \quad (6)$$

$$H_3(s) = \frac{V_{out}(s)}{V_{n,S_4}} \approx \frac{1}{\frac{C_I}{C_S} + \left(RonC_I + \frac{C_I + C_L}{2gm}\right)s} \quad (7)$$

Thus, the total integrated noise power at the output due to each one is given by



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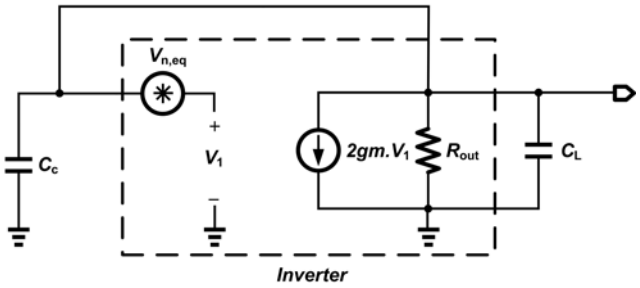

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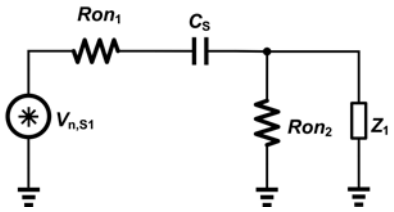


(c)

Fig. 6. (a) Equivalent circuit of the integrator under sampling phase in adition to various noise sources. (b) The simplified circuit for analying the effect of inverter intrinsic noise and (c) the equivalent circuit for deriving the effect of S_1 on-resistance thermal noise on the entire noise behaviour.

$$\overline{V_{n,out_2}^2} = \int_0^\infty \overline{V_{n,S_5}^2(f)}\left|H_2(j2\pi f)\right|^2 df = \frac{kT}{4C_L}\cdot\frac{1}{1+2C_L\dfrac{C_I+C_S}{C_IC_S}} \tag{8}$$

$$\overline{V_{n,out_3}^2} = \int_0^\infty \overline{V_{n,S_4}^2(f)}\left|H_3(j2\pi f)\right|^2 df = \frac{kT}{{C_I}^2}\cdot\frac{C_SR_{on}}{R_{on}+\dfrac{1}{2gm}\left(1+\dfrac{C_L}{C_I}\right)} \tag{9}$$

From (9), it can be noted that the effect of V_{n,S_4} on the output can be neglected if $gmRon \gg 1$.

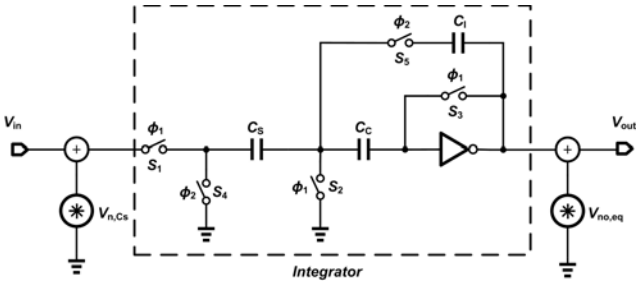


Fig. 7. The overall noise model for the inverter-based SC integrator.

2) Sampling phase

a) Effect of intrinsic inverter noise

The equivalent circuit under sampling phase (ϕ_1) is shown in fig 6 (a) . Under assumption that the switches have very low on-resistance, the transfer function from inverter intrinsic noise to the output can be expressed the same as (4) whereas $C_I \to \infty$ (fig 6(b)). Therefore the total integrated output noise power due to inverter intrinsic noise, can be derived as

$$\overline{V_{n,out_4}^2} = \frac{kT}{2(C_L+C_c)}. \tag{10}$$

It is clear that increasing the C_c can be reduced the effect of inverter intrinsic noise on the total output noise.

b) Effect of on-resistance thermal noise of switches

In this case the three switches S_1,S_2 and S_3 become ON and have contribution on integrator overall noise performance.

Figure 6(c) shows the equivalent circuit for deriving the effect of S_1 thermal noise in which Z_1 denotes the parallel impedance looking into the circuit. Practically, Ron_2 is too small so that Z_1 has no effect. Thus, the total integrated noise appeared across C_s can be written as

$$\overline{V_{n,C_S}^2} = \frac{kT}{2C_S}. \tag{11}$$

The transfer function from output to V_{n,S_2} has a complicated expression that cannot be solved easily. However for having some useful insight for designing purpose, several simplification has made and finally it can be approximated as

$$H_5(s) = \frac{V_{out}(s)}{V_{n,S_2}} \approx \frac{1}{1+\dfrac{C_L}{C_C}+4gmRon+2RonC_Ls}. \tag{12}$$

Therefore, the approximated total integrated output noise power due to V_{n,S_2} will be

$$\overline{V_{n,out_5}^2} = \int_0^\infty \overline{V_{n,S_2}^2(f)}\left|H_5(j2\pi f)\right|^2 df \approx \frac{kT}{2C_L}.\frac{1}{1+\frac{C_L}{C_C}+4gmRon}. \quad (13)$$

Using the approximated transfer function (14) the total integrated noise power due to the thermal noise of switch S_3 can be written as (15).

$$H_6(s) = \frac{V_{out}(s)}{V_{n,S_3}} \approx \frac{1}{1+\frac{C_L}{C_C}+2RonC_L s} \quad (14)$$

$$\overline{V_{n,out_6}^2} = \int_0^\infty \overline{V_{n,S_3}^2(f)}\left|H_6(j2\pi f)\right|^2 df = \frac{kT}{2C_L}.\frac{1}{1+\frac{C_L}{C_C}} \quad (15)$$

Form both (13) and (15) it can be find that, increasing the C_L / C_C ratio (if it is possible) can be reduced the effect of V_{n,S_2} and V_{n,S_3} on the total output noise power.

C. The overall noise model

Figure 7 shows the overall noise model for the inverter-based SC integrator. It consists of two noise sources, the total noise power on C_s which is obtained by (11) and $V_{no,eq}$ denotes the sum of all integrated noise powers given as follows.

$$\overline{V_{no,eq}^2} = \overline{V_{n,out_1}^2} + \overline{V_{n,out_2}^2} + \overline{V_{n,out_3}^2} + \overline{V_{n,out_4}^2} + \overline{V_{n,out_5}^2} + \overline{V_{n,out_6}^2} \quad (16)$$

Thus, from this model the total output-referred noise PSD can be obtained as

$$S_{total}(f) = S_{n,C_S}(f)\left|H(z)\right|^2 + S_{no,eq}(f) \quad (17)$$

where $H(z)$ is the transfer function of the integrator. Since both noise sources in the model fig. 7 are sampled with sampling frequency f_s, the PSDs in (17) should computed as $S_x = 2\overline{V_x^2}/f_s$ in which V_x can be both V_{n,C_s} and $V_{no,eq}$.

Finally, integrating S_{total} over the entire bandwidth gives the total output-referred noise (18).

$$\overline{V_{n,out}^2} = \int_0^\infty S_{total}(f)df \quad (18)$$

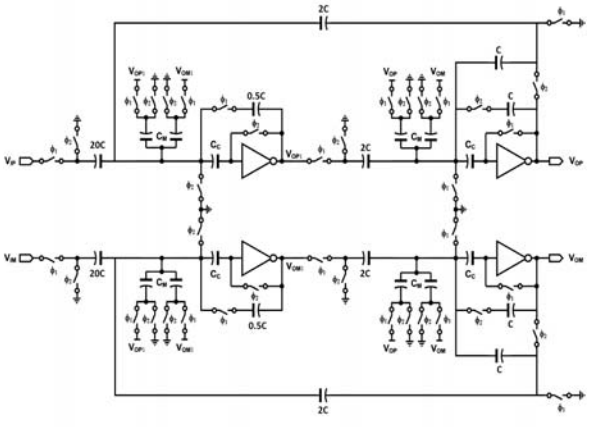


Fig. 8. Differential inverter-based SC low pass implementation.

D. Evaluation

For evaluation purpose the SC inverter-based integrator shown in fig. 3(a) is simulated using Cadence Spectre. The capacitor values are given in Table I. The inverter has a 0.7V power supply and its both NMOS and PMOS transistors have the W/L equal to $12/0.18\,\mu m$.

TABLE I. THE CAPACITOR VALUES USED IN SIMULATION.

Capacitor	C_S	C_I	C_L	C_C
Value (fF)	500	250	100	1000

The simulated integrator has a bandwidth of 1.5 KHz and the total integrated output noise of $3.64\times10^{-9}\,V^2$ which is nearly the same as the calculated value of $3.57\times10^{-9}V^2$ (assuming $gmRon \gg 1$).

IV. CIRCUIT DESIGN PROCEDURES

A. Switched Capacitor Low Pass Filter

In order to realize a low pass filter stage, a second-order biquad SC circuit was chosen. Figure 8 illustrates a fully differential SC low pass stage as a Chebyshev type-I filter which uses class-C inverters instead of OTA. The inverters' power supply and simulated DC-gain are 0.7 V and 32.9 dB, respectively, while their static current is only 77.3 nA. The switched capacitors have two non-overlapping clocks ϕ_1 and ϕ_2. The transfer function of this filter can be written as

$$H(s) = \frac{-80f_s^2}{s^2 + f_s s + 8f_s^2} \quad (19)$$

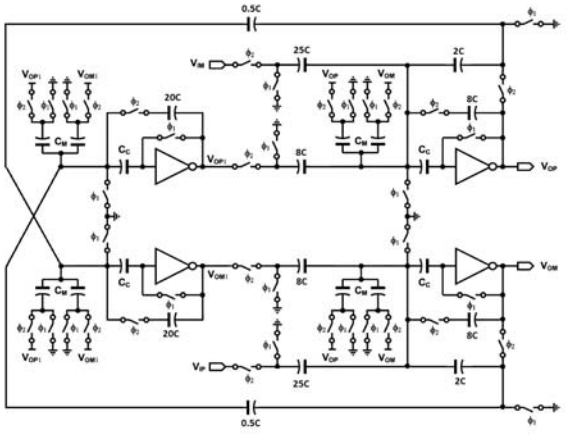


Fig. 9. Differential inverter-based SC band pass implementation.

where f_s is the sampling frequency. By applying different sampling frequencies, it is clear that the filter can be made tunable.

The low pass stage plays two different roles. When we are interested in LFP signals, it is a low pass filter with about 80Hz bandwidth and 1 KSamples/sec sampling frequency. However, when the system wants to record spikes, this stage works as a gain stage with bandwidth of about 8 KHz and 100 KSamples/sec sampling frequency.

B. Switched-Capacitor Band -Pass Filter

To allow spikes only and to prevent the low-frequency signals, a band-pass filter is applied for the second stage. Similar to the low-pass stage, the band pass stage is a fully differential second-order inverter-based biquad SC circuit, as shown in Fig. 9. The transfer function of this stage is given as follows

$$H(s) = \frac{-2.5 f_s s}{s^2 + \frac{1}{4} f_s s + \frac{1}{50} f_s^2} \tag{20}$$

where f_s is the sampling frequency. With 100 KSample/sec sampling frequency, the filter has about 4.5 KHz bandwidth whose the center frequency is 1.8 KHz.

By applying different sampling frequencies the cut-off frequencies can be made reconfigurable.

C. Half-Clock Delay

In order to cascade two stages, a half- delay clock stage is needed to break the continues loop and to reduce the loading effect of the stages. Thus a simple stage such as one introduced in [8] (shown in Fig. 10) is located between output and input lines of LPF and BPF stages.

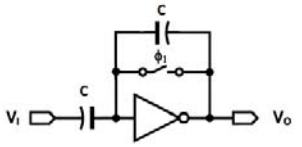


Fig. 10. A simple half-clock delay stage [8].

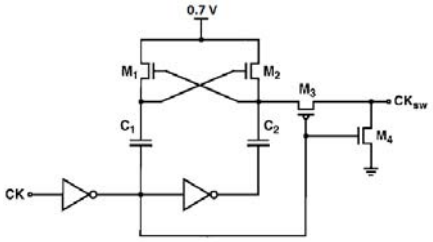


Fig. 11. Boosted clock driver [13].

D. Clock Bootstrapping

When the supply voltage is reduced the switch on- resistance increases, thus in order to have an adequately low switch resistance in low voltage era, the clock voltage should be bootstrapped beyond the supply voltage range. For this reason we use the clock boosted driver in [13] as illustrated in Fig. 11.

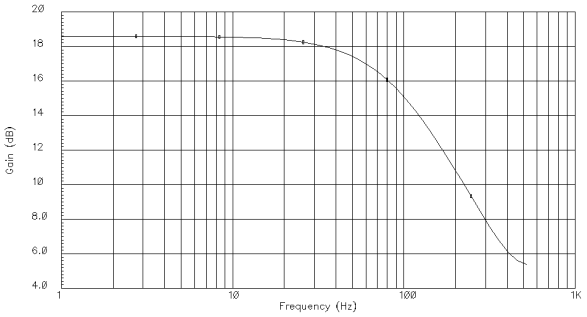
I. SIMULATION RESULTS

For evaluating the performance of the proposed circuits, simulations were performed in Cadence Spectre. The circuit was designed with 0.18-µm CMOS technology. With a 0.7 V supply voltage, the system consumes only 538 nW power (excluding clock generation) which is very suitable for neural recording application. A class-C inverter having 32.9 dB DC-gain and 77.3 nA static current is used in both stages.

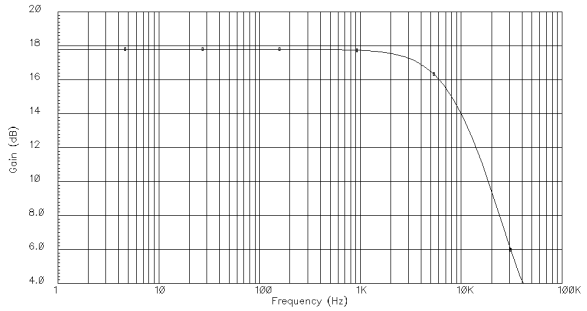
The transfer function of low pass stage for 1 KSamples/sec sampling frequency is illustrated in Fig. 12(a). The low pass cut-off frequency is 90 Hz with a DC gain of 18.6 dB which senses the LFP signals. Figure 12(b) shows the transfer function of the low pass stage for sampling frequency of 100 KSamples/sec. In this case this stage is only a gain stage for spike signals. It demonstrates 8.4 KHz cut-off frequency and 17.8 dB DC gain. Figure 13 illustrates the simulated cascaded stage, transfer function with 100 KSamples/sec sampling frequency. The pass band is in the range between 680 Hz and 5 KHz and the center frequency is located at 1.8 KHz with the pass band gain 28.2 dB.

Using PNOISE tool in Cadence Spectre, the total integrated input referred noise of the system, computed as 6.42 μV_{rms} with 8.4 KHz noise bandwidth. This can be translate as 70.1 $nV/\sqrt{Hz}$ input noise density with 8.4 KHz noise bandwidth.

Figure 14 shows the frequency response of the system for three different supply voltages. As shown, it is not very sensitive to the variation of the supply voltage showing that the design is robust and could be a good choice for neural recording systems.



(a)



(b)

Fig. 12. Low pass stage transfer function at (a) 1 KSamples/sec (b) 100 KSamples/sec

Table II summarizes the specification of some recently published neural amplifiers. The presented structure has quite good power consumption. But in comparison to other works, it has a good noise performance.

I. CONCLUSION

The large number of channels in multichannel microprobes and, the implantation of the system in the body, necessitate a low power design for neural recording applications.

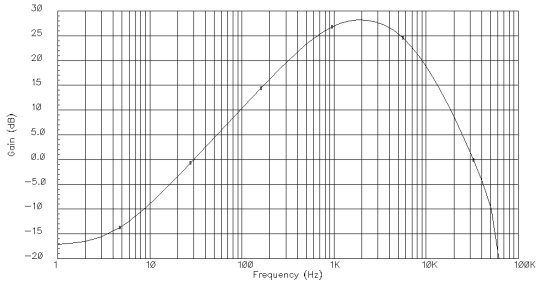


Fig. 13. Cascaded transfer function at 100 KSamples/sec.

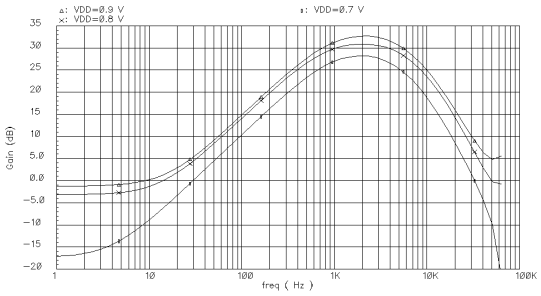


Fig. 14. Frequency response of cascaded filter by different supply voltages.

It has been shown that the OTA-less inverter-based technique greatly satisfies this requirement so that a sub-μW system which is composed of two stages has been designed. Using switched capacitor technique enables the adjustable cut-off frequency of the system by applying different sampling frequencies, so that both LFP and spike signals could be filtered and amplified. Also, a detailed analysis of noise performance for the inverter-based SC circuits has been presented. A mathematical model useful for analysis of such SC integrators has been derived and a good comparison between simulation and analytical technique has been obtained.

TABLE II. PERFORMANCE COMPARISON

Specification	[14]	[15]	[16]	[17]	[3]	**This work**[1]
Supply voltage (V)	1.8~3.3	1.8	3	1	1.6	**0.7**
Power/ch (μW)	2	225	15	3.77	69	**0.538**
Gain (dB)	41/50.5	59.5	48~68	45.7/49.3/53.7/60.5	19.1/37.5	**18.6/28.2**
High-pass corner (Hz)	0.05/0.4/2.5	10~100	0.01~70	0.23~217	100~660	**680**
Low-pass corner (Hz)	180	9.1k	500~5k	7.8k	80~8k	**90~8.4k**
Input referred noise (μV_{rms})	0.95	8	7	4.43	2.36	**6.42**
Input-noise density ($nV/\sqrt{Hz}$)	95	83.9	99	40.4	26.4	**70.1**
Technology (μm)	0.8	0.5	0.35	0.35	0.18	**0.18**

[1] Although this may not a fair comparison, this results are simulated results, whereas the others are measured ones.

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