A New Low-Voltage, Low-Power and High-Slew Rate CMOS Unity-Gain Buffer

M. Piry*, M. Khanjani moaf* and P. Amiri**

Abstract: Class-AB circuits, which are able to deal with currents several orders of magnitude larger than their quiescent current, are good candidates for low-power and high slew-rate analog design. This paper presents a novel topology of a class AB flipped voltage follower (FVF) that has better slew rate and the same power consumption as the conventional class-AB FVF buffer previously presented in literature. It is thus suitable for low-voltage and low-power stages requiring low bias currents. These buffers have been simulated using 0.5µm CMOS Technology models provided by IBM. The buffer consumes 20µA from a 0.9V supply and has a bandwidth of 50MHz with a 18pF load. It has a slew rate of 9.8V/µs and power consumption of 42µw.

Keywords: flipped voltage follower, class-AB circuits, level shifting techniques, high slew rate buffers, CMOS integrated circuits.

1 Introduction

Voltage follower which is here denoted VF, are widely used as output stages of operational amplifiers or in standalone configuration for signal conditioning, to accurately force an input voltage to a load with both high input and low output impedance [1]. The conventional implantation of a VF is the voltage follower shown in Fig. 1(a). It has an output impedance of $R_{out} = \frac{1}{g_m}$ (~2kΩ)[2] and positive slew rate $SR = \frac{I_{D_2}}{C_L}$ (Notation CL is the load capacitance, I_{D2} the drain current of transistor M2 and gm the small signal transconductance).

This VF is biased on the source side with a constant current source which ideally keeps a constant gate-to-source voltage in M1. This causes output voltage variations to follow the input voltage with a gate to source DC level shift. In practice this VF suffers from some problems like, not enough low output impedance, dependence of drain current of M1 on I_{out} and nonsymmetrical slew rate.

The FVF [3] shown in Fig. 1(b) is an improvement to a conventional VF. The FVF has a constant current through transistor M1, independent on the output current. Because of the shunt feedback, the output impedance is decreased to:

$$R_{out} = \frac{1}{\frac{1}{r_{o_2}} + g_{m_2}(1 + r_{o_1} g_{m_1})} \simeq \frac{1}{g_m^2 r_o} \quad (1)$$

It is much smaller than R_{out} of conventional VF. The voltage gain is almost unity:

$$\frac{V_o}{V_i} = \frac{r_{o_1} r_{o_2} g_{m_1} g_{m_2}}{r_{o_1} r_{o_2} g_{m_1} g_{m_2} + r_{o_2} g_{m_2} + 1} \quad (2)$$

This is bigger than the voltage gain of conventional VF. The circuit in Fig. 1(b) is able to source a large current but its sinking capability is limited by the drain current of M3.

To overcome this problem, circuit in Fig. 1(c) [4], [5], [6] is used. Under quiescent conditions, every transistor is in saturation and no current is delivered to the load. Neglecting second order effects, transistor M4 copies the drain current of transistor M1. Therefore the total current taken from supply voltage is $2I_b$ ($=2I_{D3}$) which increases the power consumption of the circuit.

In this paper a very simple, low-voltage class-AB structure is proposed which is able to take current from supply sources only when the load requires it, so the power consumption decreases, and the slew rate increases.

Iranian Journal of Electrical & Electronic Engineering, 2013.
Paper first received DD MMM YYYY and in revised form DD MMM YYYY.
* The Authors is with the Department of Electrical Engineering, Shahid Rajaee Teacher Training University, Tehran, Iran.
E-mail: Piry.milad@yahoo.com, m_khanjani69@yahoo.com.
** The Author are with the Department of Electrical Engineering, Shahid Rajaee Teacher Training University, Tehran, Iran.
E-mails: pamiri@srttu.edu.
Corresponding Author: P. Amiri.

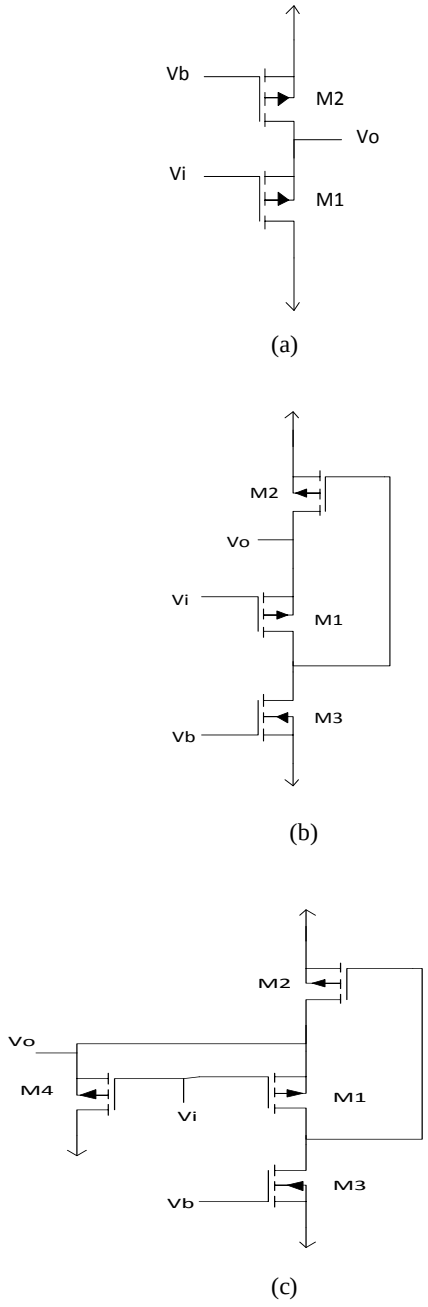


Fig. 1 Unity-Gain buffers: (a) Conventional VF. (b) FVF [3]. (c) Class-AB [4].

The proposed structure has been simulated using the models of the IBM CMOS 0.5µm technology, in order to compare its performance with the other buffers in terms of settling time, bandwidth, output impedance, power consumption and total harmonic distortion.

2 A New Class-AB Unity Gain Buffer

The new unity-gain buffer in Fig. 2 is able to source and sink a maximum current which is higher than its quiescent current providing class-AB operation, as it will be shown next.

When the input signal Vi increases, with respect to the output voltage Vo, the source-to-gate voltage of transistor M1 tends to decrease. As transistor M1 is biased by the current source M3, its drain-to-source voltage increases, forcing a large current through transistor M2, and leading the transistor M4 into the cut-off region. In this operation regime the output current is $I_{D_2} - I_{D_3}$, and the output impedance is given by:

$$R_{out} = \frac{1}{\frac{1}{r_{o_2}} + g_{m_2}(1 + r_{o_1} g_{m_1})} \tag{3}$$

When the input signal decreases, the source-to-gate voltage of transistor M1 tends to increase and this transistor tends to the ohmic region. As the current through transistor M1 is fixed, its source-to-drain voltage decreases, leading the transistor M2 into the cut-off region and transistor M4 into the saturation region. In this operation regime the current which is sinking equals to $I_{D_3} + I_{D_4}$, and the output impedance is approximately given by:

$$R_{out} = \frac{1}{\frac{1}{r_{o_4}} + g_{m_4}(1 + r_{o_1} g_{m_1})} \tag{4}$$

Thus transistor M4 sinks current only when the input signal is small, so the current taken from the supply voltage in quiescent conditions is decreased.

In quiescent conditions, the gate-to-source voltage of transistor M4 is given by:

$$V_{GS_4} = V_{DD} - V_{SG_2} - V_{SS} = V_{DD} - \sqrt{\frac{I_{D_2}}{k_2}} - |V_{th_P}| - V_{SS} \tag{5}$$

In Eq. (5) notation k_2 is $\frac{1}{2}\frac{\mu_P C_{OX} W}{L}$. To keep the drain current of transistor M4 near zero, its gate-to-source voltage should be near the threshold voltage of transistor M4. Thus the Eq. (5) is given by:

$$V_{DD} - V_{SS} = V_{th_N} + \sqrt{\frac{I_{D_2}}{k_2}} + |V_{th_P}| \tag{6}$$

To decrease the required supply voltage, a DC level shifter shown in Fig. 3(a) is used. In this circuit the Eq. (6) is given by:

$$V_{DD} - V_{SS} = V_{th_N} + \sqrt{\frac{I_{D_2}}{k_2}} + |V_{th_P}| - V_L \tag{7}$$

One basic implementation of this DC level shifter is shown in Fig. 3(b), in which VL is the source-to-gate voltage of transistor M5. The minimum voltage required to keep M1 in saturation is given by:

$$V_i \geq V_{G_2} - |V_{th_p}| \tag{8}$$

Also the condition of saturation for transistor M4 is given by:

$$V_i \geq V_{G_2} + V_L - V_{SG_1} - V_{th_N} \tag{9}$$

From Eq. (8) and (9), we conclude that decreasing the input signal leads the transistor M1 into the ohmic region before the transistor M4.

If the input signal is a square wave, in the falling edge, the gate voltage of transistor M2 increases, this voltage is shifted to a higher value by transistor M5 and leads transistor M6 into the cut-off region. Fig. 4(a) shows the variations of gate voltages of transistors M2 and M4. In Fig. 4(a) a limitation can be observed as the gate voltage of transistor M4 cannot exactly follow the variations of gate voltage of transistor M2. Thus the maximum drain current of transistor M4 is limited, so the negative slew rate decreases.

A better technique for implementation of this floating voltage source is discussed in [7], shown in Fig.3(c). In quiescent conditions, the gate voltage of transistor M4 is equal to V_C and the voltage across capacitor C is equal to $V_C - V_{G_2} = V_L$. Since the capacitor C and the resistor R form a high pass circuit with a corner frequency $f_{3dB_{LOW}} = \frac{1}{2\pi RC}$, in order to set the lower 3dB frequency of the amplifier as low as possible, R should have extremely large values. For typical values of integrated capacitors (in the pF range) to set $f_{3dB_{LOW}} < 100Hz$, R should be larger than 1GΩ. Such a large resistor would have large area and parasitic capacitance that would limit the bandwidth of the amplifier. Efficient implementation of such a large resistor is discussed in [8], shown in Fig. 3(d). In this circuit, under dynamic conditions, only one of the transistors M5 and M6 are on, and the other is off. So the effective resistance of the series combination of these transistors is very large. Under quiescent conditions the control voltages V_{b2} and V_{b3} keep M5 and M6 in subthreshold region with a very large effective resistance.

In the circuit of Fig. 3(d), the gate voltage variations of transistor M4 follow the gate voltage variations of transistors M2 exactly, as can be observed in Fig. 4(b). Thus the limitation mentioned before is eliminated, and the negative slew rate improves.

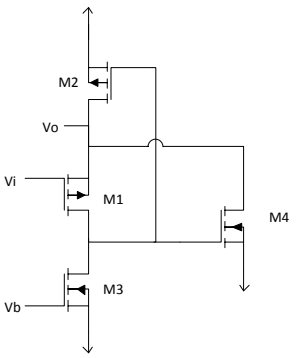


Fig. 2 basic implementation of Proposed circuit.

If we use the circuit in Fig. 3(d) and its P-channel structure like the configuration shown in Fig. 5, although the power consumption increases, the slew rate improves, because the right circuit has the capability of sourcing large currents and the left one has the capability of sinking large currents, also transistors M4 and M10 improve the capability of sinking and sourcing current of right and left circuits respectively.

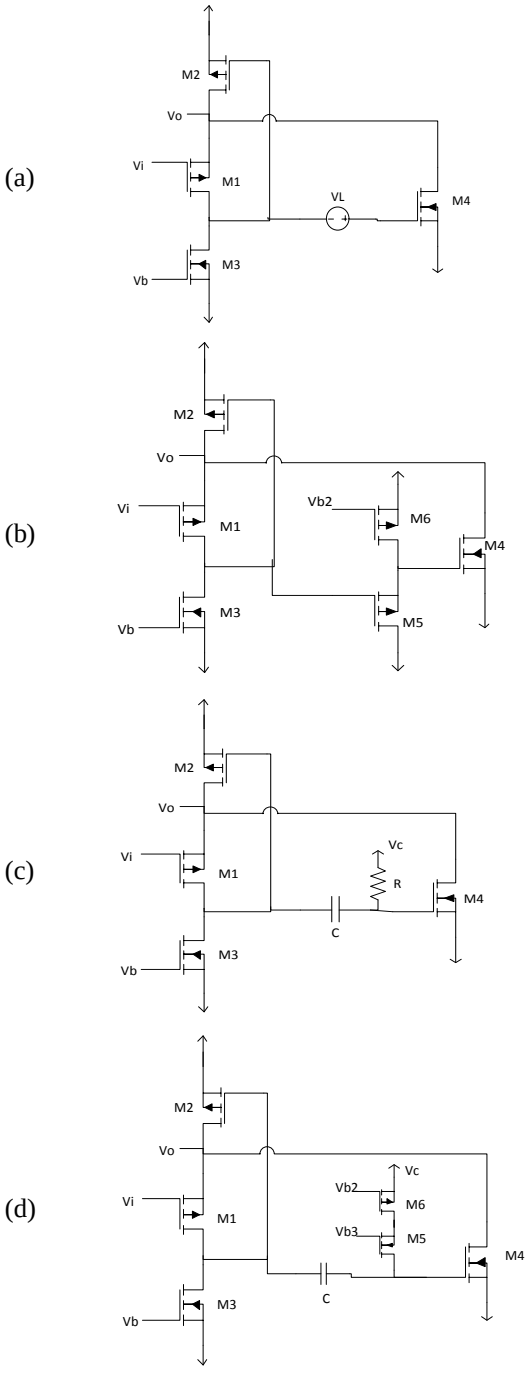
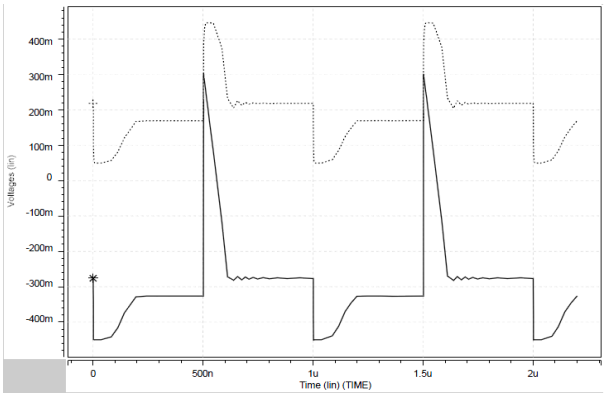
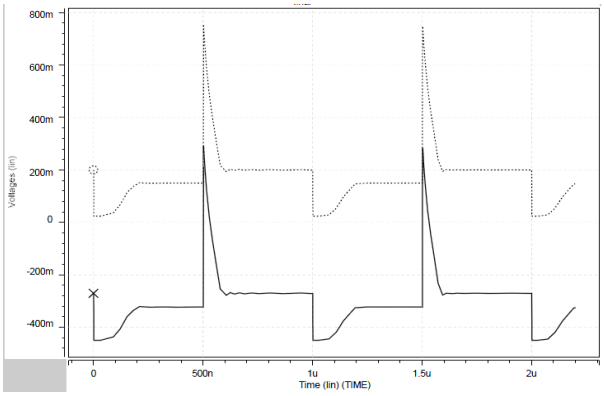


Fig. 3 Proposed circuit: (a) improved by level shifter. (b) DC level shifter implemented by transistor. (c) DC level shifter based on [7]. (d) large resistor implemented by transistor based on [8].



(a)



(b)

Fig. 4 gate voltage variations of transistors M2 (continuous line) and M4 (dotted line): (a) circuit 3(b). (b) circuit 3(d).

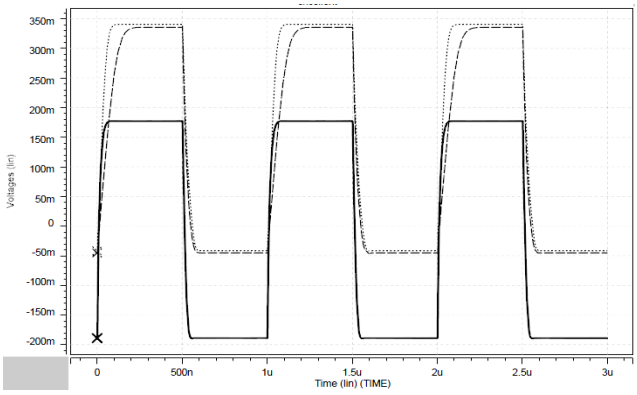


Fig. 6 step response of three buffers Fig. 5 (continuous line), Fig. 3(d) (dash line) and Fig. 1(c) (dotted line).

Table 1 Sizes of transistors.

MOS Width (µm)	Fig. 5	Fig. 3(d)	Fig. 1(c)
0.6	M5,M6,M11,M12	M5,M6	-
4	M3	M3	M3
6	M4	M4	-
8	M2	M2	-
13.88	M1,M9	M1	M1
15	M8	-	-
3.8	M7	-	-
17	-	-	M2
13	-	-	M4
70	M10	-	-

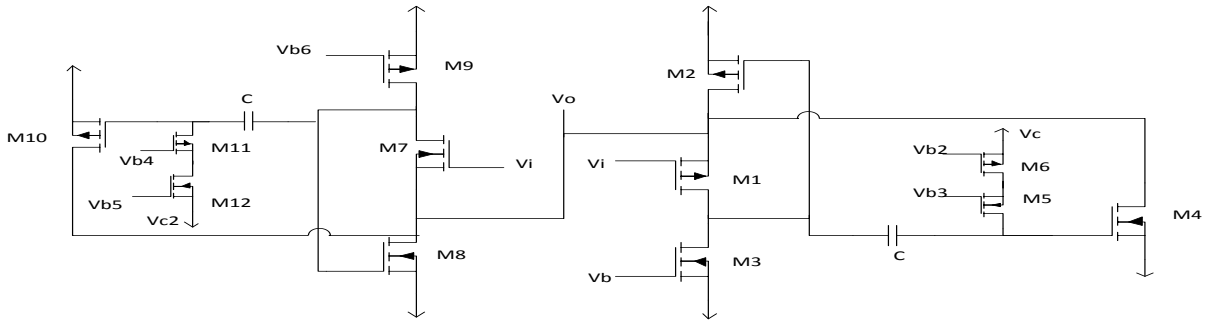


Fig. 5 improved voltage buffer

3 Simulation Results

The structures of proposed buffers (Fig. 3(d) and Fig. 5) and class-AB FVF [3] (Fig. 1(c)) were simulated for comparison with V_{DD}=0.45V, V_{SS}=-0.45V and C_L=18pF. For simulations 0.5µm CMOS technology parameters were used that have nominal NMOS and PMOS threshold voltages $V_{th_N} = 0.67V$ and $|V_{th_P}| = 0.5V$ respectively. The biasing current source is equal to 20µA. All the devices used have 0.6µm length. The sizes of transistors are reported in Tabale 1.

Fig. 6 shows the step response of the three buffers. The input step signals of the buffers have 400mVPP swing and frequency of 1MHz. This figure shows the negative slew rate of 9.76 V/µs for the circuit of Fig. 5, 6.09 V/µs for the circuit of Fig. 3(d) and 6.1 V/µs for the circuit of Fig. 1(c).

That it agrees with the expected negative slew rate. Also the positive slew rate is 9.76, 2.53, 6.1 V/µs respectively**.**

Fig. 7 shows the frequency response comparison of all FVFs. They are characterized by similar 3dB frequencies. It can be observed that the circuits have bandwidth of 49.9, 20.4 and 53.7 MHz respectively.

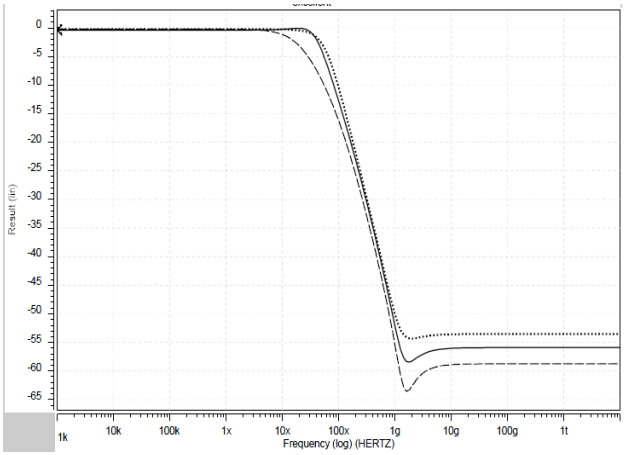


Fig. 7 Frequency response comparison Fig. 5 (continuous line), Fig. 3(d) (dash line) and Fig. 1(c) (dotted line).

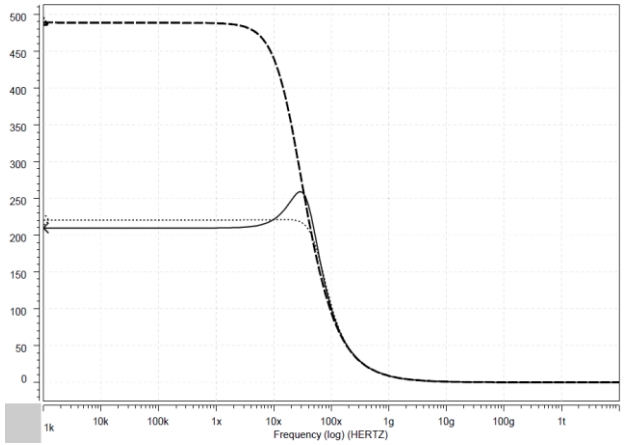


Fig. 8 Output impedance comparison Fig. 5 (continuous line), Fig. 3(d) (dash line), Fig. 1(c) (dotted line).

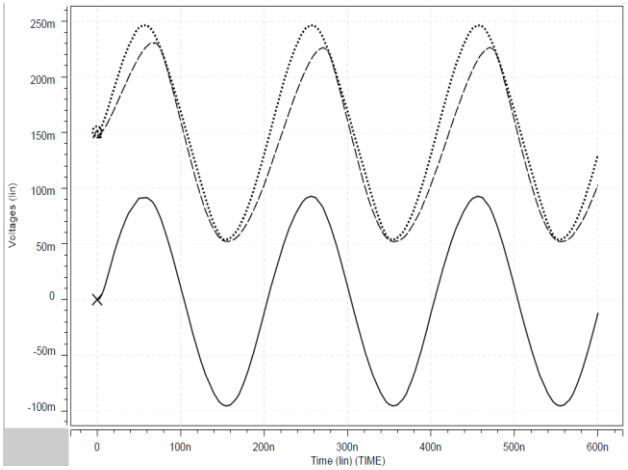


Fig. 9 Output of the buffers with 0.2V_{PP} 1MHz input Fig. 5 (continuous line), Fig. 3(d) (dotted line) and Fig. 1(c) (dash line).

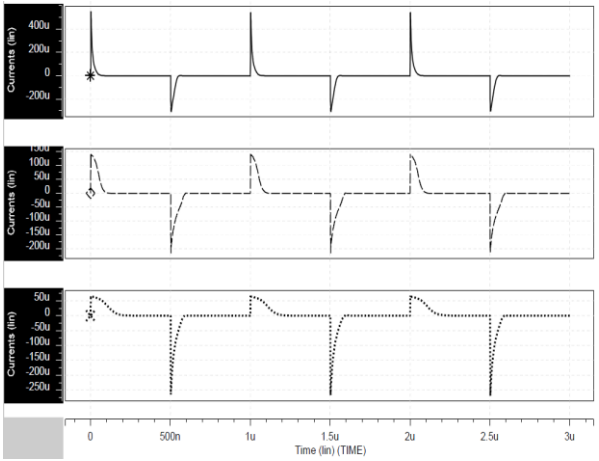


Fig. 10 Simulated output current Fig. 5 (continuous line), Fig. 3(d) (dotted line) and Fig. 1(c) (dash line).

Fig. 8 shows a comparison of the (magnitude) of the output impedance obtained by applying a 1A AC current source to the buffer's output terminals with the input grounded. The voltage in this case corresponds directly to the output impedance. It can be seen that the circuits have output impedance of 210, 489, 220 Ω respectively.

Fig. 9 shows the measured response for a 5MHz, 200mv peak-to-peak sinusoidal input voltage. The measured THD for a 1MHz, 200mv peak-to-peak sinusoidal input signal was -45.6, -41.4, -54.9 dB respectively.

In Fig. 10 the simulated output current for a 1MHz, 200mv square input signal is presented. The represented current is the one going through the load capacitor. It can be seen that the maximum current drained from load capacitor is 309, 266 and 216 µA and the maximum current sourced to the load capacitor is 553, 57.8 and 139 µA. It can be seen why the slew rate in the circuit of Fig. 5 is improved.

4 Comparison with buffers

Table 2 presents a comparison of three buffers in terms of bandwidth, static power consumption, positive and negative slew rate, output impedance, voltage gain, THD, HD_2 and HD_3.

It can be seen that, although the power consumption in circuit of Fig. 5 is a little larger than circuit of Fig. 1(c), the slew rate is highly improved. If we use two circuit of Fig. 1(c) in circuit of Fig. 5 structure, although the slew rate enhances, the power consumption is 72µw, which is 30µw larger than power consumption of circuit Fig. 5. Circuit of Fig. 5 suffers from low gain and distortion in comparison to circuit of Fig. 1(c).

Circuit Fig. 3(d) suffers from low positive slew rate, small bandwidth and high output impedance, while it has low power consumption and high negative slew rate.

Table 2 Comparison with buffers

Circuit	P	BW	SR^+	SR^-	R_{out}	Gain	THD	HD_2	HD_3
Fig. 5 Second proposed circuit	42µw	50MHz	9.8V/µs	9.8V/µs	210Ω	-0.4dB	-46dB	47dB	52dB
Fig. 3 (d) First proposed circuit	21µw	20MHz	2.5V/µs	6.1V/µs	489Ω	-0.3dB	-41dB	44dB	51dB
Fig. 1 (c) Conventional circuit	36µw	54MHz	6.1V/µs	6.1V/µs	220	-0.2dB	-55dB	56dB	62dB

5 Conclusion

A new class-AB unity-gain buffer based on the Fipped Voltage Follower (FVF) has been proposed. This circuit can be operated at a low voltage and low power. With respect to other class-AB stages based on the FVF topology, it has superior slew rate with low power consumption. This novel buffer has also low output impedance. The characteristics of the proposed circuit were validated by simulations.

References

[1] Centrurelli F., Monsurro P. and Trifiletti A., "A Class-AB Flipped Voltage Follower Output Stage", IEEE 2011, 20th European Conference on Circuit Theory and Dedsing (ECCTD), 2011.

[2] Razavi B., Design of Analog CMOS Integrated Circuits. New York:McGraw-Hill, 2001.

[3] Carvajal R.G., Ramirez-Angulo J., Lopez-Martin A., Torralba A., Galhn J., Carlosena A. and Mufioz F., "The Flipped Voltage Follower: A useful cell for low-voltage low-power circuit design", *IEEE Transactions on Circuits and Systems I*, vol. 52, no.7, pp. 1276-1291, July 2005.

[4] Ramirez-Angulo J., Gupta S. and Carvajal R.G., "New Improved CMOS Class-AB Buffers Based on Differential Filipped Voltage Followers", Circuits and Systems, 2006. ISCAS 2006. Proceedings. *2006 IEEE International Symposium on, 2006.*

[5] Ramirez-Angulo J., Gupta S. and Carvajal R.G., Torralba A., Jimenez M. and Munoz F., "Comparison of Conventional and New Flipped Voltage Structures With Increased Input/output Signal Swing and Current Sourcing/Sinking Capabilities", Circuits and Systems, 2006. ISCAS 2006. Proceedings. *2006 IEEE International Symposium on, 2006.*

[6] Jimenez M., Torralba A., Carvajal R.G., Ramirez-Angulo J., "A new low-voltage CMOS unity-gain buffer", Circuits and Systems, 2006. ISCAS 2006. Proceedings. *2006 IEEE International Symposium on, 2006.*

[7] Ramirez-Angulo J., Sawant M.S., Carvajal R.G., Lopez-Martin A.J., "cascode mirrors and telescopic op-amps", Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006. *IEEE International Symposium on 2006.*

[8] Bikumandla M., Ramirez-Angulo J., Urquidi C., Carvajal R.G. and Lopez-Martin A.J., "Biasing CMOS amplifiers using MOS transistors in subthreshold region", IEICE Electronics Express, vol.1, no.12, pp. 339-345, September 25, 2004.

Milad Piry was born in 1990 in Tehran. He received the electrical enginnering in 2013 from Shahid Rajaee Teacher Training University (SRTTU Tehran, Iran). His research interest is to design Analog integrated circuit, especially the design of operational amplifier**s.**

Mona Khanjani moaf was born in 1991 in Bandar-e Anzali. She received the electrical enginnering in 2013 from Shahid Rajaee Teacher Training University (SRTTU Tehran, Iran). Her research interest is to design Analog integrated circuit, especially the design of low-voltage and low-power circuits.

Parviz Amiri was born in 1970, received B.S degree from University of Mazandaran in 1994, M.S from Khajeh Nasir Toosi University (KNTU Tehran, Iran) in 1997, and his Ph.D. from University of Tarbiat Modares (TMU Tehran, Iran) (2010), all degrees in electrial engineering (electronic). His main research internest include electronic circuit design in industries. His primary research interest is RF and power circuit design. He is currently with the department of electrical engineering Shahid Rajaee Teacher Trainning University in Tehran, Iran**.**