Modeling and Simulation of Substrate Noise in Mixed-Signal Circuits Applied to a Special VCO

Golnar Khodabandehloo*, Sattar Mirzakuchaki** and Gholamreza Karimi***

Abstract: The mixed-signal circuits with both analog and digital blocks on a single chip have wide applications in communication and RF circuits. Integrating these two blocks can cause serious problems especially in applications requiring fast digital circuits and high performance analog blocks. Fast switching in digital blocks generates a noise which can be introduced to analog circuits by the common substrate. This noise can decrease the performance of mixed-signal circuits; therefore, studying this noise and the way it is transmitted will lead to solutions for reducing it and improving mixed-signal circuit's performance. In this paper, an efficient model for substrate is extracted from Green's function in MATLAB environment, and its accuracy is demonstrated. Using a VCO and a multiplier as analog and digital blocks, respectively and simulating them along with the proposed model of the substrate, the effects of substrate noise coupled to analog blocks are shown. Finally, some methods for reducing this noise are applied to the circuit, and the results are compared to each other. The results indicate that using P+ Guard Rings is the best method for reducing substrate noise in the mixed-signal circuits.

Keywords: Mixes-Signal Circuits, Coupling, Substrate Noise, Green's Function, VCO, Phase Noise.

1 Introduction

Nowadays, VLSI technology makes it possible to have mixed-signal circuits on a single silicon die where fast digital circuits are integrated with high performance analog blocks. Noise isolation is one of the most important problems in these circuits and becomes worse as noise increases due to higher integration density and faster digital circuits [1].

Noise coupling problems are a crippling factor in many advanced circuits. Therefore, studying this effect is inevitable in order to find solutions for reducing it.

The aim of this work is to simulate and analyze the noise transmitted through the common substrate in a mixed-signal circuit. For this purpose, first a VCO is designed to act as the analog block and then a multiplier is chosen as the high frequency digital block. The most important part of this work is modeling the substrate. Substrate should be modeled in a way that it can be used in simulators like SPICE.

After designing analog and digital blocks, substrate model can be used to illustrate the path between them. Thus, switching noise in digital circuits transfers to analog circuits through the substrate. By comparing analog block characteristics after and before relating it to digital block, noise effects can be specified. Thus, substrate noise in real mixed-signal circuits is simulated. Some methods of reducing substrate noise are applied to the designed circuit and compared to each other.

In section 2, substrate noise and some injection and reception mechanisms are described. Some methods for modeling substrate and the one used in this paper are outlined in section 3. Section 4 discusses analog and digital blocks designed here. Analog and digital blocks are related by the substrate model in section 5, and some simulations are performed. In section 6 some substrate noise reduction methods are applied and the results are compared.

2 Substrate coupled noise

A silicon substrate is generally considered to provide a good isolation between devices because of its high resistance. However, in some cases, switching devices can introduce some turbulence to the substrate which

Iranian Journal of Electrical & Electronic Engineering, 2006.
Paper first received 2nd January 2005 and in revised form 7th April 2007.
* Golnar Khodabandehloo is with the Department of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran. E-mail: kh_golnar@yahoo.com.
** Sattar Mirzakuchaki is with the Department of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran. E-mail: m_kuchaki@iust.ac.ir.
*** Gholamreza Karimi is with the Department of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran. E-mail: gh_karimi@iust.ac.ir.

can be transferred to other devices because of substrate finite resistance.
Figure 1 shows two common substrates: lightly doped or P- and heavily doped or P+ [2].
Each switching node can introduce some noise to the substrate. Finite resistance of substrate means that this noise can be transferred to adjacent devices. There are several injection and reception mechanisms, some of which are shown in Fig. 2.

2.1 Noise injection mechanisms

The most important noise injection mechanism is coupling of PN junctions between devices and substrate or wells (Fig. 3) [3]. Another mechanism is the injection through digital supply lines [1].

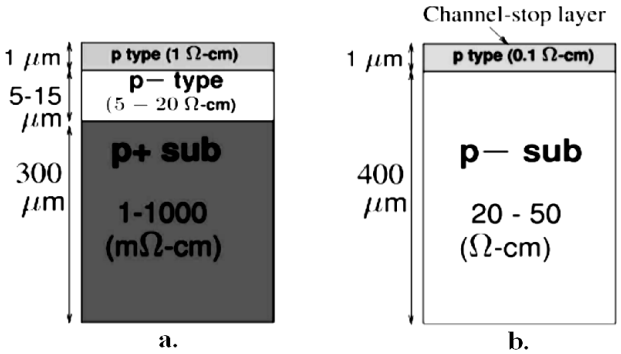


Fig. 1 Common substrates for VLSI circuits: a) heavily doped substrate b) lightly doped substrate.

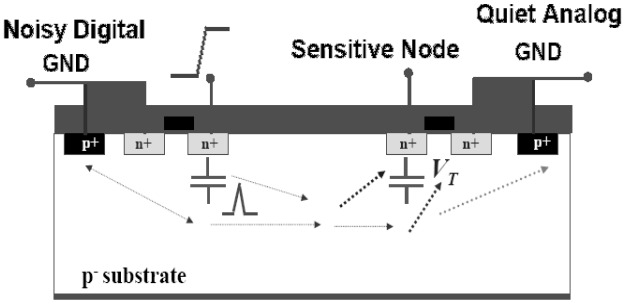


Fig. 2 The most important noise injection and reception mechanisms.

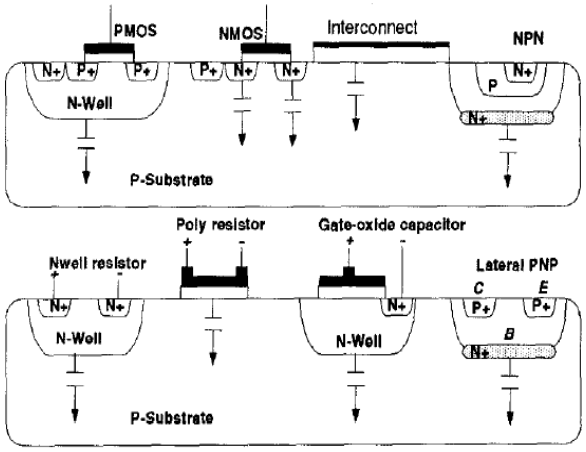


Fig. 3 Noise injection to substrate by PN junctions [3].

2.2 Noise reception mechanisms

Junction capacitors can also cause noise reception due to voltage difference between substrate and the sensitive node, mostly drain. Furthermore, threshold voltage depends on the source-body voltage, V_{bs}, so that variations on the $V_{bs,}$ caused by the noise will cause variations in the threshold voltage. Another mechanism is through analog supply lines [1].

3 Substrate modeling

Several methods are used for substrate modeling such as approximate methods [2-7], numerical methods like Finite Element Method (FEM) [1, 8], and Boundary Element Method (BEM) based on Green's Function. In this section the process of substrate modeling using Green's Function is discussed.

3.1 Green's Function

As the resistance varies with different doping values, the substrate with several levels of doping can be modeled as a stack of parallel homogeneous layers [9]. Figure 4 shows that substrate can be considered as a dielectric consisting of several layers with different dielectric constant ε_k, where k is the number of layers [10].
In most cases, the substrate can be treated as a two layer medium: an epitaxial layer and a substrate. Contacts are placed at the top of this medium. This configuration is shown in Fig. 5. Ground contacts, if desired, can be placed at the bottom of the medium.

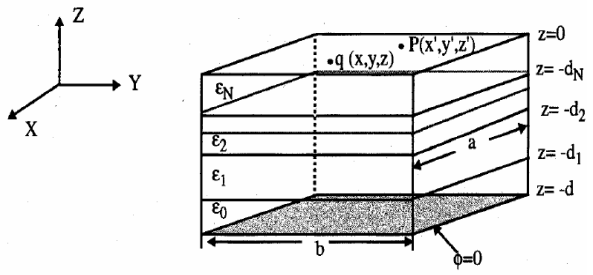


Fig. 4 A cross-section of substrate [10].

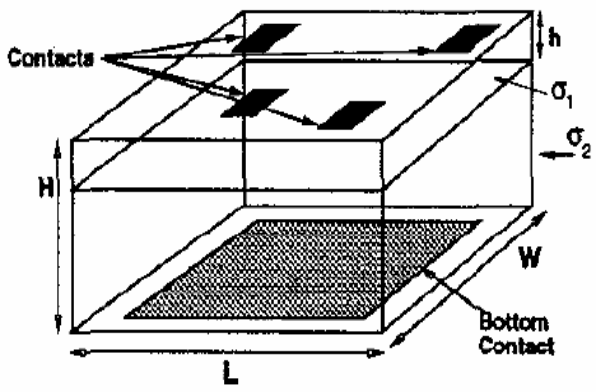


Fig. 5 A three-dimensional schematic of an epitaxial layer and contacts [9].

When the substrate has only resistive effect, Laplace's equation yields the following:

$$\nabla^2\phi = 0 \tag{1}$$

where ϕ is the Electrostatic Potential. Using the Green theorem in (1), ϕ at an observation point, r, due to a unit current injected in source point, r', will be

$$\phi(r) = \int_S J(r')G(r,r')da \tag{2}$$

where $G(r,r')$ is the Green's Function of the substrate which can fit in the substrate boundary conditions, and $J(r')$ is the source current density. Observation and source points are on the defined contacts of substrate which are planar and two dimensional; thus, the integral is on the surface [11].

There are some methods for solving the Green's Function [10, 11]. One of them is the Method of Images. Obtaining the Green's Function, equation (2) will be solved. With discretizing each port on the substrate to small panels, a system of equations is produced which imply the relation between current and potential of each panel (current distribution in each panel is considered constant). This can be shown in matrix form as

$$\phi = Zi \tag{3}$$

where each z_{ij} is computed from

$$z_{ij} = \frac{1}{S_i S_j}\int_{S_i}\int_{S_j} G(r,r')da'da \tag{4}$$

where S_i and S_j are the surface areas of panels i and j, respectively. By inverting the impedance matrix, Z, the admittance matrix is obtained. Substrate resistance between each two ports is the sum of corresponding matrix entries [11].

3.2 Method of Images

Method of images is a simple technique for demonstrating the Green's Function. In this method, point charges are distributed in the space in order to match the desired boundary conditions. Method of images can be used for dielectrics, too. In Fig. 6 essential image charges for representing the potential of a charge Q inside a medium with dielectric constant ε_2 and in the presence of a ground-plane are shown. One limitation of the proposed method is the assumption of infinite substrate structure (infinite x and y directions). However, this does not affect the adaptability of this approach. In fact, the rough guidelines reported in [2] suggest that the sidewall effect can be neglected if the contact is kept away from the edges of the chip at least a distance of twice the epi-layer thickness. Potential at any point on the medium is obtained as

$$\Phi(r) = \frac{1}{4\pi\varepsilon_2}\sum_{n=1}^{\infty}\frac{q_n}{|r - r_n'|} \tag{5}$$

where r_n' is the location of the nth image charge [12].

For the substrate shown in Fig. 7 which has two media with different permitivities of ε_1 and ε_2 and a ground-plane, the Green's Function is obtained as [13]

$$\begin{aligned} G(x',y',x,y) = \frac{1}{4\pi\varepsilon_1}\Bigg[& \frac{1+\eta}{\sqrt{(x'-x)^2+(y'-y)^2}} \\ & + \frac{\eta^2-1}{\eta}\Bigg[\frac{1}{2h}\ln\left(\frac{1}{1-\eta}\right) + \\ & \sum_{n=1}^{N}\Bigg[\frac{\eta^n}{\sqrt{(x'-x)^2+(y'-y)^2+(2h)^2n^2}} \\ & - \frac{\eta^n}{2hn}\Bigg]\Bigg]\Bigg] \end{aligned} \tag{6}$$

where h is the substrate height, (x,y) is the observation point, (x',y') is the source point, N is 5 or 10 for lightly doped and heavily doped substrates, respectively and η is defined as

$$\eta = \frac{\varepsilon_1 - \varepsilon_2}{\varepsilon_1 + \varepsilon_2} \tag{7}$$

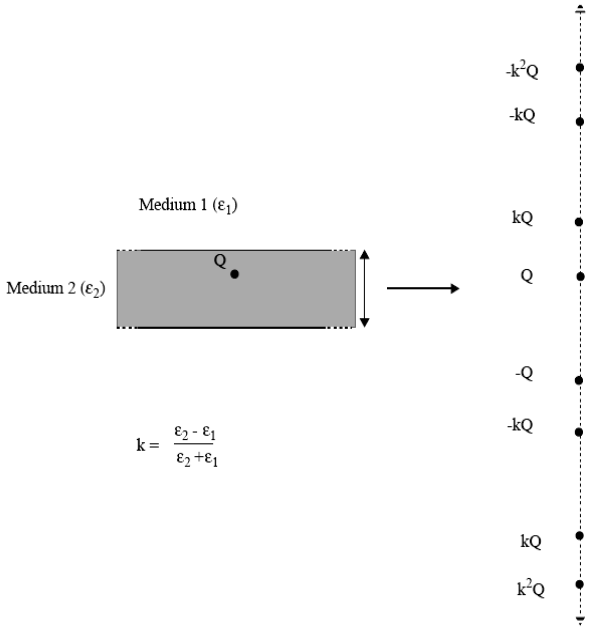


Fig. 6 Method of images in two-layer dielectric [12].

3.3 Obtaining numerical values

Considered frequency in this paper is about 2 GHz. At this frequency, substrate has only resistive effects. Also, Green's Function is determined by method of images and the integrals are solved using numerical methods [14]. All the calculations are accomplished by MATALB. The obtained values have been compared to values presented in other papers for evaluating their accuracy.

Considering substrate as a dielectric and a uniform charge distribution on contact i, the mean potential induced to contact j is obtained as

$$\phi_{ji} = p_{ji} q_i = \frac{q_i}{S_i S_j} \int_{S_i} \int_{S_j} G(x', y', x, y) ds_j ds_i \quad (8)$$

This can be rewritten in matrix form as

$$\Phi = PQ \quad (9)$$

It means that $Q=P^{-1}\phi$ or $Q=C\phi$. Matrix C is referred to as capacitance-coefficient matrix. Inverting matrix Z, C is obtained. From circuit theorem it is shown that

$$C_{ij} = -c_{ij}, \quad C_{ii} = c_{ii} + \sum_{k=1}^{M} c_{ik}, k \neq i \quad (10)$$

Under the quasi-static approximation, the conductance G and the capacitance C between any two contacts are in the same proportion [15] as

$$G^{-1}C = \rho\varepsilon \quad (11)$$

Consequently, the resistance values will be obtained by calculating and inverting G_{ii}.

3.4 Results

As discussed above, a program is written in MATLAB. Replacing variable data for substrate and contacts with those of [14] and comparing the results, the accuracy of the program is proven. Comparison is done for three different situations. First, when there is only one contact on the substrate (substrate height, 100 μm and contact's dimension, 100 μm × 100 μm). Table 1 compares the results. In the second situation, two contacts are placed on the substrate (substrate height, 400 μm and contacts' dimension, 10 μm × 10 μm). Figures 8 and 9 compare the value of C for different distances between contacts. Third, when there are four contacts on the substrate (substrate height, 100 μm, contacts' dimension, 20 μm × 20 μm, and distance between contacts, 100 μm center to center). Table 2 compares the results.

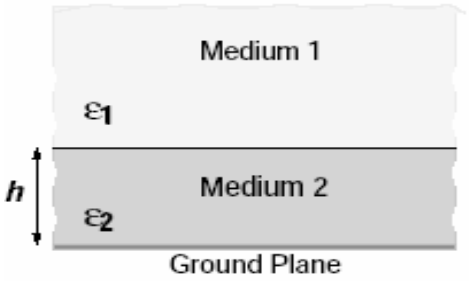


Fig. 7 Two mediums with different permitivities and a ground-plane.

Table 1 Comparison of resistant values in [14] and program written in MATLAB for one contact.

Resistance implied in [14]	342.8 Ω
Resistance achieved in MATLAB	344.1 Ω

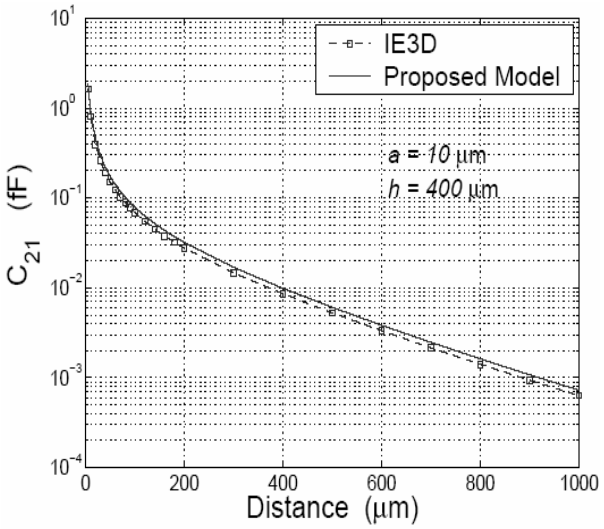


Fig. 8 C values for different distances between contacts in [14].

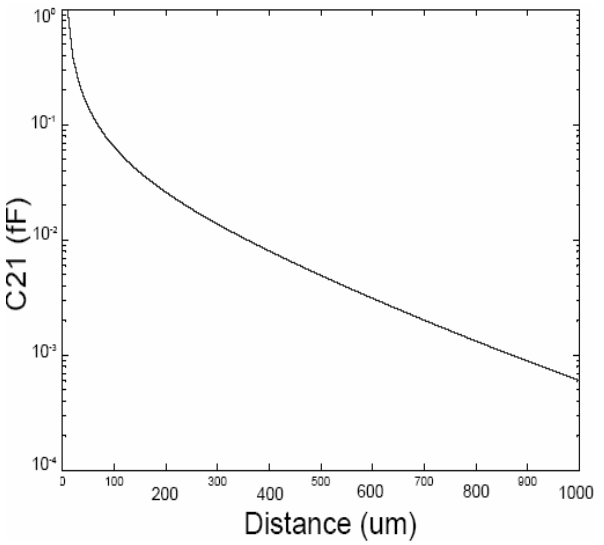


Fig. 9 C values for different distances between contacts in MATLAB.

Table 2 Comparison of resistant values in [14] and program written in MATLAB for four contacts.

	R1,1	R1,2	R1,3	R1,4	R2,3	R2,4	R3,4
Resistances implied in [14] (kΩ)	2.10	70.07	523.39	2,713.02	70.35	523.91	70.07
Resistances achieved in MATLAB (kΩ)	2.13	74.33	550.57	2,581.4	74.62	550.57	74.33

As is shown in Tables 1 and 2 and Figs. 8 and 9, the values achieved in MATLAB are approximately equal to those implied in [14], and in the worst case the difference is about 6%. Consequently, the program written in MATLAB can be properly used for extracting resistant values needed in modeling the substrate in this work.

4 Analog and digital blocks

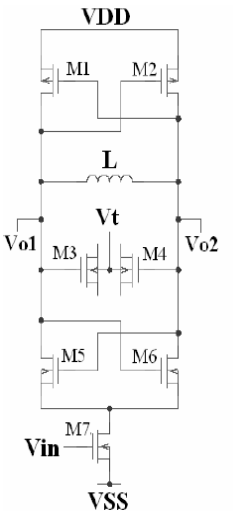
Mixed-signal circuits have both analog and digital parts. As VCO is one of the most common analog circuits used in mixed-signal and communication circuits, it is chosen as the analog block in this paper. On the other hand, a high frequency digital circuit is needed, so multiplier is an appropriate selection.

4.1 VCO

A cross-coupled VCO [16] is designed in this paper and its SPICE model is shown in Fig. 10. This VCO is designed so that it can oscillate at a frequency of 2 GHz; its component values are shown in Fig. 10. Figure 11 shows the VCO output simulated with HSPICE.

4.2 Multiplier

A 2×2 bit parallel multiplier is designed for this paper. 2-bit full adders are used in this design. The multiplier layout which has 132 transistors in 0.35 micron technology is shown in Fig. 12. This multiplier has acceptable outputs at a frequency of 2 GHz.



M1,M2(W/L) (μm/μm)	800/.35
M3,M4(W/L) (μm/μm)	1600/.35
M5,M6(W/L) (μm/μm)	300/.35
M7(W/L) (μm/μm)	2000/1.05
L(nH)	2
Vin(V)	1

Fig. 10 Spice model and component values of the designed VCO.

5 Simulations and results

After designing analog and digital circuits and modeling the substrate in MATLAB, simulations in HSPICE are performed. Simulations are done in 0 to 30 ns with 0.05 ns steps. The substrate is considered as lightly-doped for this paper. Other substrate characteristics are shown in table 3. The proposed substrate model is located between substrate contacts in NMOS transistors of VCO (3 contacts) and some of NMOS transistors of multiplier (9 contacts) and a contact to digital ground. Contacts' dimension is 10 μm × 10 μm, and there is a distance of 800 μm between analog and digital blocks.

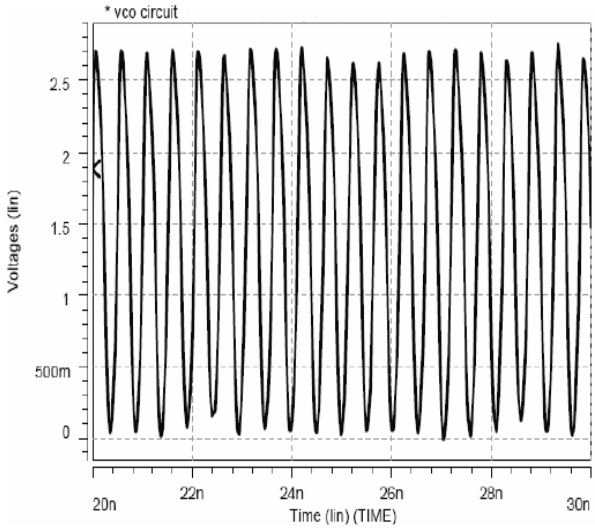


Fig. 11 Output of the simulated VCO.

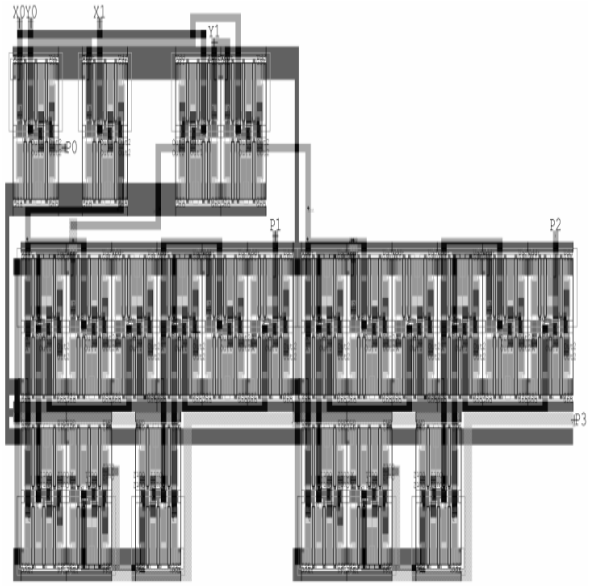


Fig. 12 Layout of the designed multiplier.

Table 3 Characteristics of substrate in this paper.

Permittivity(ε)	11.8 ε_0
Conductivity(ρ)	10Ω-cm
Substrate Height(h)	400μm

Figure 13 shows the VCO output when there is no voltage applied to the multiplier inputs. After applying voltages to the multiplier inputs (Fig. 14), it is observed that switching in multiplier's output will cause distortion in VCO output.

6 Applying noise reduction methods

There are a lot of methods for reducing substrate noise in mixed-signal circuits [3, 6, 7, 17, 18, 19]. Some of these methods, namely back-plane, P+ guard ring and separation (2000 μm) between analog and digital blocks are applied in this paper, and simulations are carried out for each of them.

Figure 15 shows the VCO output in 5 configurations: 1. without any input in multiplier, 2. after applying input to multiplier and without using any noise reduction method, 3. by using back-plane, 4. by separating the analog and digital blocks, and 5. by using a P+ guard ring. Figure 16 shows the VCO output noise in different situations, and Fig. 17 compares these noise levels with each other.

Phase Noise is one of the most important issues of a VCO which can increase in presence of the substrate noise. As is shown in Fig. 15, phase noise is at its maximum value in case 2 using no noise reduction method, but it reduces when some methods for noise reduction are applied. This is shown in Fig. 18.

Consequently, it is shown that using P+ guard ring has the best effect in reducing substrate noise.

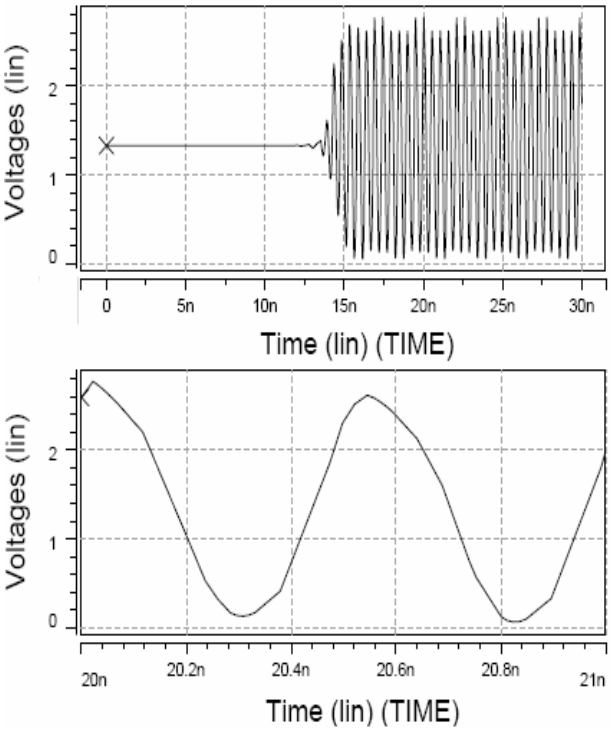


Fig. 13 VCO output when multiplier inputs are 0V.

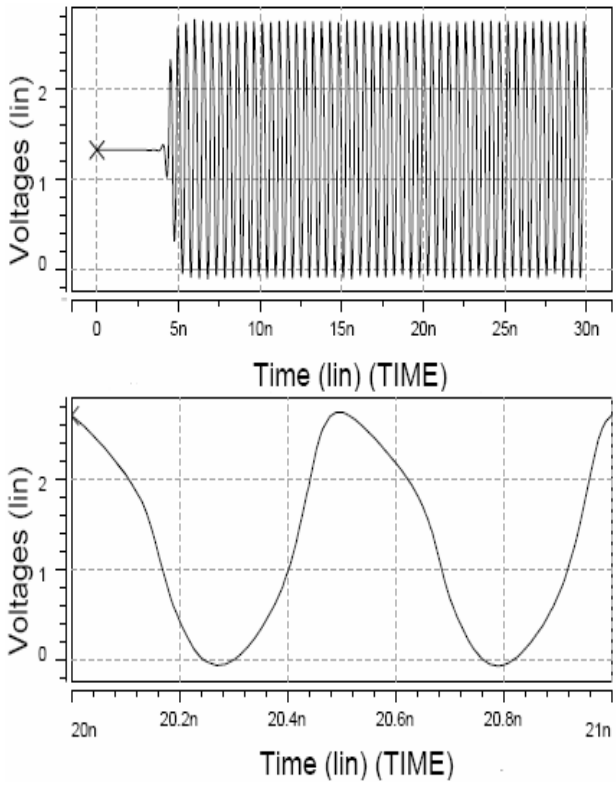


Fig. 14 VCO output when voltages are applied to multiplier inputs.

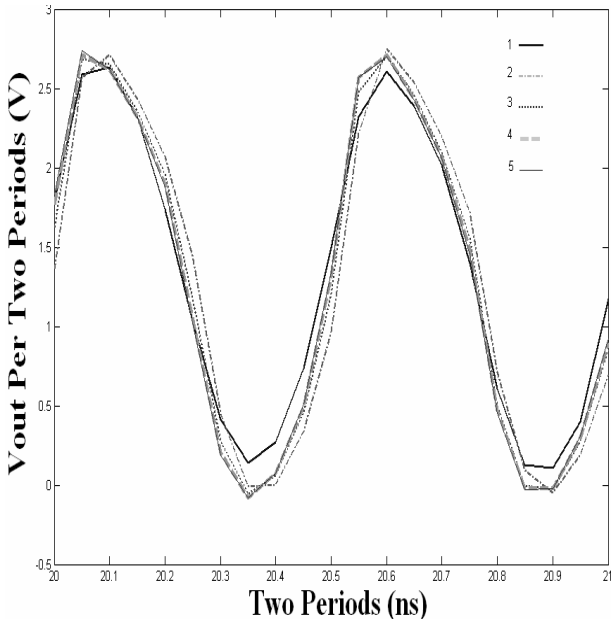


Fig. 15 VCO output for 1. without any input in multiplier, 2. with applying input to multiplier and without using any noise reduction method, 3. by using back-plane, 4. by separating the analog and digital blocks, and 5. by using P+ guard ring.

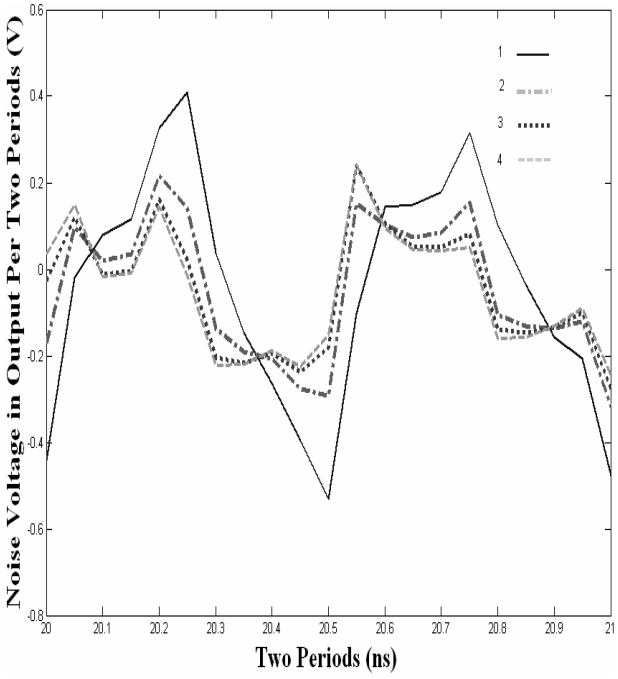


Fig. 16 VCO output noise for 1. without using any noise reduction method, 2. by using back-plane, 3. by separating the analog and digital blocks, and 4. by using P+ guard ring.

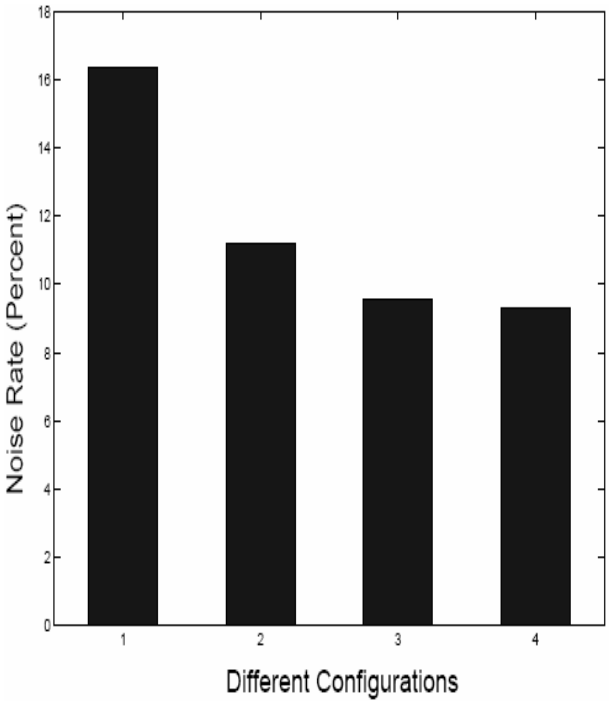


Fig. 17 Comparing noise level for 1. without using any noise reduction method, 2. by using back-plane, 3. by separating the analog and digital blocks, and 4. by using P+ guard ring.

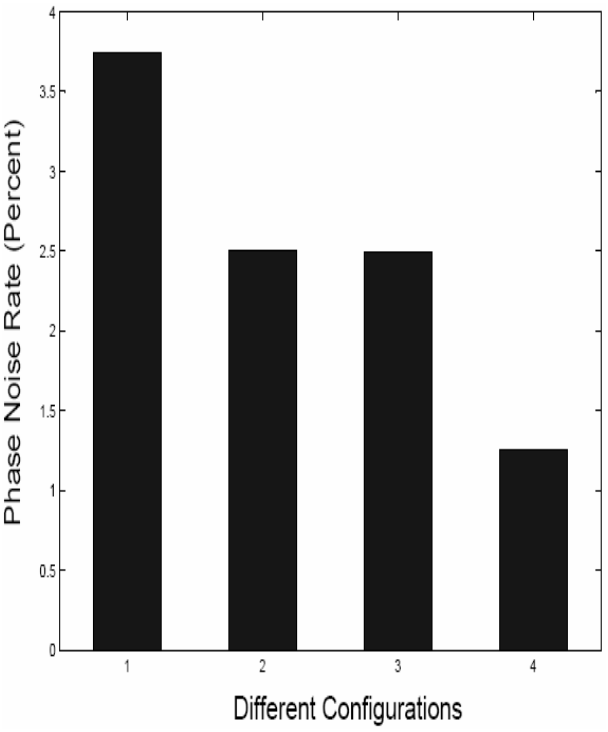


Fig. 18 Comparing phase noise for 1. without using any noise reduction method, 2. by using back-plane, 3. by separating the analog and digital blocks, and 4. by using P+ guard ring.

7 Conclusion

Substrate coupling is an important problem in mixed-signal circuit designs. This must be considered especially where fast digital blocks are used because fast switching noise in digital circuits is coupled to analog blocks through the common substrate thereby reducing the performance.

This paper introduced an applicable model, based on Green's Function, for substrate coupling which was then used by a program written in MATLAB. This model has acceptable results for small circuits. This fact was shown by comparing the achieved values in MATLAB by those implied in an IEEE-published paper. In out case, the analog block and digital block are a VCO and a multiplier, respectively. Effects of switching noise in multiplier which is coupled to VCO through the proposed model for substrate were shown in the VCO output. All simulations are accomplished in HSPICE. Some methods for noise reduction were applied and their effects compared. Results show that P+ guard ring is the best method in noise reduction. Simultaneous usage of guard rings and back-plane is suggested for obtaining the highest performance in a mixed-signal circuit.

References

[1] Xavier Aragones, Jose Luis Gonzalez and Antonio Rubio, *Analysis and Solutions for Switching Noise Coupling in Mixed-Signal IC's*, Kluwer Academic Publishers, 1999.

[2] N. Masoumi, M. I. Elmasry, and S. Safavi-Naeini, "Fast and Efficient Parametric Modeling of Contact-to-Substrate Coupling", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 11, pp. 1282-1292, 2000.

[3] R. Singh, "A Review of Substrate Coupling Issues and Modeling Strategies", *IEEE Custom Integrated Circuits Conference*, vol. 23, no. 6, pp. 491-498, 1999.

[4] P. Miliozzi, L. Carloni, E. Charbon, and A. Sangiovanni-Vincentelli, "Sub-Wave: z Methodology for Modeling Digital Substrate Noise Injection in Mixed-signal ICs", *IEEE Custom Integrated Circuits Conference*, vol. 17, no. 3, pp. 385-388, 1996.

[5] S. Kristiansson, S. P. Kagganti, T. Ewert, F. Ingvarson, J. Olsson, and K. O. Jeppson, "Substrate Resistance Modeling for Noise Coupling Analysis", *International Conference on Microelectronic Test Structures*, pp. 124-129, Mar. 2003.

[6] K. Joardar, "A Simple Approach to Modeling Cross-Talk in Integrated Circuits", *IEEE Journal of Solid-State Circuits*, vol. 29, no. 10, pp. 1212-1219, Oct. 1994.

[7] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits", *IEEE Journal of Solid-State Circuits*, vol. 28, no. 4, pp. 420-430, Apr. 1993.

[8] B. R. Stanisic, N. K. Verghese, R. A. Rutenbar, L. R. Carley, and D. J. Allstot, "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power Distribution Synthesis", *IEEE Journal of Solid-State Circuits*, vol. 29, no. 3, pp. 226-238, Mar. 1994.

[9] T. Smedes, N. P. van der Meijs, and A. J. van Genderen, "Extraction of Circuit Models for Substrate Cross-talk", *Proc. IEEE International Conference on CAD*, pp. 199-206, 1995.

[10] R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits", *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 344-353, Mar. 1996.

[11] N. K. Verghese, D. J. Allstot, and M. A. Wolfe, "Verification Techniques for Substrate Coupling and Their Application to Mixed-Signal IC Design", *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 354-365, Mar. 1996.

[12] R. Gharpurey, *Modeling and Analysis of Substrate Coupling in Integrated Circuits*, PHD Thesis, University of California at Berkeley, 1995.

[13] N. Masoumi, S. Safavi-Naeini, and M. I. Elmasry, "Efficient Green's Function for Substrate Coupling Modeling in VLSI Circuits", *in Processing of International Conference on VLSI-SOC: Systems on A Chip*, Kluwer Academic Publications, pp. 152-157, Dec. 2001.

[14] N. Masoumi, M. I. Elmasry, S. Safavi-Naeini, and H. Hadi, "A Novel Analytical Model for Evaluation of Substrate Crosstalk in VLSI Circuits", *Proceeding of the First IEEE International Workshop on Electronic Design*, Test and Applications, pp. 355-359, Jan. 2002.

[15] N. Masoumi, M. I. Elmasry, and S. Safavi-Naeini, "Modeling Techniques for Substrate Coupling for System-On-A-Chip", *The 13th International Conference on Microelectronics*, pp. 35-38, 2001.

[16] R. Aparicio, and A. Hajimiri, "A CMOS Differential Noise-Shifting Colpitts VCO", *IEEE International Solid-State Circuits Conference*, Digest of Technical Papers, vol. 2, pp. 226-227, Feb. 2002.

[17] R. J. Welch and A. T. Yang, "Substrate Coupling Analysis and Simulation for an Industrial Phase-Locked Loop", *Proceedings of IEEE International Symposium on Circuits and Systems*, vol. 6, pp. 94-97, Jun. 1998.

[18] R. Singh and S. Sali, "Substrate Noise Issues in Mixed-Signal Chip Designs Using SPICE", *10th International Conference on Electromagnetic Compatibility*, pp. 108-112, Sep. 1997.

[19] K. Makie-Fukuda, S. Maeda, T. Tsukada, and T. Matsuura, "Substrate Noise Reduction Using Active Guard Band Filters in Mixed-Signal Integrated Circuits", *Symposium on VLSI Circuits*, Digest of Technical Papers, pp. 33-34, 1995.

Golnar Khodabandehloo was born in 1981 in Hamedan, Iran. She received a B.S. degree in Electrical Engineering from Amirkabir University of Technology in 2003 and the M.S. Degree in Electrical Engineering from Iran University of Science and Technology in 2005. She is currently an instructor in Islamic Azad University, Hamedan branch.

Sattar Mirzakuchaki was born in Tehran, Iran in 1964. He received the B.S. degree in electrical engineering from University of Mississippi in USA in 1989 and the M.Sc and Ph.D also in Electrical Engineering from the University of Missouri in 1991 and 1996 respectively. He is currently an assistant professor in the electrical engineering department at IUST. His research interests include growth and characterization of semiconductor devices and VLSI design.

Gholam Reza Karimi was born in Kermanshah, Iran in 1977. He received the B.S. and M.S degrees in electrical engineering from Iran University of Science and Technology (IUST) in 1999 and 2001, respectively. He is currently pursuing the Ph.D. degree in electrical engineering at IUST. His research interests include substrate coupling noise in SOC and mixed-mode IC design.