Optimum Structures of a Cascaded Multilevel Inverter for Minimum Number of Power Electronic Devices

S. Laali*, E. Babaei*(C.A.) and Z. Saadatizadeh*

Abstract: In this paper, several optimum structures of a cascaded multilevel inverter is proposed. This optimization is based on generation a constant number of output voltage levels by using minimum number of power switches or dc voltage sources or minimum amount of blocked voltage by power switches. In addition, the optimum structure for a constant number of dc voltage sources by using minimum number of power switches is obtained. In these optimizations, all of the presented algorithms to generate a desired sinosuidal waveform of the cascaded multilevel inverter are considered. Then, the proposed optimum topologies are compared with several conventional cascaded multilevel invereters that have been presented in literature. These comparisons are from the number of required power switches, dc voltag sources, variabilty the magnitude of dc voltage source and the value of blocked voltage by switches points of view. The conduction and switching losses of the proposed topologies are calculated. In addition, a 49-level cascaded inverter based on the proposed optimum topologies is designed. Moreover, the designed topologies are compared to each other from the amount of blocked voltage by swithes, the maximum magnitude of output voltage levels and the number of required power electronic devices such as power switches, driver circuits and diodes points of view. Finally, the ability of the optimium topology in generation all voltage levels (even and odd) by using minimum number of power switches is reconfirmed thruogh PSCAD/EMTDC simulation and experimental results on a 49-level inverter.

Keywords: Multilevel inverter; cascaded multilvel inverter; basic unit; optimum structures; power electronic devices.

1 Introduction

Recently, the multilevel inverters have received more attention in comparison with traditional two-level inverter because of the capability of using in high voltage and high power applications [1]. In multilevel inverters, the desired sinusoidal waveform is generated by using several dc voltage sources as inputs. These dc voltage sources could be supplied by batteries and renewable energy sources such as fuel cells, photovoltaic and wind [2]. With an increasing the number of dc voltage sources in input side, the sinusoidal like waveform can be generated at the output. As a result, the total harmonic distortion (THD) decreases and the output waveform quality increases, which are two main advantages of the multilevel inverters [3]. In addition, lower switching losses, lower voltage stress of dv/dt on switches; high efficiency and better electromagnetic interference are other most important advantages of the multilevel inverters [4-6]. There are three main topologies and several derivation structures for voltage source multilevel inverters. These are diode-clamped multilevel inverter [7], flying capacitor multilevel inverter [8] and cascaded multilevel inverter [9]. The last one has received special attention due to the modularity, simplicity of the control and reliability. In addition, there is no need to clamping diodes or flying capacitors in cascaded multilevel inverters [10-11]. High required numbers of power semiconductor devices and insulated dc voltage sources in generation specific output level are the most important disadvantages of the cascaded multilevel inverter that lead to increase the control complexity. Therefore, the concentration of this paper is on the cascaded multilevel inverters. These multilevel inverters consist of series connection of several basic units. These basic units consist of different array of power electronic devices and dc voltage sources [12-13]. According to the structure of the basic units, the number of generated output voltage levels, used power electronic devices such as power switches, driver circuits, diodes and dc voltage sources, the installation space and the cost of the inverter will be differ. In this inverter, with an

increasing the number of producible output voltage levels in each basic unit, the sinusoidal like waveform is generated at the output and so the power quality of output waveforms is increased. In addition, the magnitude of dc voltage sources in each basic unit has most important influence in the generated output voltage levels. By considering the magnitude of dc voltage sources differently, the number of output voltage levels and the maximum producible magnitude of the output levels are increased. In this kind of cascaded multilevel inverter, there are different switching patterns to generate a specific number of output levels. This feature causes to reduce and control of the switching losses. This kind of cascaded inverter is called asymmetric cascaded multilevel inverter while by considering the magnitude of dc voltage sources equally; the other group of cascaded multilevel inverters that are called symmetric multilevel inverters are made [14]. In the symmetric ones, the variety of the value of dc voltage sources decrease that leads to more modularity of the inverter but the number of required power electronic devices to generate specific number of output levels is increased. Recently, different kinds of symmetric and asymmetric cascaded multilevel inverters have been presented in literature. One of these cascaded inverters has been presented in [15] and consists of series connected of several basic units. In the basic unit of this inverter, the number of required dc voltage sources, power electronic devices and generated output voltage levels are variable and completely depend on the number of output voltage levels. Moreover, for this basic unit in order to generate a desired output levels, three different algorithms to determine the magnitude of dc voltage sources have been presented in [13] and [15]. The main disadvantage of the presented algorithm in [15] is its inability in generation all voltage levels (even and odd) at the output. This results in presenting two other algorithms in [13].

In this paper, the cascaded multilevel inverter and its algorithms that have been proposed in [13] and [15] are represented. Then, the optimum structures of the cascaded inverter by considering its algorithms from different points of view such as the minimum number of required power switches or dc voltage sources or minimum amount of blocked voltage in a constant number of output voltage levels are proposed. It is important to note that the presented optimum topologies in [13] is only based on the first proposed algorithm while in this paper, all of the three algorithms are considered. Then, the proposed optimum structures based on different algorithms are compared with H-bridge cascaded multilevel inverter [9], [14], [16-17] and several multilevel inverters that have been presented in literature [18-26]. These topologies consist of symmetric and asymmetric cascaded inverters. The obtained results from the comparison show the advantages and disadvantages of the proposed optimum topologies. Moreover, the conduction and switching losses of the multilevel inverter are calculated and the optimum structures are compared to each other from the number of generated output levels, required semiconductor devices and the amount of blocked voltage. Then, the design of a 49-level cascaded inverter based on the proposed optimum structures is obtained. Finally, in order to verify the theoretical issues and correct performance of the designed optimum structure in generation all voltage levels by using minimum number of power switches, the simulation and experimental results on a 49-level inverter are used.

2 Review of Presented Topology in [15] with its Presented Algorithms in [13] and [15]

Fig. 1 shows the presented cascaded multilevel inverter in [15]. As it is obvious, this topology consists of n number of series connected basic units. Each basic unit consists of four unidirectional switches and $2(m_i-1)$ bidirectional ones. The bidirectional switches conduct currents in two directions and block voltages in positive and negative polarities while the unidirectional ones conduct current in two directions and block voltage in one polarity. It is important to note that, each bidirectional switches consists of two integrated gate bipolar transistors (IGBTs) with the same number of anti-parallel diodes and a driver circuit if the common emitter switch is used. In addition, the first unit, second unit, ... and n^{th} unit of the presented topology include of m_1, m_2, ... and m_n number of dc voltage sources with different amplitudes, respectively. Because of locating two powers switches between two dc voltage sources commonly, only one switch from right side and one switch from left side have to be turned on simultaneously to avoid of short circuit across dc voltage sources. In addition, for the cascaded inverter, three different algorithms to determine the magnitude of dc voltage sources have been presented in [13] and [15].

In the first algorithm that leads to generate maximum number of output voltage levels, the magnitude of dc voltage sources is selected as follows [15]:

$$V_{1,n} = V_{dc} + 2\sum_{i=1}^{n-1}\sum_{j=1}^{m_i} V_{j,i} = \prod_{i=1}^{n-1}(2^{m_i+1}-1)\,V_{dc} \qquad (1)$$

$$V_{j,n} = 2^{j-1}V_{1,n} \qquad for\ j = 2, 3, \cdots, m_1 \qquad (2)$$

According to this algorithm, it is impossible to generate all voltage level at the output. For instance, by considering $n=1$ and $m=4$, the magnitude of dc voltage sources are V_{dc}, $2V_{dc}$, $4V_{dc}$ and $8V_{dc}$ and the inverter is able to produce 21 levels at the output. While, the output levels of $\pm 5V_{dc}$, $\pm 9V_{dc}$, $\pm 10V_{dc}$, $\pm 11V_{dc}$ and $\pm 13V_{dc}$ could not be generated by this algorithm. Generally, if more than two dc voltage sources are used in each unit, it is impossible to generate all voltage levels (even and odd) at the output.

In the second algorithm to generate all voltage levels (even and odd) at the output, the magnitude of dc voltage sources is considered as follows [13]:

$$V_{1,n} = V_{dc} + 2\sum_{i=1}^{n-1}\sum_{j=1}^{m_i} V_{j,i} = \prod_{i=1}^{n-1}(4m_i - 1)\,V_{dc} \tag{3}$$

$$V_{j,n} = 2\,V_{1,n} \qquad for\ \ j = 2,\ 3,\ \cdots,\ m_1 \tag{4}$$

In order to reduce the variety of the value of dc voltage sources, another algorithm to determine the magnitude of dc voltage sources has been presented in [13]. According to this algorithm the value of dc voltage sources are selected as follows:

$$\begin{aligned} V_{j,n} &= V_{dc} + 2\sum_{i=1}^{n-1}\sum_{j=1}^{m_i} V_{j,i} \\ &= \prod_{i=1}^{n-1}(2m_i + 1) \qquad for\ \ j = 2,\ 3,\ \cdots,\ m_1 \end{aligned} \tag{5}$$

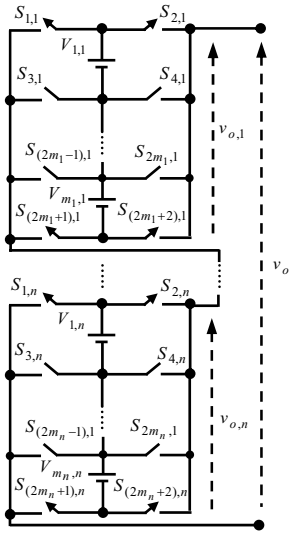


Fig. 1 The presented multilevel inverter in [15].

3 Proposed Optimum Structures

There are different arrays of power electronic devices in the multilevel inverter to generate different output levels. Therefore, in order to generate constant number of output voltage levels by using minimum number of dc voltage sources or power switches or even minimum amount of blocked voltage, optimum structures have to be obtained. Considering the variety of existing structures, following some of the optimum topologies are proposed.

In addition, for the shown cascaded inverter in Fig. 1, the maximum number of output voltage levels by using minimum number of dc voltage sources is generated when the same numbers of dc voltage sources are used in all units. In other word:

$$m_1 = m_2 = m_3 = \cdots = m_n = m \tag{6}$$

In this condition, the number of power switches (N_{switch}), IGBTs (N_{IGBT}), driver circuits (N_{driver}), dc voltage sources (N_{source}) and the variety of the value of dc voltage sources ($N_{variety}$) are obtained as follows, respectively:

$$N_{switch} = 2n(m+1) \tag{7}$$

$$N_{IGBT} = 4mn \tag{8}$$

$$N_{driver} = 2n(m+1) \tag{9}$$

$$N_{source} = nm \tag{10}$$

$$N_{variety} = nm \tag{11}$$

3.1 Optimum Structure for The Minimum Number of Power Switches with Constant Number of dc Voltage Sources

In this sub-section, the main aim is to introduce an optimum structure in which the minimum number of power switches is required while constant numbers of dc voltage sources are used. The number of dc voltage sources for the presented inverter in Fig. 1 is calculated as follows:

$$N_{source} = m_1 + m_2 + \cdots + m_n = cte \tag{12}$$

The number of power switches is calculated as follows:

$$N_{switch} = \sum_{i=1}^{n}(2m_i + 2) = 2(m_1 + m_2 + \cdots + m_n) + 2n \tag{13}$$

Considering (12) and (13), the number of switches is equal to:

$$N_{switch} = 2N_{source} + 2n \tag{14}$$

According to (14), the number of power switches will be minimized when the number of units (n) is minimized. In other word, the number of power switches is minimized while one unit is used. It is clear that in this condition, the number of output voltage level will extremely reduce. Fig. 2(a) shows this optimum structure.

3.2 Optimum Structure for Minimum Number of Power Switches with Constant Number of Output Voltage Levels

The main aim of the multilevel inverter is generating maximum number of output voltage levels by using minimum number of switches. In this sub-section, the question is that which topology generates a constant number of output voltage levels by using minimum number of power switches? The number of output voltage levels in the cascaded multilevel inverter is obtained as follows:

$$N_{level} = \prod_{i=1}^{n} N_{level,i} = \prod_{i=1}^{n}\left[m_i\,(m_i + 1) + 1\right] \tag{15}$$

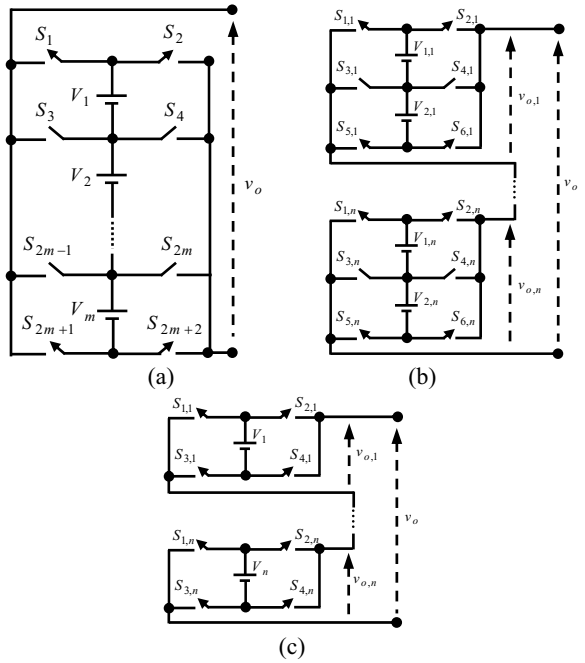


Fig. 2 Optimum topologies; (a) for minimum number of power switches in a constant number of dc voltage sources; (b) for minimum number of switches with constant number of output voltage levels for the first and second algorithms; (c) for minimum number of switches with constant number of output voltage levels for third algorithm.

Considering (6), the equation (15) is rewritten as follows:

$$N_{level} = (am^2 + bm + c)^n \tag{16}$$

where a, b and c are coefficients that are depends on used different algorithms. The number of output voltage levels based on the first, second and third presented algorithms are calculated as follows, respectively:

$$N_{level,1} = \left[m(m+1)+1\right]^n \tag{17}$$

$$N_{level,2} = (4m-1)^n \tag{18}$$

$$N_{level,3} = (2m+1)^n \tag{19}$$

Considering (17) to (19), Table 1 shows these coefficients in the first, second and third algorithm.

Table. 1 Coefficients of output voltage levels for first, second and third algorithm.

Determination algorithm of the magnitudes of dc voltage sources	Coefficients		
	a	b	c
First algorithm	1	1	1
Second algorithm	0	4	−1
Third algorithm	0	2	1

Moreover, (16) can be rewritten as follows:

$$n = \frac{\ln(N_{level})}{\ln(am^2 + bm + c)} \tag{20}$$

Considering (7) and (20), the number of power switches is equal to:

$$N_{switch} = \frac{2(m+1)}{\ln(am^2 + bm + c)} \ln(N_{level}) \tag{21}$$

By minimizing $\frac{2(m+1)}{\ln(am^2 + bm + c)}$, the equation (21) will be minimized. Fig. 3(a) indicates the variation of $\frac{2(m+1)}{\ln(am^2 + bm + c)}$ versus m. As it is obvious, the minimum number of power switches is obtained when $m = 2$ for the first and second algorithms while this amount is $m = 1$ for the third algorithm. It is necessary to point out that the number of used elements in each unit is an integer number, so if the calculated number is not an integer number, the nearest integer number is certainly proposed answer. This structure is shown in Figs. 2(b) and 2(c).

The numbers of output voltage levels, power switches, IGBTs, driver circuits and dc voltage sources and the variety of the value of dc voltage sources for the optimized topology that is shown in Fig. 2(b) are equal as follows, respectively:

$$N_{level} = 7^n \tag{22}$$

$$N_{switch} = 6n \tag{23}$$

$$N_{IGBT} = 8n \tag{24}$$

$$N_{driver} = 6n \tag{25}$$

$$N_{source} = 2n \tag{26}$$

$$N_{variety} = 2n \tag{27}$$

In this condition, the maximum producible output voltage and the amount of blocked voltage by switches in the optimum structure that is shown in Fig. 2(b) are calculated as follows, respectively:

$$V_{o,\max} = \frac{7^n - 1}{2} V_{dc} \tag{28}$$

$$V_{block} = \frac{8}{3}(7^n - 1)V_{dc} \tag{29}$$

The number of output voltage levels, power switches, IGBTs, driver circuits, dc voltage sources and the variety of the value of dc voltage sources for the optimized topology that is shown in Fig. 2(c) are equal as follows, respectively:

$$N_{level} = 3^n \tag{30}$$

$$N_{switch} = 4n \tag{31}$$

$$N_{IGBT} = 4n \tag{32}$$

$$N_{driver} = 4n \tag{33}$$

$$N_{source} = n \tag{34}$$

$$N_{variety} = n \tag{35}$$

As it is obvious from Fig. 2(c) and based on (31) to (33), the number of switches, IGBTs and driver circuits are equal. The maximum producible output voltage and the amount of blocked voltage by switches in the

optimum structure shown in Fig. 2(c) are calculated as follows, respectively:

$$V_{o,\max} = \frac{3^n - 1}{2} V_{dc} \tag{36}$$

$$V_{block} = 2(3^n - 1)V_{dc} \tag{37}$$

3.3 Optimum Structure for Minimum Number of dc Voltage Sources with Constant Number of Output Voltage Levels

In this sub-section, it is required to know that which topology generates specific output voltage levels while the minimum number of dc voltage sources is used. The number of dc voltage sources is equal to:

$$N_{source} = m_1 + m_2 + \cdots + m_n \tag{38}$$

Considering (6) and (20) and replacing them into (38), the number of output voltage levels is rewritten as follows:

$$N_{source} = nm = \frac{m}{\ln(am^2 + bm + c)} \ln(N_{level}) \tag{39}$$

By reducing the value of $\frac{m}{\ln(am^2 + bm + c)}$, the number of dc voltage sources decreases while the number of output levels is constant. Fig. 3(b) indicates the variation of $\frac{m}{\ln(am^2 + bm + c)}$ versus m.

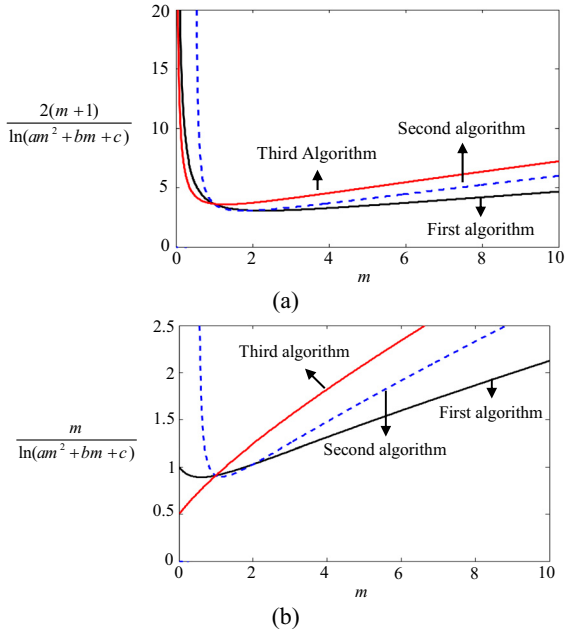


Fig. 3 (a) Variation of $\frac{2(m+1)}{\ln(am^2 + bm + c)}$ versus m; (b) Variation of $\frac{m}{\ln(am^2 + bm + c)}$ versus m.

It is obvious that the minimum number of required dc voltage sources for generation specific number of output voltage is obtained for $m = 1$ (Fig. 2(c)). The number of output voltage levels, power switches, IGBTs, driver circuits and dc voltage sources, the variety of the value of dc voltage sources, the maximum producible output voltage and the amount of blocked voltage by switches are calculated by (30) to (37), respectively.

3.4 Optimum Structure for Minimum Value of Blocked Voltage by Switches with Constant Number of Output Voltage Levels

The current and voltage ratings of switches have the most significant role in determining the cost of the multilevel inverters. In all topologies, the current of all switches are as same as the load current. This feature is incorrect from voltage point of view. Therefore, the amount of blocked voltage by switches could be considered as a significant index for comparison different topologies. If the number of output voltage levels be constant, which topology makes the minimum amount of blocked voltage?

The amount of blocked voltage for n number of series connected units for the first, second and third proposed algorithms are written as follows, respectively:

$$\begin{aligned} V_{block} &= m2^{m+1}(V_{1,1} + V_{1,2} + \cdots + V_{1,n}) \\ &= m2^m \left[\frac{(2^{m+1} - 1)^n - 1}{2^m - 1} \right] V_{dc} \end{aligned} \tag{40}$$

$$\begin{aligned} V_{block} &= (3m^2 + 3m - 2)(V_{1,1} + V_{1,2} + \cdots + V_{1,n}) \\ &= (3m^2 + 3m - 2) \frac{(4m-1)^n - 1}{4m - 2} V_{dc} \end{aligned} \tag{41}$$

$$V_{block} = \begin{cases} \left(\frac{3}{2}m^2 + 2m \right) \frac{(2m+1)^n - 1}{2m} V_{dc} \\ for\ m = even\ number \\ \left(\frac{3}{2}m^2 + 2m + \frac{1}{2} \right) \frac{(2m+1)^n - 1}{2m} V_{dc} \\ for\ m = odd\ number \end{cases} \tag{42}$$

By replacing (20) into (40) to (42), the value of blocked voltage by switches based on the first, second and third algorithms are calculated as follows, respectively:

$$V_{block} = m2^m \frac{(2^{m+1} - 1)^{\left\lceil \frac{\ln(N_{level})}{\ln[m(m+1)+1]} \right\rceil} - 1}{2^m - 1} V_{dc} \tag{43}$$

$$V_{block} = (3m^2 + 3m - 2) \frac{(4m-1)^{\left\lceil \frac{\ln(N_{level})}{\ln(4m-1)} \right\rceil} - 1}{4m - 2} V_{dc} \tag{44}$$

$$V_{block}=\begin{cases}\left(\frac{3}{2}m^2+2m\right)\frac{(2m+1)^{\left[\frac{\ln(N_{level})}{\ln(2m+1)}\right]}-1}{2m}\,V_{dc} \\ \text{for } m=\text{even number} \\ \left(\frac{3}{2}m^2+2m+\frac{1}{2}\right)\frac{(2m+1)^{\left[\frac{\ln(N_{level})}{\ln(2m+1)}\right]}-1}{2m}\,V_{dc} \\ \text{for } m=\text{odd number}\end{cases} \quad (45)$$

The variations of V_{block} versus m for different algorithms are shown in Fig. 4. In this figure, V_{dc} is considered as a basic value in per unit system. As it is obvious from Fig. 4, the minimum value of blocked voltage is obtained by $m=1$. Therefore, the optimum structure from minimum amount of blocked voltage point of view is obtained by series connection of several units with a dc voltage source in each unit (Fig. 2(c)). In this condition, the number of output voltage levels, power switches, IGBTs, driver circuits and dc voltage sources, the variety of the value of dc voltage sources, the maximum producible output voltage and the amount of blocked voltage by switches are calculated by (30) to (37), respectively.

4 Comparing the Proposed General Topology with the Conventional Topologies

In order to clarify the advantages and disadvantage of the proposed optimum topologies, they should be compared with different kinds of presented topologies in literature. In this comparison, the optimum topologies that are shown in Figs. 2(a) to 2(c) are considered as P_1-P_6, respectively. In other word, the proposed topology in Fig. 2(a) with three different algorithms are considered by P_1-P_3, respectively and the proposed topology in Fig. 2(b) with two different algorithms is considered by P_4-P_5, respectively and finally the proposed one in Fig. 2(c) is considered as P_6. In [9], the H-bridge cascaded multilevel inverter has been presented. This inverter is known as symmetric one. In this comparison, the symmetric H-bridge cascaded multilevel inverter is indicated by R_1. In addition, two different algorithms for H-bridge cascaded multilevel inverter with the binary and trinary methods to determine the magnitude of dc voltage sources have been presented in [16] and are shown by R_2-R_3. Two other algorithms have been presented for this topology in [14] and [17] which are indicated by R_4-R_5, respectively. In addition, three different symmetric cascaded multilevel inverter have been presented in [18-20] that are considered by R_6 and $R_{10}-R_{11}$, respectively. In [21], another cascaded multilevel inverter based on three different algorithms has been presented that are considered by R_7-R_9 in this comparison. Fig. 5 indicates all of the above-mentioned topologies.

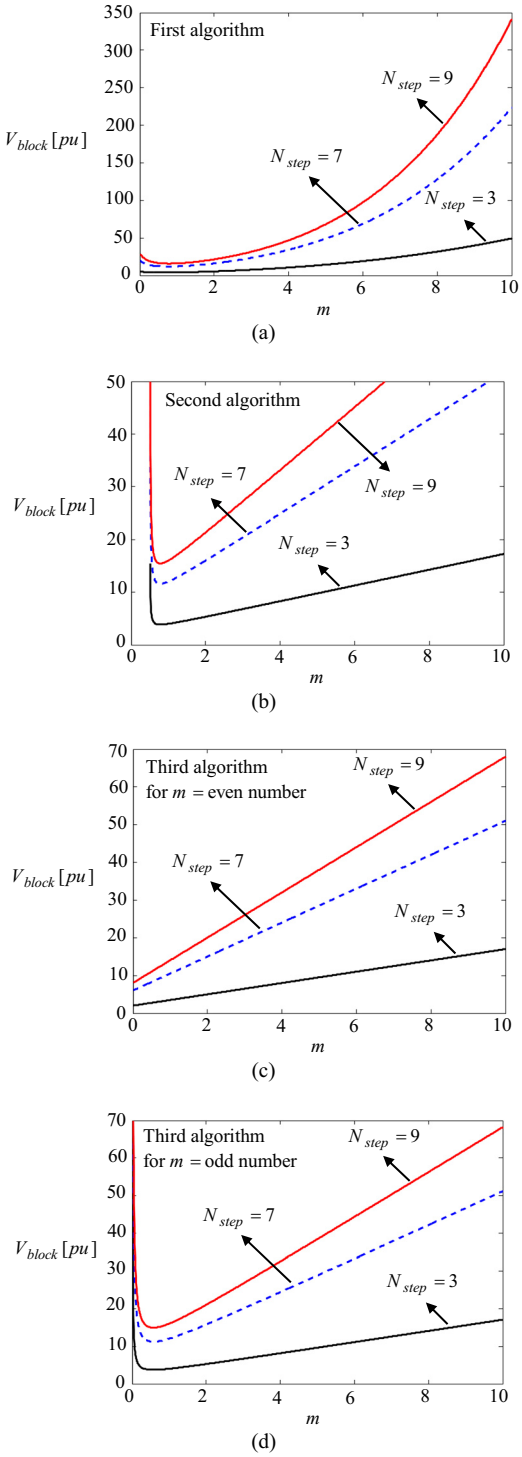


Fig. 4 variation of V_{block} versus m; (a) first algorithm; (b) second algorithm; (c) third algorithm for even number of m; (d) third algorithm for odd number of m.

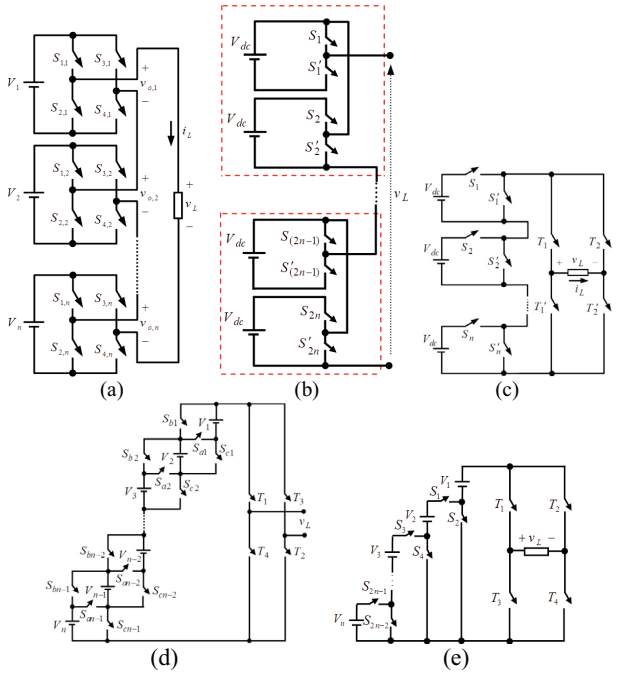


Fig. 5 The cascaded multilevel inverters; (a) H-bridge cascaded multilevel inverter R_1 for $V_1 = V_2 = \cdots = V_n = V_{dc}$ [9], R_2 for $V_1 = V_{dc}, V_2 = 2V_{dc} \cdots, V_n = (2^{n-1})V_{dc}$, R_3 for $V_1 = V_{dc}, V_2 = 3V_{dc} \cdots, V_n = (3^{n-1})V_{dc}$ [16], R_4 for $V_1 = V_{dc}, V_2 = \cdots = V_n = 2V_{dc}$ [14], R_5 for $V_1 = V_{dc}, V_2 = \cdots = V_n = 3V_{dc}$ [17]; (b) presented topology in [18] R_6 for $V_1 = V_2 = \cdots = V_n = V_{dc}$; (c) presented topology in [21] R_7 for $V_1 = V_2 = \cdots = V_n = V_{dc}$, R_8 for $V_1 = V_{dc}, V_2 = 2V_{dc} \cdots, V_n = (2^{n-1})V_{dc}$, R_9 for $V_1 = V_{dc}, V_2 = \cdots = V_n = 2V_{dc}$; (d) presented topology in [19] R_{10} for $V_1 = V_2 = \cdots = V_n = V_{dc}$; (e) presented topology in [20] R_{11} for $V_1 = V_2 = \cdots = V_n = V_{dc}$.

Fig. 6(a) compares the number of power switches of the proposed optimum topologies with the above-mentioned cascaded multilevel inverters. It is obvious that the proposed optimum inverters require less number of power switches in comparison with other mentioned topologies to generate particular levels. This feature is remarkable when the presented optimum topology by P_4 is considered because as mentioned in section IV the optimum structure for minimum number of used power switches is shown in Fig. 2(b) and is considered by P_4. On the other words, the number of required switches in the proposed topology not only is lower than the topologies with bidirectional switches but also it is even less than the topologies with unidirectional switches. It is important to note that in the proposed optimum topologies, the number of power diodes is as same as the number of switches and driver circuits. As a result, the proposed topologies have better feature in these points of view.

In Fig. 6(b), the number of dc voltage sources of the proposed optimum inverters is compared with the above-mentioned cascaded multilevel inverters. As shown in this figure, the number of required dc voltage sources in the proposed optimum inverters is less than other presented multilevel inverters in the literature. This difference will be higher while the P_6 is considered among all proposed optimum topologies because the related structures to the P_6 is considered as optimum structure from the number of required dc voltage sources point of view. However, the number of dc voltage sources in the presented inverter by R_3 is as same as the proposed optimum topology by P_6. In addition, there is a difference between the proposed optimum topologies. For instance, the optimum topology that is shown by P_1 needs higher number of dc sources than the proposed optimum topology that is shown by P_2 until 18 levels approximately but after this level as shown in Fig. 6(b), P_1 requires lower number of dc voltage sources than P_2. There is the same explanation between the proposed topology by P_4 and the presented inverter by R_5 because their performance is change after approximately 20 levels in a way that after this level the proposed inverter by P_4 needs lower number of dc sources than the presented inverter by R_5.

Fig. 6(c) compares the variability in the magnitude of the dc voltage sources of the proposed optimum inverters with the above-mentioned cascaded multilevel inverters. As it is obvious, the proposed inverter as p_3 has minimum variability in the magnitude of the dc voltage sources than other proposed optimum inverters and conventional cascaded inverters. This feature is as one of the remarkable factors in determining the cost of the inverter. However, this feature in the proposed topology is similar to the presented topologies in R_1, R_6, R_{10} and R_{11}. In addition, there is a difference between the proposed optimum topology by P_4 and the presented inverter by R_2. As shown in Fig. 6(c), before 7 levels the variability of the value of dc voltage sources in the inverter P_4 is higher than this parameter in inverter R_2 but after this level the proposed inverter by P_4 consists of lower variability of the value of dc voltage sources than the inverter R_2.

In Fig. 6(d), the maximum amount of blocked voltage by power switches in the proposed optimum inverters is compared with the other above-mentioned cascaded multilevel inverters. As it is obvious, the proposed optimum inverter as p_6 generates lower amount of blocked voltage by switches than other proposed optimum inverters and conventional cascaded inverters because as mentioned in section IV, the

optimum proposed structure for minimum amount of blocked voltage is shown in Fig. 2(c) and is considered by p_6 in this comparison. This value in the proposed inverter is as same as presented inverters as R_1 to R_6. However, this inverter has different advantages in comparison to the presented topologies by R_1 to R_6 such as its required lower number of power switches, driver circuits and dc voltage sources. It is point out that all values are considered in per unit and V_{dc} is used as the base value in per unit system.

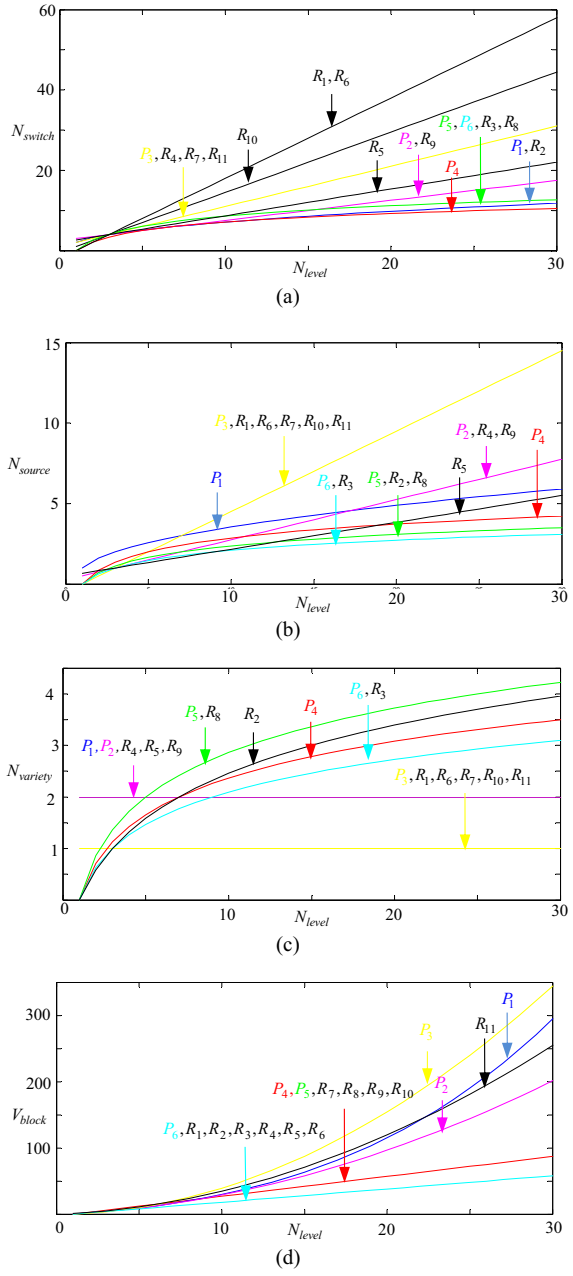


Fig. 6 (a) Variation of N_{switch} versus N_{level}; (b) Variation of N_{source} versus N_{level}; (c) Variation of N_{variety} versus N_{level}; (d) Variation of V_{block} versus N_{level}.

5 Calculation the Conduction and Switching Losses of the Proposed Topologies

The calculation of the power switches losses is the most important part of estimating losses in the power electronic converters. These kinds of switches consist of two different losses: conduction losses and switching losses. The conduction losses are made by the resistance and inverse voltage of the conduction state and switching losses are made by non-ideal switching. Although the value of the losses are different in different topologies and control methods but the method of calculation the losses of a switch is same for different topologies and control methods. Therefore, it is better to calculate the losses of a switch without considering the control method and or topology and then develop the obtained results to a converter based on the control method and its structure.

5.1 Conduction Losses

In order to calculate the conduction losses in the multilevel inverter, it is better to calculate the losses of a transistor and a diode in conduction state firstly and then develop it to the multilevel inverter. The equivalent circuit of the conduction state for a diode and a transistor are shown in Figs. 7(a) and 7(b), respectively. As shown in Fig. 7(a), it is possible to consider the turned on state of a diode by an inverse voltage with the magnitude of $V_{on,D}$ and a constant and linear series connected resistant with the value of R_D. As it can be also seen from Fig. 7(b) that it is possible to consider the turned on state of a transistor by an inverse voltage with the magnitude of $V_{on,T}$ and a constant series connected resistant with the value of R_T that can be nonlinear totally. In order to simplify the calculation and analysis of the transistor's losses, its resistance is considered constant and linear in turned on state. According to Fig. 7, the conduction losses of the transistor ($p_{c,T}(t)$) and a diode ($p_{c,D}(t)$) are equal to:

$$p_{c,T}(t) = [V_{on,T} + R_T i^{\beta}(t)]i(t) \quad (46)$$

$$p_{c,D}(t) = [V_{on,D} + R_D i(t)]i(t) \quad (47)$$

In (46), β is a constant coefficient that is depends on the characteristic of the transistor.

It is clear form (46) and (47) that it is possible to obtain the losses value of the transistor and diode by determining the current waveform of each of them. It is noted that the average losses are mostly considered and the value of transient losses are not considered. By considering T as a time of duty cycle, the average losses of a transistor ($P_{c,T}$) and a diode ($P_{c,D}$) are calculated as follows:

$$P_{c,T} = \int_T p_{c,T}(t)dt \quad (48)$$

$$P_{c,D} = \int_T p_{c,D}(t)dt \tag{49}$$

The conduction losses of a multilevel inverter are obtained as follows:

$$P_c = \sum_{j=1}^{N_{transistor}} \left\{ \frac{1}{\pi} \int_0^{\pi} \left[\left(f_{D,j}(t) V_{D,j} + f_{D,j}(t) R_{D,j} i(t) \right) i(t) \right] d(\omega t) \right\}$$
$$+ \sum_{j=1}^{N_{diode}} \left\{ \frac{1}{\pi} \int_0^{\pi} \left[\left(f_{T,j}(t) V_{T,j} + f_{T,j}(t) R_{T,j} i^{\beta}(t) \right) i(t) \right] d(\omega t) \right\} \tag{50}$$

In (50), $f_{T,j}(t)$ and $f_{D,j}(t)$ are the switching function of the j^{th} transistor and j^{th} diode, respectively. In addition, $N_{transistor}$ and N_{diode} are the number of used transistors and diodes in the circuit. When the considered semiconductor element is in the current way, the value of its switching function is equal to 1 and otherwise is equal to zero. The (50) is mentioned the conduction losses totally and it can be simpler for different topologies.

(a) (b)

Fig. 7 (a) Turned on model of a diode; (b) Turned on model of a transistor.

5.2 Switching Losses

In order to calculate the switching losses, the losses of a switch are calculated firstly. It is also assumed that during the switching, the voltage and current of the switch are considered linear. Therefore, the variation of the switch current and voltage are shown in Fig. 8. These waveforms in the turned on and off states of the switch are shown in Figs. 8(a) and 8(b), respectively.

As the loosed energy are obtained based on the integral of the loosed power and by considering Fig. 8, the relation of the loosed energy when the switch is turned off for the first time is obtained as follows:

$$E_{off} = \int_0^{t_{off}} v(t) i(t) dt$$
$$= \int_0^{t_{off}} \left[\left(\frac{V_{sw}}{t_{off}} t \right) \left(-\frac{I_{sw}}{t_{off}} (t - t_{off}) \right) \right] dt = \frac{1}{6} V_{sw} I_{sw} t_{off} \tag{51}$$

In above relation, $v(t)$ and $i(t)$ are considered as switch voltage and current during switching. In addition, V_{sw} is the switch voltage after it is turned off and I_{sw} is the switch current before it is turned off. t_{off} is the necessity time for turning off the switch completely. The relation of the loosed energy when the switch is turned on for the first time is obtained as follows:

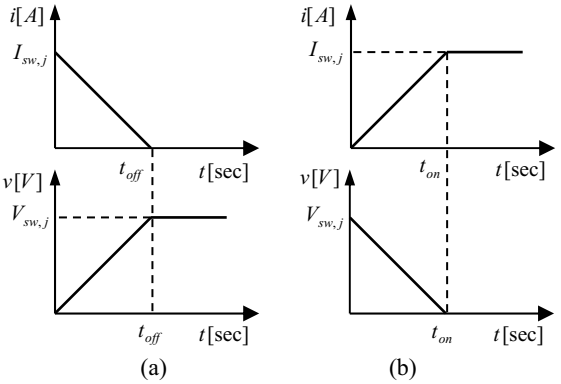
$$E_{on} = \int_0^{t_{on}} v(t) i(t) dt$$
$$= \int_0^{t_{on}} \left[\left(\frac{V_{sw}}{t_{on}} t \right) \left(-\frac{I_{sw}}{t_{on}} (t - t_{on}) \right) \right] dt = \frac{1}{6} V_{sw} I_{sw} t_{on} \tag{52}$$

In (52), V_{sw} is the switch voltage after the switch is turned on and I_{sw} is the switch current before it is turned on. t_{on} is the necessity time for turning on the switch completely.

(51) and (52) show that by determining the value of the voltage and current in each time, the loosed energy value of switching can be calculated. Totally, the relation of the switching losses can be obtained as same as conduction losses. The switching losses are depending on the number of switching and modulation strategy. It is totally mentioned that the value of loosed switching power is obtained by dividing the sum of loosed switching energy of each switch in a half duty cycle to the time of this half duty cycle. As a result, the average value of switching power losses (P_{sw}) is calculated as follows:

$$P_{sw} = 2f \left[\sum_{k=1}^{N_{switch}} \left(\sum_{j=1}^{N_{on,k}} E_{on,kj} + \sum_{j=1}^{N_{off,k}} E_{off,kj} \right) \right] \tag{53}$$

In (53), $E_{on,kj}$ is the loosed energy of the k^{th} switch during its j^{th} time of turning on and $E_{off,kj}$ is the loosed energy of the k^{th} switch during its j^{th} time of turning off. In addition, $N_{on,k}$ and $N_{off,k}$ are the number of turning on and off states of the k^{th} switch during half cycle.



(a) (b)

Fig. 8 The variation of the switch current and voltage; (a) in the turned on state; (b) in the turned off state.

6 Design of a Multilevel Inverter

In this section, in order to investigate the correct performance of the proposed optimum topologies with their algorithms in generation all voltage levels, a

multilevel inverter is designed. The main aim is to design a 360V single-phase multilevel inverter with minimum number of 49 levels. The optimum proposed structures in the previous sections could be used for this design. Therefore, the number and array of units and their necessities power electronic devices will be differed. As a result, the design of required multilevel inverter based on optimum structures and their algorithms will separately investigate.

6.1 Design of Multilevel Inverter Based on First Algorithm

If the design of an optimum topology with minimum number of power switches in a constant number of voltage levels is considered based on (22) two series connected basic units are required. According to Fig. 2(b), two dc voltage sources are used to obtain this optimum structure. Considering (28), the value of each voltage step (V_{dc}) is equal to 15V. This topology is shown in Fig. 9(a). In addition, by applying (23), (24) and (27), the variety of the value of dc voltage sources, the number of switches and IGBTs are equal to 4, 12 and 16, respectively. It is important to note that the number of switches in this structure is as same as the number of driver circuits. Based on (29), the amount of blocked voltage by switches will be 1920V.

If the design of an optimum topology with minimum number of dc voltage sources in a constant number of voltage levels is considered, four series connected basic units are required based on (30). In other word, $N_{level}=3^4=81$. According to (36), the value of each voltage step (V_{dc}) is equal to 9V. This topology is shown in Fig. 9(b). Considering (31) to (33), the number of switches, IGBTs and driver circuits, which are same as each other are equal to 16. This feature is because of using the unidirectional switches in this topology. Moreover, the number of used dc voltage sources and the variety of the value of dc voltage sources are equal to 1, similarly. Considering (37), the amount of blocked voltage by switches will be 1440V.

If the design of an optimum topology with the minimum amount of blocked voltage by switches in a constant number of voltage levels is considered, based on (30), four series connected units are needed. In other word, $N_{level}=3^4=81$. This topology is as same as the shown topology in Fig. 9(b). In this optimum topology, (30) to (35) and (37) calculate the number of output voltage levels, switches, IGBTs and dc voltage sources, the variety of the value of dc voltage sources and the amount of blocked voltage. Therefore, the obtained results for the optimum structure by using minimum number of dc voltage source are as same as the obtained structure for minimum amount of blocked voltage. In other word, $N_{switch}=N_{IGBT}=N_{driver}=4n=16$, $V_{block}=1440V$ and $N_{source}=N_{variety}=n=4$.

As it is obvious, the proposed topology from the minimum number of power switches point of view requires less number of switches and driver circuits than other proposed structures in this section. These results lead to reduce the installation space and total cost of the inverter. In addition, the variety of the value of dc voltage sources, the number of IGBTs and dc voltage sources in all proposed optimum topologies are same. However, the amount of blocked voltage in optimum topology by using the minimum number of power switches is higher than two other topologies. This feature is because of using the high amplitude for dc voltage sources in this topology. It is important to note that this inverter (Fig. 9(a)) is able to generate 49 levels at the output but the topology shown in Fig. 9(b) generates 81 levels at the output. Therefore, it will be anticipated that the waveform of the proposed topology in Fig. 9(b) is nearest to the sinusoidal waveform than the indicated topology in Fig. 9(a).

6.2 Design of Multilevel Inverter Based on Second Algorithm

In this section, the design of proposed optimum topology by using second algorithm is considered. If the design of optimum topology by using the minimum number of power switches in a constant number of voltage levels is considered, the topology is as same as the shown topology in Fig. 9(a). Therefore, this inverter consists of two basic units with two dc voltage sources in each unit. The magnitude of dc voltage sources has to be 15V to generate 49 levels at the output. The number of switches, IGBTs and driver circuits are equal to 12, 16 and 12, respectively. By applying (26) and (27), the number of dc voltage sources is as same as the variety of the value of dc voltage source and are equal to four. Considering (30), the amount of blocked voltage by switches will be 1920V.

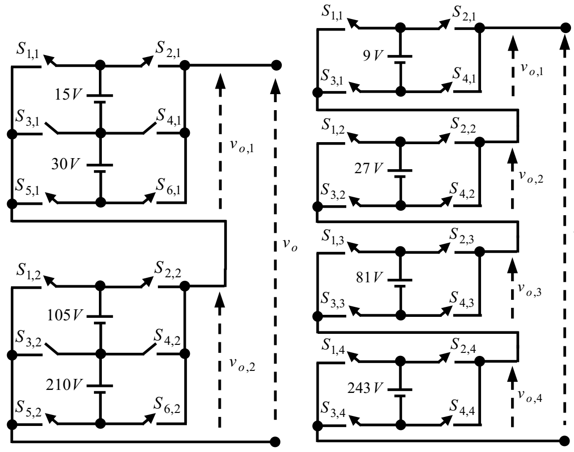
If the design of optimum topology by using the minimum number of dc voltage sources and minimum amount of blocked voltage by switches in a constant number of voltage levels is considered, the topology is shown in Fig. 9(b). According to (30), this inverter is able to generate 81 levels with the maximum magnitude of 360V at the output. Considering (36), the value of each voltage step (V_{dc}) is equal to 9V. As a result, by using (30) to (35) and (37) the number of output voltage levels, switches, IGBTs and dc voltage sources, the variety of the value of dc voltage sources and the amount of blocked voltage by switches are equal to $N_{switch}=N_{IGBT}=N_{driver}=4n=16$, $V_{block}=1440V$ and $N_{source}=N_{variety}=n=4$, respectively. The obtained results by comparing of these topologies from the number of output voltage levels, the variety of dc voltage source and the amount of blocked voltage points of view are as same as the obtained results in previous sub-sections.

6.3 Design of Multilevel Inverter Based on Third Algorithm

This design consists of the optimum topologies that decrease the required number of power electronic devices for specific number of output voltage levels. As mentioned before, the optimum topologies for minimum number of required switches or dc voltage sources or minimum amount of the blocked voltage by switches points of view based on third proposed algorithm consist of only one dc voltage source in each unit. By considering (30), in order to generate minimum 49 levels at the output, it is needed four numbers of basic units to connect in series and generate 81 levels at the output. This structure is shown in Fig. 9(b). According to (36), the magnitude of dc voltage sources (V_{dc}) is equal to 9V. In this optimum topology, (30) to (35) and (37) calculate the number of output voltage levels, switches, IGBTs and dc voltage sources, the variety of the value of dc voltage sources and the amount of blocked voltage. In other word, $N_{switch} = N_{IGBT} = N_{driver} = 4n = 16$ $N_{source} = N_{variety} = n = 4$ and $V_{block} = 1440V$. Table 2 summarizes the number of required power electronic devices for designed optimum structures by using first, second and third algorithm.

Table. 2 The number of required power electronic devices in designed optimum topologies.

Optimum structures	First algorithm	Second algorithm	Third algorithm
Minimum number of switches in a constant number of output levels	$V_{dc}=15V$ $N_{level}=49$ $N_{switch}=12$ $N_{IGBT}=16$ $N_{driver}=12$ $N_{source}=4$ $N_{variety}=4$ $V_{block}=1920V$	$V_{dc}=15V$ $N_{level}=49$ $N_{switch}=12$ $N_{IGBT}=16$ $N_{driver}=12$ $N_{source}=4$ $N_{variety}=4$ $V_{block}=1920V$	$V_{dc}=9V$ $N_{level}=81$ $N_{switch}=16$ $N_{IGBT}=16$ $N_{driver}=16$ $N_{source}=4$ $N_{variety}=4$ $V_{block}=1920V$
Minimum number of dc voltage sources in a constant number of output levels	$V_{dc}=9V$ $N_{level}=81$ $N_{switch}=16$ $N_{IGBT}=16$ $N_{driver}=16$ $N_{source}=4$ $N_{variety}=4$ $V_{block}=1440V$	$V_{dc}=9V$ $N_{level}=81$ $N_{switch}=16$ $N_{IGBT}=16$ $N_{driver}=16$ $N_{source}=4$ $N_{variety}=4$ $V_{block}=1440V$	$V_{dc}=9V$ $N_{level}=81$ $N_{switch}=16$ $N_{IGBT}=16$ $N_{driver}=16$ $N_{source}=4$ $N_{variety}=4$ $V_{block}=1440V$
Minimum amount of blocking voltage by switches in a constant number of output levels	$V_{dc}=9V$ $N_{level}=81$ $N_{switch}=16$ $N_{IGBT}=16$ $N_{driver}=16$ $N_{source}=4$ $N_{variety}=4$ $V_{block}=1440V$	$V_{dc}=9V$ $N_{level}=81$ $N_{switch}=16$ $N_{IGBT}=16$ $N_{driver}=16$ $N_{source}=4$ $N_{variety}=4$ $V_{block}=1440V$	$V_{dc}=9V$ $N_{level}=81$ $N_{switch}=16$ $N_{IGBT}=16$ $N_{driver}=16$ $N_{source}=4$ $N_{variety}=4$ $V_{block}=1440V$



(a) (b)

Fig. 9 Optimum structures; (a) based on minimum number of power switches in first and second algorithm; (b) based on minimum number of power switches in third algorithm and considering minimum number of dc voltage sources and minimum blocking voltage for three algorithms.

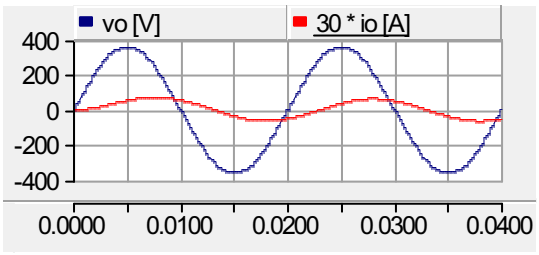
7 Simulation and Experimental Results

In order to investigate the theoretical issues and correct performance of the optimum topologies in generation all voltage levels (even and odd) at the output, the optimum structure based on minimum number of used power switches to generate a constant number of output levels by using second proposed algorithm is simulated and experimented. This simulation is done by EMTDC/PSCAD software program and practical prototype is made in the experimental environment. The aim is to design a 360V single-phase inverter with 49 levels at the output. According to (25), this inverter consists of two series connected units. Each unit includes of two dc voltage sources, two unidirectional switches and four bidirectional ones. It is important to note that the used IGBTs in the prototype are HGTP10N40CID (with an internal anti-parallel diode). The 89C52 microcontroller by ATMEL Company has been used to generate all switching pattern. As mentioned before and based on (23) and (25), the number of driver circuits is equal to the number of switches. By considering (30), in order to be able to generate maximum amplitude of 360V at the output, the magnitude of dc voltage source (V_{dc}) in the optimum topology has to consider 15 V. In all simulation and experimental studies the load is assumed as resistive-inductive load with $R = 100\Omega$ and $L = 440mH$. It is important to note that for measuring the output current, the voltage of a 0.1Ω resistor is used. This optimum structure is shown in Fig. 9(a).

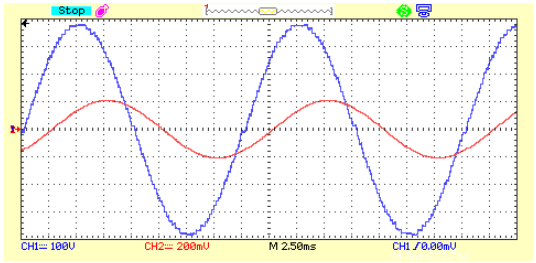
There are several control methods to control the multilevel inverters such as pulse with modulation (PWM), space vector modulation (SVM), selective harmonic elimination and fundamental frequency control method [22-25]. In this work, the fundamental

frequency switching method is used. This selection is because of low switching frequency that leads to less switching losses on switches in comparison with other control methods [26].

Fig. 10(a) shows the simulation output voltage and current waveforms. As it is obvious, this inverter is able to generate stepped waveform with maximum amplitude of 360V and 49 levels at the output. In addition, the current waveform is closer to ideal sinusoidal one than voltage waveform and consists of a phase shift in comparison to the voltage waveform. These differences are because of inductive-resistive load feature. The $R-L$ load acts as low pass filter. It is important to note that the output waveforms will be closer to ideal sinusoidal if the number of used units increase. In addition, Fig. 10(b) indicates the experimental results of the output voltage and current waveforms. As this figure shows, the experimental results reconfirm the simulation ones.



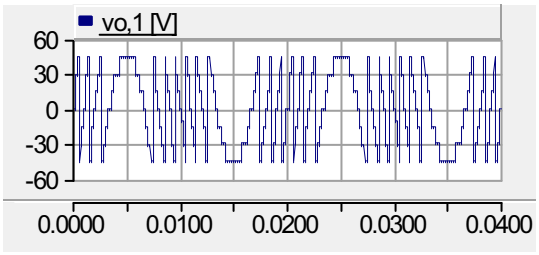
(a)



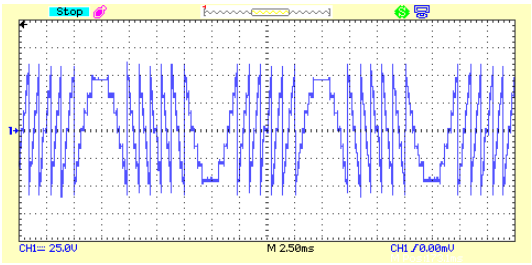
(b)

Fig. 10 Output voltage and current waveform for 49-level proposed optimum inverter; (a) Simulated results; (b) Experimental results.

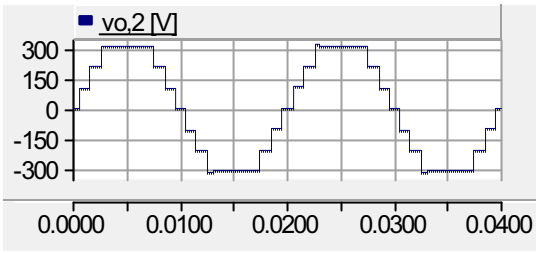
The simulation and experimental output voltage waveforms of each unit are shown in Fig. 11. As Fig. 11(a) shows, the first unit is able to generate voltage levels of 15V, 30V and 45V at the output. However, the second unit that is shown in Fig. 11(c) generates voltage levels of 105V, 210V and 315V at the output. It is clear that the output voltage waveform is equal to adding the output voltage levels of each unit. In addition, the experimental output voltage waveforms of each unit is completely corresponded by simulation ones. In the test condition, the efficiency is about 93.4%.



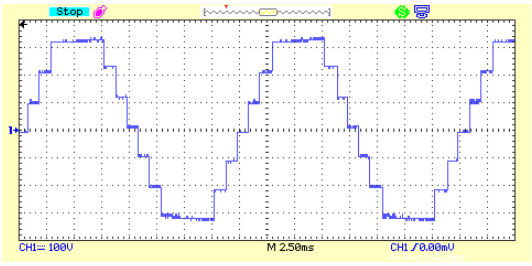
(a)



(b)



(c)

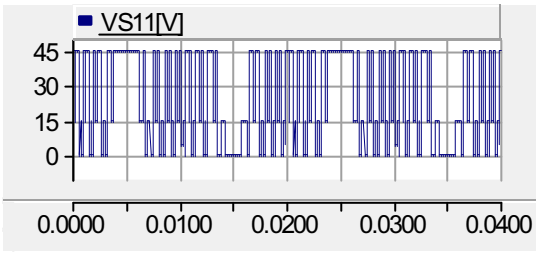


(d)

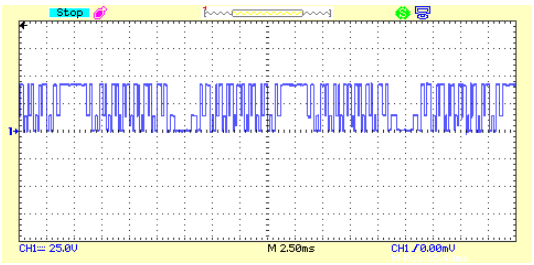
Fig. 11 Output voltage waveforms of each unit; (a) simulated result for first unit; (b) experimental result of first unit; (c) simulated result for second unit; (d) experimental result of second unit.

As mentioned before, the optimum strcuture consists of four bidirectional switch and two unidirectional ones from voltage point of view. In order to investigate these facts, the amount of blocked voltage by switches $S_{1,1}$ $S_{2,1}$, $S_{5,1}$ and $S_{6,1}$ of the first basic unit based on simulation results are shown in Figs. 12. 12(a), 12(c), 12(e) and 12(g), respectively. As shown in these figures, the magnitudes of the blocking voltage by switches $S_{1,1}$, $S_{2,1}$, $S_{5,1}$ and $S_{6,1}$ are either positive or zero and are equal to 45V, so, there is no negative values on them. Moreover, Figs. 12(b), 12(d), 12(f) and 12(h) are obtained from experimental prototype. These figures

also reconfirm the existence of four unidirectional power switches in the proposed optimum topology. Figs. 12(i) and 12(k) indicate the amount of blocked voltage by the switches $S_{3,1}$ and $S_{4,1}$, respectively. As shown in these figures, there are positive and negative amount of voltages with maximum magnitude of 30V on them. This fact verifies that the switches $S_{3,1}$ and $S_{4,1}$ are bidirectional ones. Figs. 12(j) and 12(l) are experimental waveforms of the blocked voltage by switches $S_{3,1}$ and $S_{4,1}$. These figures also show that these switches are bidirectional ones. Moreover, the amount of blocked voltage by the proposed optimum topology is equal to 1920V that is equal to add the magnitude of the blocked voltage by each switch in the first and second units.



(a)



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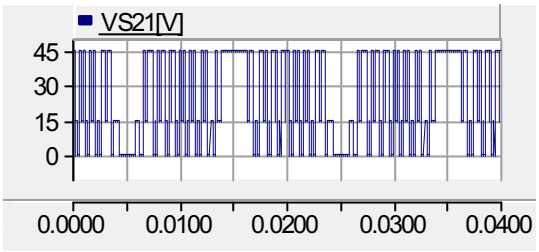

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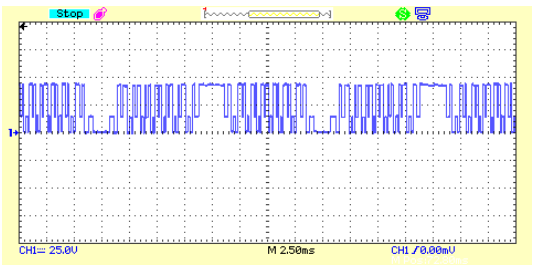

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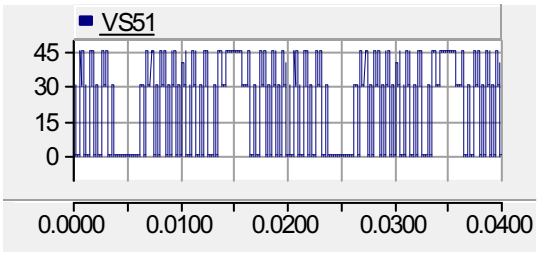

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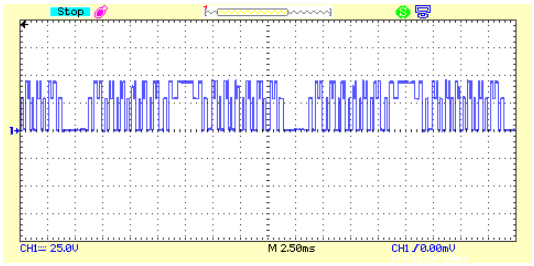
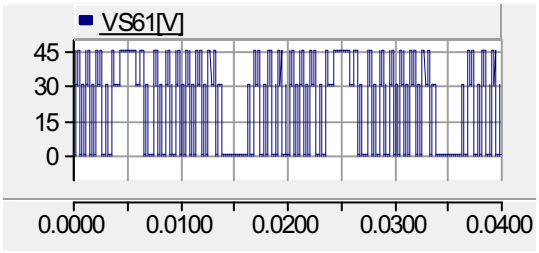


(f)



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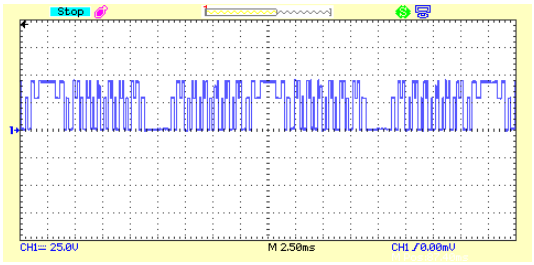
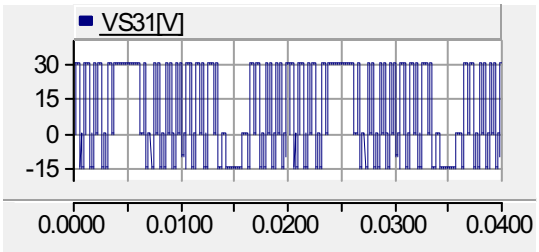
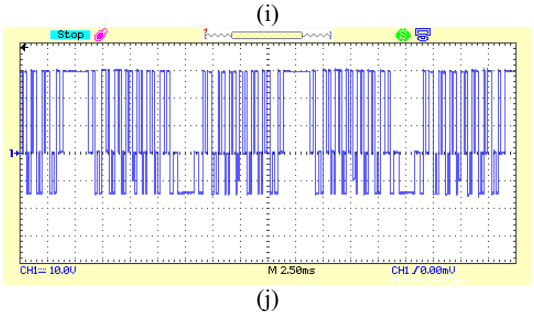


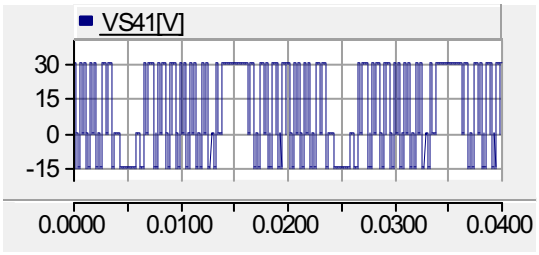
(h)



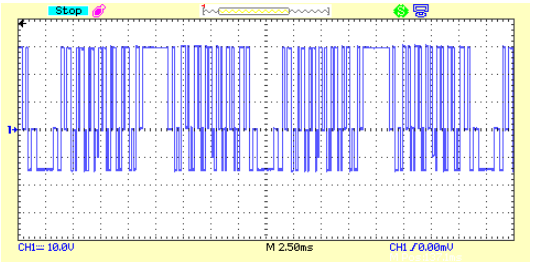
(i)



(j)



(k)



(l)

Fig. 12 Blocking voltages by the switches of the 49-level optimum inverter; (a) simulation result for $S_{1,1}$; (b) experimental result for $S_{1,1}$;(c) simulation result for $S_{2,1}$; (d) experimental result for $S_{2,1}$; (e) simulation result for $S_{5,1}$; (f) experimental result for $S_{5,1}$; (g) simulation result for $S_{6,1}$; (h) experimental result for $S_{6,1}$; (i) simulation result for $S_{3,1}$; (j) experimental result for $S_{3,1}$;(k) simulation result for $S_{4,1}$; (l) experimental result for $S_{4,1}$.

8 Conclusion

In this paper, a cascaded multilevel inverter with its algorithms that have been proposed in [13] and [15] are represented. Then, the optimum structures from minimum number of power switches or dc voltage sources or the minimum amount of blocked voltage by power switches in a constant number of output voltage levels are proposed. The proposed optimum topologies require lower number of power switches, dc voltage sources, the variability of the value of dc voltage sources and amount of blocked voltage by power switches than the H-bridge cascaded multilevel inverter and presented topologies in literature. Moreover, in order to investigate the ability of the proposed optimum topologies in generation all voltage levels a 49-level inverter with the magnitude of 360V at the output is designed. It is resulted that, the optimum structure by using the minimum number of power switches based on the third proposed algorithm is as same as the designed inverter by using the minimum number of used dc voltage sources and minimum amount of blocked voltage while all presented algorithms are used. This inverter needs four units with a dc voltage sources with a magnitude of 9V in each unit and therefore the number of required power electronic devices are equal to $N_{switch} = N_{IGBT} = N_{driver} = 4n = 16$, $N_{source} = N_{variety} = n = 4$ and $V_{block} = 1440\,V$. It is necessary to point out that by considering above design, 81 levels is generated at the output. In addition, the optimum topology from the minimum number of power switches in a constant number of output voltage levels based on first and second algorithm is same. At this condition, the designed optimum structure to generate 49-level inverter requires two units with two dc voltage source in each unit. The number of power electronic devices and the amount of blocked voltage are equal to $N_{switch} = 12$, $N_{IGBT} = 16$, $N_{driver} = 12$, $N_{source} = N_{variety} = 4$ and $V_{block} = 1920V$, respectively. Finally, the accuracy performance of the proposed optimum topology is verified through the PSCAD/EMTDC simulation and experimental results on a 49-level inverter.

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Sara Laali was born in Tehran, Iran in 1970. She received the B.S. degree in electronics engineering from Islamic Azad University, Tabriz Branch, and the M.S. degree in electrical engineering from Islamic Azad University, South Tehran Branch, Iran, in 2008 and 2010, respectively. She received her Ph.D. in Electrical Engineering from the Department of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran, in 2015. She has been joined to the Department of Electrical Engineering, Adiban Higher Education Institute from 2010 to 2015. In Oct 2015, she joined to Niroo Research Institute. Her major fields of interest include the analysis and control of power electronic converters, multilevel converters, and FACTS devices.

Ebrahim Babaei was born in Ahar, Iran, in 1970. He received the B.S. degree in Electronic Engineering and the M.S. degree in Electrical Engineering from the Department of Engineering, University of Tabriz, Tabriz, Iran, in 1992 and 2001, respectively, graduating with first class honors. He received the Ph.D. degree in Electrical Engineering from the Department of Electrical and Computer Engineering, University of Tabriz, in 2007.

In 2004, he joined the Faculty of Electrical and Computer Engineering, University of Tabriz. He was an Assistant Professor from 2007 to 2011, an Associate Professor from 2011 to 2015 and has been Professor since 2015. He is the author of more than 320 journal and conference papers. He also holds 17 patents in the area of power electronics. His current research interests include the analysis, modelling, design, and control of Power Electronic Converters (dc/dc; dc/ac; ac/ac; ac/dc; Matrix Converters; Multilevel Inverters; Z-Source Inverters; Resonance Converters; …) and their applications, Renewable Energy Sources, and FACTS Devices.

Prof. Babaei has been the Editor-in-Chief of the Journal of Electrical Engineering of the University of Tabriz, since 2013. He is also currently an Associate Editor of the IEEE Transactions on Industrial Electronics. He is a Guest Editor for a special issue on "Recent Advances in Multilevel Inverters and their Applications" in the IEEE Transactions on Industrial Electronics. In 2013, he was the recipient of the Best Researcher Award from of the University of Tabriz. Prof. Babaei has been included in the Top One Percent of the World's Scientists and Academics according to Thomson Reuters' list in 2015.

Zahra Saadatizadeh was born in Tabriz, Iran, in September 1991. She received her B.S. degree in Electrical Engineering from Azarbaijan Shahid Madani University, Tabriz, Iran, and the M.S. degree in Electrical Engineering from University of Tabriz, Tabriz, Iran, in 2013 and 2015, respectively.