A Grid Connected Transformerless Inverter and its Model Predictive Control Strategy with Leakage Current Elimination Capability


Abstract: This paper proposes a new single phase transformerless Photovoltaic (PV) inverter for grid connected systems. It consists of six power switches, two diodes, one capacitor and filter at the output stage. The neutral of the grid is directly connected to the negative terminal of the source. This results in constant common mode voltage and zero leakage current. Model Predictive Controller (MPC) technique is used to modulate the converter to reduce the output current ripple and filter requirements. The main advantages of this inverter are compact size, low cost, flexible grounding configuration. Due to brevity, the operating principle and analysis of the proposed circuit are presented in brief. Simulation and experimental results of 200W prototype are shown at the end to validate the proposed topology and concept. The results obtained clearly verifies the performance of the proposed inverter and its practical application for grid connected PV systems.

Keywords: Transformerless Two Stage Inverter, Switched Inductor, High Voltage Gain, Model Predictive Control, MPC.

1 Introduction

The price of PV panels is still too high, comparing with other renewable energy sources, so the grid connected PV inverters must be accurately designed to have low cost, low weight, high efficiency and small size [1]-[3]. The grid connected PV inverters can be classified into two, i.e. with and without transformer. The transformer provides a galvanic isolation between the PV panels and the grid, which includes high frequency transformer on the dc side of the inverter or a low frequency transformer on the grid side. Inverters with the low frequency transformers make the whole system bulky and costly, but inverters with the high frequency transformer reduce the system efficiency because of a several power stages [4]. In overall, inverter with transformer increases size, weight and cost of the grid connected power systems, reduce the efficiency but eliminate the leakage current. Thus, eliminating the transformer is a great benefit to improve the overall system efficiency, reduce the size, and weight [5-7]. Eliminating the leakage current is the main purpose of the transformerless grid connected inverters [8]-[9]. In [10] a modified FB is proposed, which decreases current ripple and improves efficiency but injects some dc current to the grid, which restricts performance of these inverters. The efficiency of the NPC inverter is improved compared with the FB inverter and the volume of the output filter are reduced due to its three level output voltage. However, this topology requires a doubled dc voltage input compared with the FB topologies. H5, H6 and HERIC inverters can operate with the unipolar SPWM strategy and need two filter inductors, which lead to a rise in the size and cost [11]. In multilevel neutral point clamped inverters, dc link capacitor midpoint is connected to the neutral line of the grid to reduce the leakage current. These inverters have high efficiency compared with the FB inverters but needs high dc bus voltage to feed the grid, which limits the voltage range of input dc sources [12-13].

This paper proposed a new transformerless topology to eliminate the leakage current of the grid connected PV systems using MPC technique. Compared to conventional topologies, this new inverter can be realized with minimal number of components (both active and passive). In addition, the neutral point of the grid and negative polarity of the PV are directly
connected, which effectively eliminates the leakage current. Further, it improves the power quality and reduces the filter requirements. The proposed inverter and analysis of topology are discussed briefly in Section 2 and 3 and validated with simulated and experimental results in Section 6 and conclusions with comparison in Section 7.

2 Leakage Current

One of the important issues in grid connected photovoltaic applications is leakage current problems. The leakage current flows through parasitic capacitance of the panel and causes personal safety problems, reduce the quality of injection current to the grid, and also decrease system losses [14]. In the transformerless grid connected inverters, full bridge (FB) inverter, neutral point clamped (NPC) inverter and many topologies with SPWM such as H5, H6 and HERIC were proposed to reduce the leakage current with disconnection of the grid from the PV during the freewheeling modes [15,16]. The Karschny inverter eliminates the leakage current by directly connecting the PV negative terminal with the neutral line of the grid [16]. The FB-based inverter with bipolar SPWM strategy can employ to generate a minimal leakage current, but the required output filter is large, which induces high current ripple, low system efficiency and reduces the power density. The path of the leakage current flowing through the parasitic capacitance ($C_{G-PV}$) in the grid connected transformerless inverter is shown in Fig. 1.

3 Description of the proposed topology

The proposed grid tied transformerless inverter is shown in Fig. 2. The proposed system consists of six switches ($S_1$- $S_6$), two capacitors ($C$ and $C_f$), two diodes ($D_1$ and $D_2$) and also two inductors ($L_1$ and $L_2$). The proposed grid connected single phase PV system consists of two main parts: primary stage and secondary stage. The primary stage consists of dc-dc converter that used to match the voltage level by stepping up the output voltage of the PV arrays to a required dc link voltage. The output of the primary stage is then connected to a dc link with an expected constant voltage. The secondary stage of the topology includes voltage source inverter to synthesize a desired voltage from dc source. As shown in Fig. 2, $V_d$ is an input dc voltage from the primary stage, $v_g$ and $i_g$ are grid voltage and current, respectively and $v_{AB}$ is inverter output voltage.

This topology utilizes the MPC method as modulation technique. The proposed inverter has three level output voltage (positive, zero and negative levels) which is shown in Fig. 3. According to the switching of the Sp and Sn, inverter output voltage ($v_{AB}$) will be $+V_d$ (positive state) or 0 (zero state), respectively in the positive cycle of the grid as shown in Fig. 4 and Fig. 5. In the positive cycle of the grid, switch $S_1$ always ON for the whole of this period and the switch $S_2$ will be ON and OFF with the switching frequency ($f_s$) to produce the high level voltage as shown in Fig. 4. In this cycle, when the switch $S_2$ is ON, the $D$ point connected to the ground and the switch $S_4$ operates with switching frequency in a boost mode. In this stage, diode $D_2$ is OFF and $D_1$ is turned ON and OFF, so the capacitor $C$ is charged through diode $D_1$ and the voltage across the capacitor $C$ maintains to be constant. In the period, when the switch $S_P$ is ON, $v_{AB}$ will be $+V_d$ and when the switch $S_N$ is ON, $v_{AB}$ will be 0. In the negative cycle of the grid, the switch $S_4$ always ON for the whole of this period and the switch $S_5$ will be ON and OFF with the switching frequency. In the negative cycle of the grid, when the switch $S_1$ is ON and the switch $S_6$ acts with the high frequency in a buck-boost mode and according to the switching of $S_N$ and $S_P$, $v_{AB}$ will be $-V_d$ (negative state) or 0 (zero state) respectively as shown in Fig. 5. In this stage, diode $D_1$ is OFF and $D_2$ is turned ON and OFF. In this period, when the switch $S_N$ is ON, $v_{AB}$ will be $-V_d$ and when the switches $S_P$ is ON, $v_{AB}$ will be 0. The proposed inverter is capable to deliver reactive power. In this condition the sequences for the output voltage and current of the proposed inverter are shown in the Fig. 6. Fig. 6 and Fig. 7 show the equivalent circuit in the negative voltage levels that...
Three interval, the switch is less than the injected current. The voltage and current waveforms of the inductor in DCM is shown in Fig. 9.

$$V_L = V_{PV} - V_d \frac{d}{2}$$

Also, when the switch S2 is turned on, the diodes D1 and D2 are on and the inductors L1 and L2 are charged in parallel by the input voltage VPV. The equation is:

$$V_{L1} = V_{L2} = V_{PV}$$

During the switching period \(T_S\), the average voltage across inductors \(L_1\) and \(L_2\) are obtained as follows:

$$\langle V_{L1} \rangle = \langle V_{L2} \rangle = \frac{V_{PV}}{2}$$

In Fig. 4, the equivalent circuit of the CCM in negative cycle of the grid is shown. In this interval, the switch \(S_2\) is always turned ON and the switch \(S_1\) is in both ON and OFF state. During \(S_1\) off period, the diode \(D_3\) is on and the inductors are series. Therefore, voltage across each inductor during this interval is:

$$V_L = \frac{-V_d}{2}$$

Also, when the switch \(S_1\) is ON, the diode \(D_1\) will be reverse-biased. The voltage across inductors will be:

$$V_{L1} = V_{L2} = V_{PV}$$

The voltage across each inductor with voltage balance is:

$$\langle V_{L1} \rangle = \langle V_{L2} \rangle = d_1 \left( \frac{V_{PV}}{2} + V_{PV} \right) - \frac{V_d}{2}$$

In the equation (6), \(d_1\) is the duty cycle of \(S_1\) at the primary stage. The voltage gain of the proposed converter in CCM is found as:

$$G_{CCM} = \frac{V_{PV}}{V_{m}} = \frac{2d_1 + d_3 + 1}{2 - d_1 - d_3}$$

4.2 DCM analysis of the proposed topology

In DCM, the inductor current equals zero during a time interval and is more than zero during another time interval. During a time interval, the inductor current is less than the injected current. The voltage and current waveforms of the inductor in DCM is shown in Fig. 9.
A cost function is used to calculate the switching state must be activated to reduce the current. In the negative cycle of the grid, if $i_{ref} > i_{s}$, negative mode switching must be activated to reduce the current. Otherwise zero switching states (zero, positive or negative) applied during $0 < t < T/2$. The selected optimal associated voltage level with the least error for current state with minimizing the function model [17].

The voltage gain of proposed inverter in DCM state will be as follows:

$$M_{V,DCM}(d_2, d_1) = \frac{V_d}{V_m} = \frac{1 + d_{21} + d_{22} + d_{12}}{d_{12} + d_{22} - 1}$$

(9)

4.3 BCM analysis of the proposed topology

As shown in Fig. 10, $I_{L_{min}} = 0$ should be valid to obtain the critical inductance between DCM and BCM. Primary stage of the proposed topology is combined with a boost and buck boost converter. Since boost converter reaches DCM faster than the buck boost converter, so the BCM is restricted with the boost converter. The critical inductance of the proposed topology is similar with the boost converter. In this state, the waveforms of current and voltage of the inductor is indicated in Fig. 10. As shown in this figure, the minimum value of inductor current will be zero. By applying voltage second law for the inductor using the combination of DCM mode during $0 < t < T/2$ and BCM mode during $T/2 < t < T$, we have:

$$\dot{V}_L = DT (V_m d_{11} + (V_m - V_d) d_{21}) + (1 - D) T (V_m d_2 - V_d (1 - d_2)) = 0$$

(10)

From (9), the voltage gain of proposed topology in this state will be:

$$M_{V,BCM}(d_1, d_2) = \frac{V_d}{V_m} = \frac{d_{11} + d_{21} + d_2 + 1}{d_{21} + d_{22}}$$

(11)

5 MPC strategy for the proposed topology

In this paper, the predictive current controller is designed to regulate the injected current to the grid based on the reference current. The control action on each sampling interval is obtained by measuring the current state with minimizing the function model [17]. In this paper, the MPC technique is used to control the switches $S_1$, $S_2$, $S_3$, and $S_4$. The selected optimal switching state (zero, positive or negative states) applied to the topology during the next sampling interval to minimize the cost function. The voltage across capacitor controlled in primary stage with this method. Also, the secondary stage of the topology controls the injected current to the grid. A cost function is used to calculate the voltage state of the next sampling interval based on the predicted behavior. The equivalent circuit and operation modes of the proposed topology at the secondary stage are shown in Fig. 11. According to the Fig. 11, with comparison of the reference current with the actual current, some switches will be on considering associated voltage level with the least error for current variations. In first operating mode, in the positive cycle of the grid, if $i_{ref} < i_t$, positive mode switching must be activated to increases current. Otherwise zero switching state must be activated to reduce the current. In the negative cycle of grid, if $i_{ref} > i_t$, negative mode...
switching must be activated to increases the current in the opposite direction. Otherwise zero switching state must be activated.

According to Fig. 11(a), which labeled as \( P=1 \), for inductor voltage \( (L_L) \), we have:

\[
\frac{di_L}{dt} = \frac{di_s}{dt} = \frac{v_s}{L_L}
\]

(12)

With discretizing of the time-continuous relation (11) for sampling time of \( T_s \), it can be written as follows:

\[
i_s(k+1) = i_s(k) + \frac{T}{L_f} V_d(k) - \frac{v_s(k)}{L_f} T
\]

(13)

Also, according to Fig. 11(b) which labeled as \( Z=1 \), for inductor voltage \( (L_L) \), we have:

\[
\frac{di_L}{dt} = \frac{di_s}{dt} = \frac{v_s}{L_L}
\]

(14)

With discretizing of time-continuous relation (13) for sampling time of \( T_s \), it is clear that:

\[
i_s(k+1) = i_s(k) + \frac{T}{L_f} V_d(k)
\]

(15)

Moreover, according to Fig. 11(c), which labeled as \( (L=1) \), for inductor voltage \( (L_L) \), it can be write:

\[
\frac{di_L}{dt} = \frac{di_s}{dt} = -\frac{v_s}{L_L} - \frac{v_s}{L_f}
\]

(16)

Discretizing of time-continuous relation 16, for sampling time of \( T_s \), results:

\[
i_s(k+1) = i_s(k) - \frac{T}{L_f} V_d(k) - \frac{T}{L_f} v_s(k)
\]

(17)

Converter time-discrete equations for relations (12-17) can be summarized as follows:

\[
i_s(k+1)_{Z,P,N} = i_s(k) + P \frac{T}{L_f} (V_d(k) - v_s(k)) - N \frac{T}{L_f} (v_s(k)) + Z \frac{T}{L_f} (v_s(k))
\]

(18)

Fig. 11 Equivalent circuits of the secondary stage of the proposed topology.

Table 1 Simulation parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated power</td>
<td>( P_{out} )</td>
<td>1000 W</td>
</tr>
<tr>
<td>Input voltage</td>
<td>( V_{in} )</td>
<td>50 V</td>
</tr>
<tr>
<td>Switching and sampling frequency</td>
<td>( f_{sw} )</td>
<td>20 kHz</td>
</tr>
<tr>
<td>Filter inductor</td>
<td>( L_f )</td>
<td>1 mH</td>
</tr>
<tr>
<td>PV parasitic capacitor</td>
<td>( C_{PV} )</td>
<td>0.1 mF</td>
</tr>
<tr>
<td>Ground resistance</td>
<td>( R_g )</td>
<td>3 Ω</td>
</tr>
<tr>
<td>DC bus capacitor</td>
<td>( C_{bus} )</td>
<td>940 μF</td>
</tr>
<tr>
<td>Topology inductor</td>
<td>( L )</td>
<td>10 mH</td>
</tr>
</tbody>
</table>

According to relations (15,17), in next sampling instant \( k+1 \), the control variable \( i_s \) can be predicted through \( k^{th} \) instant of current \( i_s \). According to (19), defined cost function \( J \) in \( k^{th} \) instant, determine switching states for the least value of that for various states.

\[
J^1_{Z=0.1, P=0.1, N=0.1} = W \left| i_s(k+1)_{Z,P,N} - i_{ref} \right|^2
\]

(19)

6 Experimental and simulation verifications

Using the PSCAD software, simulation results of the proposed inverter are shown in Fig. 12(a) and Fig. 12(b). The selected parameters of the simulations are listed in Table 1. A resistor and a capacitor are connected in series to simulate the parasitic effect of the PV panel and they connected between the ground and the input source. A sinusoidal current is injected to the grid. Fig. 10(a) shows the sinusoidal injected current with small ripple. The output current waveform in comparison with a reference waveform is presented in Fig. 12(a). The response of MPC is very fast for the following reference current. The blue curve shows the output current, and the green curve shows the reference current. It is clear that the output current is highly sinusoidal with low harmonic distortion due to the three level output voltage. The partial enlargement of the injection current and three level output voltage are provided in Fig. 12 (c) and Fig. 12 (d).

The experimental results of the proposed inverter is provided with unity power factor for the pure resistive load in order to verify the feasibility of the proposed topology. A photograph of the proposed transformerless inverter prototype is depicted in Fig. 13. The specifications of the prototype are listed in Table 2. Fig. 14 and Fig. 15 show the experimental waveforms of the proposed topology. The experimental results for the
output voltage and the output current are shown in Fig. 14. The voltage of dc link and input voltage are shown in Fig. 15. As shown in Fig. 14, the output voltage has three levels as $V_d$, 0, and $-V_d$, so a good differential mode characteristic has been achieved. As it can be seen in Fig. 14, it is clear that the output current and voltage of the proposed inverter are highly sinusoidal due to the three-level inherency of the output voltage. The RMS value of the current is equal to 2A, and the output power is 200 W. In Fig. 16 amplitudes of harmonics and fundamental component and THD of output voltage and current are shown. THD amplitude of voltage and current are about 2% and 5% for three level proposed inverter.

Fig. 12 Simulation results of the topology (a) injection current (b) voltage of inductor (c) enlarged of injection current (d) enlarged of output voltage.

**Table 2** Experimental parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>$V_{in}$</td>
<td>100 V</td>
</tr>
<tr>
<td>Load Resistance (R)</td>
<td>$R_l$</td>
<td>50 Ω</td>
</tr>
<tr>
<td>Load Inductance (L)</td>
<td>$L_l$</td>
<td>30 mH</td>
</tr>
<tr>
<td>DC bus capacitor</td>
<td>$C_{dc}$</td>
<td>940 uF</td>
</tr>
<tr>
<td>Topology Inductor</td>
<td>$L$</td>
<td>10 mH</td>
</tr>
</tbody>
</table>

Fig. 13 Photograph of a prototype.

Fig. 14 Experimental waveforms of the proposed topology. (a) output current ($i_{out}$) [2.5 A/div] and output voltage ($v_{Bn}$) [100V/div] (b) output current ($i_{out}$) [1 A/div], time [2ms/div].

7 Comparison of the structures with the other topologies

Table 3 shows comparison of the transformerless inverter structures with respect to number of semiconductor devices and passive elements. The proposed inverter has fewer semiconductors and passive elements than the other topologies. A comparison of the RMS leakage current, THD of the inverter output voltage and efficiency of the different PV inverter topologies with the proposed topology are accomplished in Table 3. The considered converters were H5, HERIC, ANPC, H6, [20], [21] and [22]. The THD of generated
inverter output voltage is 2.5%, which confirms high quality of produced output voltage. The magnitude of the leakage current $i_{\text{leakage}}$, for these topologies is shown in Fig. 15. All these topologies have a very low leakage current. As shown in Fig. 17(a), the proposed topology in [20] has the biggest leakage current, compared with the other topologies as illustrated in Fig. 17(b) and Fig. 17(c).

### Table 3: Comparison of the proposed converter with other topology.

<table>
<thead>
<tr>
<th>Converter</th>
<th>Diodes</th>
<th>Switches</th>
<th>$C_f$</th>
<th>$L_f$</th>
<th>Efficiency, %</th>
<th>THD (%)</th>
<th>$i_{\text{leakage}}$(mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>H5</td>
<td>0</td>
<td>5</td>
<td>1</td>
<td>3</td>
<td>96.32</td>
<td>2</td>
<td>80</td>
</tr>
<tr>
<td>HERIC</td>
<td>0</td>
<td>6</td>
<td>1</td>
<td>3</td>
<td>95.7</td>
<td>1.9</td>
<td>95</td>
</tr>
<tr>
<td>ANPC [18]</td>
<td>0</td>
<td>6</td>
<td>2</td>
<td>2</td>
<td>96.45</td>
<td>1.8</td>
<td>70</td>
</tr>
<tr>
<td>H6 [19]</td>
<td>2</td>
<td>6</td>
<td>2</td>
<td>2</td>
<td>97.6</td>
<td>1.4</td>
<td>85</td>
</tr>
<tr>
<td>[20]</td>
<td>3</td>
<td>7</td>
<td>3</td>
<td>3</td>
<td>95.2</td>
<td>4.8</td>
<td>100</td>
</tr>
<tr>
<td>[21]</td>
<td>0</td>
<td>6</td>
<td>2</td>
<td>3</td>
<td>92.77</td>
<td>4</td>
<td>90</td>
</tr>
<tr>
<td>[22]</td>
<td>2</td>
<td>7</td>
<td>3</td>
<td>3</td>
<td>96</td>
<td>2.5</td>
<td>20</td>
</tr>
<tr>
<td>Proposed</td>
<td>2</td>
<td>6</td>
<td>1</td>
<td>2</td>
<td>95.12</td>
<td>2.5</td>
<td>$1.5\times10^{-5}$</td>
</tr>
</tbody>
</table>

## 8 Conclusion

A novel transformerless inverter has been proposed in this paper for single phase grid connected PV system. The leakage current is eliminated due to the common ground. In addition, the inverter can be realized with minimal number of components; hence higher power density can be achieved at lower design cost. This
topology generates a three level voltage has low core losses of the output filter at its output terminals with high voltage gain. The negative terminal of the proposed inverter is directly connected to the ground, hence the leakage current is well suppressed with only one filter inductor unlike other topologies. Compared to the other existing transformerless two stage topologies, dc input voltage can be lower than the grid voltage. Compared with other existing transformerless topologies, performance demonstrated by the proposed inverter are presently unmatched, as quantified through detailed theoretical and comparative analysis supported by simulation and experimental results.

References
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Prof. Babaei has been the Editor-in-Chief of the Journal of Electrical Engineering of the University of Tabriz, since 2013. He is also currently an Associate Editor of the IEEE Transactions on Industrial Electronics. He is a Guest Editor for a special issue on “Recent Advances in Multilevel Inverters and their Applications” in the IEEE Transactions on Industrial Electronics. In 2013, he was the recipient of the Best Researcher Award from of the University of Tabriz. Prof. Babaei has been included in the Top One Percent of the World’s Scientists and Academics according to Thomson Reuters' list in 2015.

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