A Grid Connected Transformerless Inverter and its Model Predictive Control Strategy with Leakage Current Elimination Capability

J. F. Ardashir*, M. Sabahi *(C.A.), S. H. Hosseini* , E. Babaei* and G. B. Gharehpetian**

Abstract: This paper proposes a new single phase transformerless Photovoltaic (PV) inverter for grid connected systems. It consists of six power switches, two diodes, one capacitor and filter at the output stage. The neutral of the grid is directly connected to the negative terminal of the source. This results in constant common mode voltage and zero leakage current. Model Predictive Controller (MPC) technique is used to modulate the converter to reduce the output current ripple and filter requirements. The main advantages of this inverter are compact size, low cost, flexible grounding configuration. Due to brevity, the operating principle and analysis of the proposed circuit are presented in brief. Simulation and experimental results of 200W prototype are shown at the end to validate the proposed topology and concept. The results obtained clearly verifies the performance of the proposed inverter and its practical application for grid connected PV systems.

Keywords: Transformerless Two Stage Inverter, Switched Inductor, High Voltage Gain, Model Predictive Control, MPC.

1 Introduction

THE price of PV panels is still too high, comparing with other renewable energy sources, so the grid connected PV inverters must be accurately designed to have low cost, low weight, high efficiency and small size [1]-[3]. The grid connected PV inverters can be classified into two, i.e. with and without transformer. The transformer provides a galvanic isolation between the PV panels and the grid, which includes high frequency transformer on the dc side of the inverter or a low frequency transformer on the grid side. Inverters with the low frequency transformers make the whole system bulky and costly, but inverters with the high frequency transformer reduce the system efficiency because of a several power stages [4]. In overall, inverter with transformer increases size; weight and cost of the grid connected power systems, reduce the efficiency but eliminate the leakage current. Thus, eliminating the transformer is a great benefit to improve the overall system efficiency, reduce the size, and weight [5-7]. Eliminating the leakage current is the main purpose of the transformerless grid connected inverters [8]-[9]. In [10] a modified FB is proposed, which decreases current ripple and improves efficiency but injects some dc current to the grid, which restricts performance of these inverters. The efficiency of the NPC inverter is improved compared with the FB inverter and the volume of the output filter are reduced due to its three level output voltage. However, this topology requires a doubled dc voltage input compared with the FB topologies. H5, H6 and HERIC inverters can operate with the unipolar SPWM strategy and need two filter inductors, which lead to a rise in the size and cost [11]. In multilevel neutral point clamped inverters, dc link capacitor midpoint is connected to the neutral line of the grid to reduce the leakage current. These inverters have high efficiency compared with the FB inverters but needs high dc bus voltage to feed the grid, which limits the voltage range of input dc sources [12-13].

This paper proposed a new transformerless topology to eliminate the leakage current of the grid connected PV systems using MPC technique. Compared to conventional topologies, this new inverter can be realized with minimal number of components (both active and passive). In addition, the neutral point of the grid and negative polarity of the PV are directly

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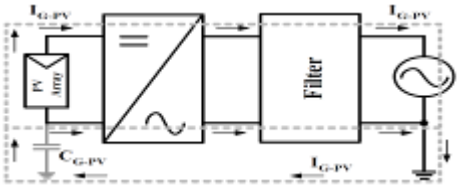


Fig. 1 Transformerless inverter with a leakage current path.

connected, which effectively eliminates the leakage current. Further, it improves the power quality and reduces the filter requirements. The proposed inverter and analysis of topology are discussed briefly in Section 2 and 3 and validated with simulated and experimental results in Section 6 and conclusions with comparison in Section 7.

2 Leakage Current

One of the important issues in grid connected photovoltaic applications is leakage current problems. The leakage current flows through parasitic capacitance of the panel and causes personal safety problems, reduce the quality of injection current to the grid, and also decrease system losses [14]. In the transformerless grid connected inverters, full bridge (FB) inverter, neutral point clamped (NPC) inverter and many topologies with SPWM such as H5, H6 and HERIC were proposed to reduce the leakage current with disconnection of the grid from the PV during the freewheeling modes [15,16]. The Karschny inverter eliminates the leakage current with directly connecting the PV negative terminal with the neutral line of the grid [16]. The FB-based inverter with bipolar SPWM strategy can employ to generate a minimal leakage current, but the required output filter is large, which induces high current ripple, low system efficiency and reduces the power density. The path of the leakage current flowing through the parasitic capacitance ($C_{G\text{-}PV}$) in the grid connected transformerless inverter is shown in Fig. 1.

3 Description of the proposed topology

The proposed grid tied transformerless inverter is shown in Fig. 2. The proposed system consists of six switches (S_1- S_6), two capacitors (C and C_f), two diodes (D_1 and D_2) and also two inductors (L_1 and L_2). The proposed grid connected single phase PV system consists of two main parts: primary stage and secondary stage. The primary stage consists of dc-dc converter that used to match the voltage level by stepping up the output voltage of the PV arrays to a required dc link voltage. The output of the primary stage is then connected to a dc link with an expected constant voltage. The secondary stage of the topology includes voltage source inverter to synthesize a desired voltage from dc source. As shown in Fig. 2, V_d is an input dc voltage from the primary stage, v_g and i_g are grid voltage and current, respectively and v_{AB} is inverter output voltage.

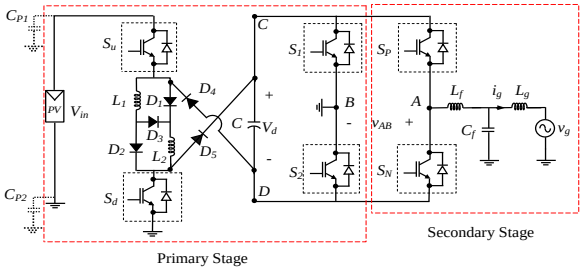


Fig. 2 Circuit configuration of the proposed transformerless negative grounding PV system.

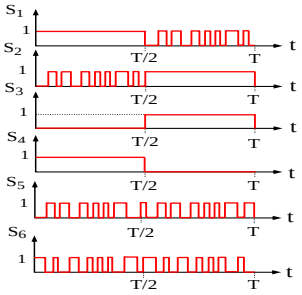


Fig. 3 Switching pulses of the proposed inverter.

voltage.

This topology utilizes the MPC method as modulation technique. The proposed inverter has three level output voltage (positive, zero and negative levels) which is shown in Fig. 3. According to the switching of the Sp and SN, inverter output voltage (vAB) will be +Vd (positive state) or 0 (zero state), respectively in the positive cycle of the grid as shown in Fig. 4 and Fig . 5.

In the positive cycle of the grid, switch S_u always ON for the whole of this period and the switch S_d will be ON and OFF with the switching frequency (f_s) to produce the high level voltage as shown in Fig. 4. In this cycle, when the switch S_2 is ON, the D point connected to the ground and the switch S_d operates with switching frequency in a boost mode. In this stage, diode D_2 is OFF and D_1 is turned ON and OFF, so the capacitor C is charged through diode D_1 and the voltage across the capacitor C maintains to be constant. In this period, when the switch S_P is ON, v_{AB} will be $+V_d$ and when the switch S_N is ON, v_{AB} will be 0. In the negative cycle of the grid, the switch S_d always ON for the whole of this period and the switch S_u will be ON and OFF with the switching frequency. In the negative cycle of the grid, when the switch S_1 is ON and the switch S_u acts with the high frequency in a buck-boost mode and according to the switching of S_N and S_p, v_{AB} will be $-V_d$ (negative state) or 0 (zero state) respectively as shown in Fig. 5. In this stage, diode D_1 is OFF and D_2 is turned ON and OFF. In this period, when the switch S_N is on, v_{AB} will be $-V_d$ and when the switches S_P is ON, v_{AB} will be 0. The proposed inverter is capable to deliver reactive power. In this condition the sequences for the output voltage and current of the proposed inverter are shown in the Fig. 6. Fig. 6 and Fig. 7 show the equivalent circuit in the negative voltage levels that

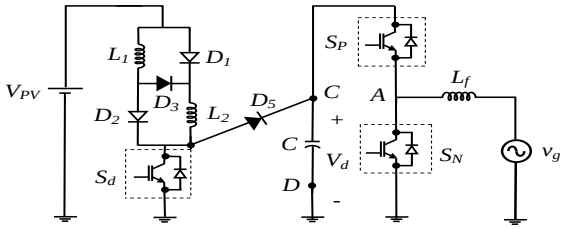


Fig. 4 Equivalent circuit of the proposed inverter in the positive cycle of the grid.

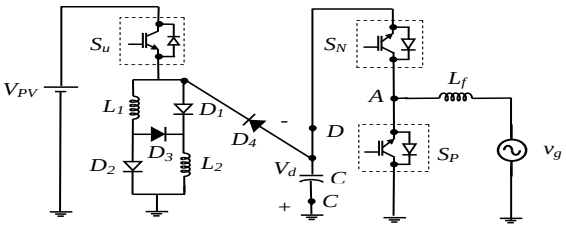


Fig. 5 Equivalent circuit of the proposed inverter in the negative cycle of the grid.

diodes of S_P and S_N are on and the voltage across the capacitor C appears at the inverter output voltage (positive and negative state).

4 Steady state analysis of the primary stage

The primary stage of the proposed inverter has three operation modes which are named continues conduction mode (CCM), discontinuous conduction mode (DCM) and boundary conduction mode (BCM).

4.1 CCM analysis of the proposed topology

The steady state waveforms of current and voltage inductor during CCM with frequency $f = 1/T$ are shown in Fig. 8. It is notable that T is the period of the grid. In this figure, I_1 is minimum inductor current and I_2 is the maximum inductor current. The inductor is able to charge the capacitor along with injected current provision due to high inductor current. In the positive cycle, the switch S_u is operated with high frequency. As shown in Fig. 4, during the switching S_2 off period, the diode D_3 is on and the inductors are series. The inductors L_1 and L_2 releases energy to capacitor C through diode D_5. Therefore, the expression is:

$$V_L = \frac{V_{PV} - V_d}{2} \tag{1}$$

Also, when the switch S2 is turned on, the diodes D_1 and D_2 are on and the inductors L_1 and L_2 are charged in parallel by the input voltage VPV. The equation is:

$$V_{L1} = V_{L2} = V_{PV} \tag{2}$$

During the switching period (T_s), the average voltage across inductors L_1 and L_2 are obtained as follows:

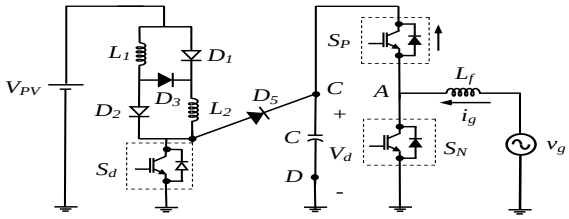


Fig. 6 The operational stages of the proposed inverter during output voltage positive and output current negative.

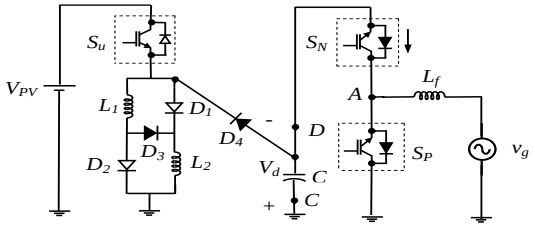


Fig. 7 The operational stages of the proposed inverter during output voltage negative and output current negative.

$$\langle V_{L1} \rangle = \langle V_{L2} \rangle = \frac{V_d}{2}(d_2 - 1) + \frac{V_{PV}}{2}(d_2 + 1) \tag{3}$$

In Fig. 4, the equivalent circuit of the CCM in negative cycle of the grid is shown. In this interval, the switch S_2 is always turned ON and the switch S_1 is in both ON and OFF state. During S_1 off period, the diode D_3 is on and the inductors are series. Therefore, voltage across each inductor during this interval is:

$$V_L = \frac{-V_d}{2} \tag{4}$$

Also, when the switch S_1 is ON, the diode D_4 will be reverse-biased. The voltage across inductors will be:

$$V_{L1} = V_{L2} = V_{PV} \tag{5}$$

The voltage across each inductor with voltage balance is:

$$\langle V_{L1} \rangle = \langle V_{L2} \rangle = d_1\left(\frac{V_d}{2} + V_{PV}\right) - \frac{V_d}{2} \tag{6}$$

In the equation (6), d_1 is the duty cycle of S_1 at the primary stage. The voltage gain of the proposed converter in CCM is found as:

$$G_{CCM} = \frac{V_O}{V_{in}} = \frac{2d_1 + d_2 + 1}{2 - d_1 - d_2} \tag{7}$$

4.2 DCM analysis of the proposed topology

In DCM, the inductor current equals zero during a time interval and is more than zero during another time interval. During a time interval, the inductor current is less than the injected current. The voltage and current waveforms of the inductor in DCM is shown in Fig. 9.

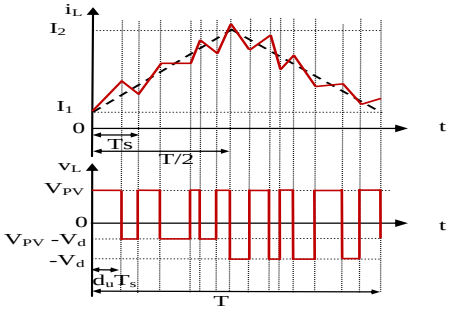


Fig. 8 Current and voltage waveforms of the inductor L in CCM.

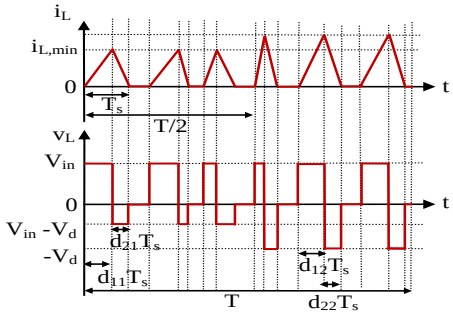


Fig. 9 Current and voltage waveforms of the inductor L in DCM.

As indicated in this figure, the inductor is being charged during $d_{11}T_s$ and the inductor will be discharged during $d_{21}T_s$. Also, during $(1\text{-}d_{11}\text{-}d_{21})T_s$ the inductor current will be zero. In this interval, the stored energy by the inductor L is lower than stored energy during $T/2<t<T$. It causes the current of inductor L during $0<t<T/2$ reaches to the zero faster than the interval $T/2<t<T$. Using volt second law across the voltage inductor L in one period, we have:

$$\langle V_L \rangle = DT\,(V_{in}\,d_{11} + (V_{in} - V_d)\,d_{21}) + (1-D)\,T\,(V_{in}\,d_{12} - V_2\,d_{22}) = 0 \tag{8}$$

in which d_{11} and d_{21} are duty cycles of the switches S_d and S_u in the positive and negative cycle of the grid, respectively. The inductor and capacitor provide the injected current together in this stage.
The voltage gain of proposed inverter in DCM state will be as follows:

$$M_{V-DCM}(d_1, d_2) = \frac{V_d}{V_{in}} = \frac{1 + d_{21} + d_{22} + d_{12}}{d_{12} + d_{22} - 1} \tag{9}$$

4.3 BCM analysis of the proposed topology

As shown in Fig. 10, $I_{L,min} = 0$ should be valid to obtain the critical inductance between DCM and CCM. Primary stage of the proposed topology is combined with a boost and buck boost converter. Since boost converter reaches DCM faster than the buck boost converter, so the BCM is restricted with the boost converter. The critical inductance of the proposed

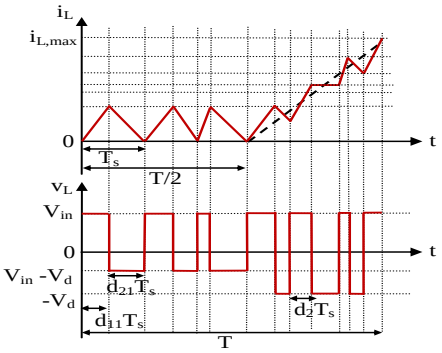


Fig. 10 Current and voltage waveforms of the inductor L in BCM.

topology is similar with the boost converter. In this state, the waveforms of current and voltage of the inductor is indicated in Fig. 10. As shown in this figure, the minimum value of inductor current will be zero. By applying voltage second law for the inductor using the combination of DCM mode during $0<t<T/2$ and CCM mode during $T/2<t<T$, we have:

$$\langle V_L \rangle = DT\,(V_{in}\,d_{11} + (V_{in} - V_d)\,d_{21}) + (1-D)\,T\,(V_{in}\,d_2 - V_2(1-d_2)) = 0 \tag{10}$$

From (9), the voltage gain of proposed topology in this state will be:

$$M_{V-BCM}(d_1, d_2) = \frac{V_d}{V_{in}} = \frac{d_{11} + d_{21} + d_2 + 1}{d_{21} + d_{11}} \tag{11}$$

5 MPC strategy for the proposed topology

In this paper, the predictive current controller is designed to regulate the injected current to the grid based on the reference current. The control action on each sampling interval is obtained by measuring the current state with minimizing the function model [17]. In this paper, the MPC technique is used to control the switches S_1, S_2, S_3 and S_4. The selected optimal switching state (zero, positive or negative states) applied to the topology during the next sampling interval to minimize the cost function. The voltage across capacitor controlled in primary stage with this method. Also, the secondary stage of the topology controls the injected current to the grid. A cost function is used to calculate the voltage state of the next sampling interval based on the predicted behavior. The equivalent circuit and operation modes of the proposed topology at the secondary stage are shown in Fig. 11. According to the Fig. 11, with comparison of the reference current with the actual current, some switches will be on considering associated voltage level with the least error for current variations. In first operating mode, in the positive cycle of the grid, if $i_{ref} < i_s$, positive mode switching must be activated to increases current. Otherwise zero switching state must be activated to reduce the current. In the negative cycle of grid, if $i_{ref} > i_s$, negative mode

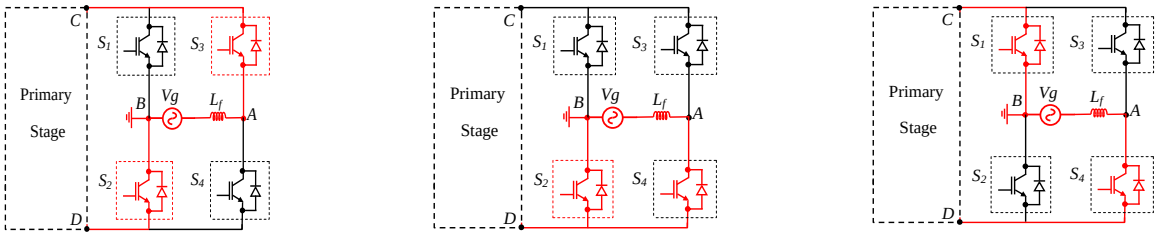


Fig. 11 Equivalent circuits of the secondary stage of the proposed topology.

switching must be activated to increases the current in the opposite direction. Otherwise zero switching state must be activated.

According to Fig. 11(a), which labeled as (P=1), for inductor voltage (L_f), we have:

$$\frac{di_{Lf}}{dt}=\frac{di_s}{dt}=\frac{V_d}{L_f}-\frac{v_g}{L_f} \tag{12}$$

With discretizing of the time-continuous relation (11) for sampling time of T_s, it can be written as follows:

$$i_s(\mathrm{k+1})=\mathrm{i}_s(\mathrm{k})+\frac{T_s}{L_f}V_d(\mathrm{k})-\frac{v_g(\mathrm{k})}{L_f}T_s \tag{13}$$

Also, according to Fig. 11(b) which labeled as (Z=1), for inductor voltage (L_f), we have:

$$\frac{di_{Lf}}{dt}=\frac{di_s}{dt}=\frac{v_g}{L_f} \tag{14}$$

With discretizing of time-continuous relation (13) for sampling time of T_s, it is clear that:

$$i_s(\mathrm{k+1})=\mathrm{i}_s(\mathrm{k})+\frac{T_s}{L_f}V_d(\mathrm{k}) \tag{15}$$

Moreover, according to Fig. 11(c), which labeled as (L=1), for inductor voltage (L_f), it can be write:

$$\frac{di_{Lf}}{dt}=\frac{di_s}{dt}=-\frac{V_d}{L_f}-\frac{v_g}{L_f} \tag{16}$$

Discretizing of time-continuous relation 16, for sampling time of T_s, results:

$$i_s(\mathrm{k+1})=\mathrm{i}_s(\mathrm{k})-\frac{T_s}{L_f}V_d(\mathrm{k})-\frac{T_s}{L_f}v_g(\mathrm{k}) \tag{17}$$

Converter time-discrete equations for relations (12-17) can be summarized as follows:

$$i_s(\mathrm{k+1})_{Z,P,N}=\mathrm{i}_s(\mathrm{k})+P\frac{T_s}{L_f}\left(V_d(\mathrm{k})-\mathrm{v}_g(\mathrm{k})\right)-\mathrm{N}\frac{T_s}{L_f}\left(V_d(\mathrm{k})+\mathrm{v}_g(\mathrm{k})\right)+Z\frac{T_s}{L_f}\left(\mathrm{v}_g(\mathrm{k})\right) \tag{18}$$

Table 1 Simulation parameters.

Parameter	Symbol	Value
Rated power	P_{out}	1000 W
Input voltage	V_{in}	50 V
Switching and sampling frequency	f_{sw}	20 kHz
Filter inductor	L_f	1 mH
PV parasitic capacitor	C_{PV}	0.1 mF
Ground resistance	R_g	3 Ω
DC bus capacitor	C_{dc}	940 µF
Topology inductor	L	10 mH

According to relations (15,17), in next sampling instant $K+1$, the control variable i_s can be predicted through k^{th} instant of current i_s. According to (19), defined cost function J in k^{th} instant, determine switching states for the least value of that for various states.

$$J^{1}_{\substack{Z=0,1\\P=0,1\\N=0,1}}=W\left|i_s(\mathrm{k+1})_{Z,P,N}-i_{ref}\right|^2 \tag{19}$$

6 Experimental and simulation verifications

Using the PSCAD software, simulation results of the proposed inverter are shown in Fig. 12(a) and Fig. 12(b). The selected parameters of the simulations are listed in Table 1. A resistor and a capacitor are connected in series to simulate the parasitic effect of the PV panel and they connected between the ground and the input source. A sinusoidal current is injected to the grid. Fig. 10(a) shows the sinusoidal injected current with small ripple. The output current waveform in comparison with a reference waveform is presented in Fig. 12(a). The response of MPC is very fast for the following reference current. The blue curve shows the output current; and the green curve shows the reference current. It is clear that the output current is highly sinusoidal with low harmonic distortion due to the three level output voltage. The partial enlargement of the injection current and three level output voltage are provided in Fig. 12 (c) and Fig. 12 (d).

The experimental results of the proposed inverter is presented with unity power factor for the pure resistive load in order to verify the feasibility of the proposed topology. A photograph of the proposed transformerless inverter prototype is depicted in Fig. 13. The specifications of the prototype are listed in Table 2. Fig. 14 and Fig. 15 show the experimental waveforms of the proposed topology. The experimental results for the

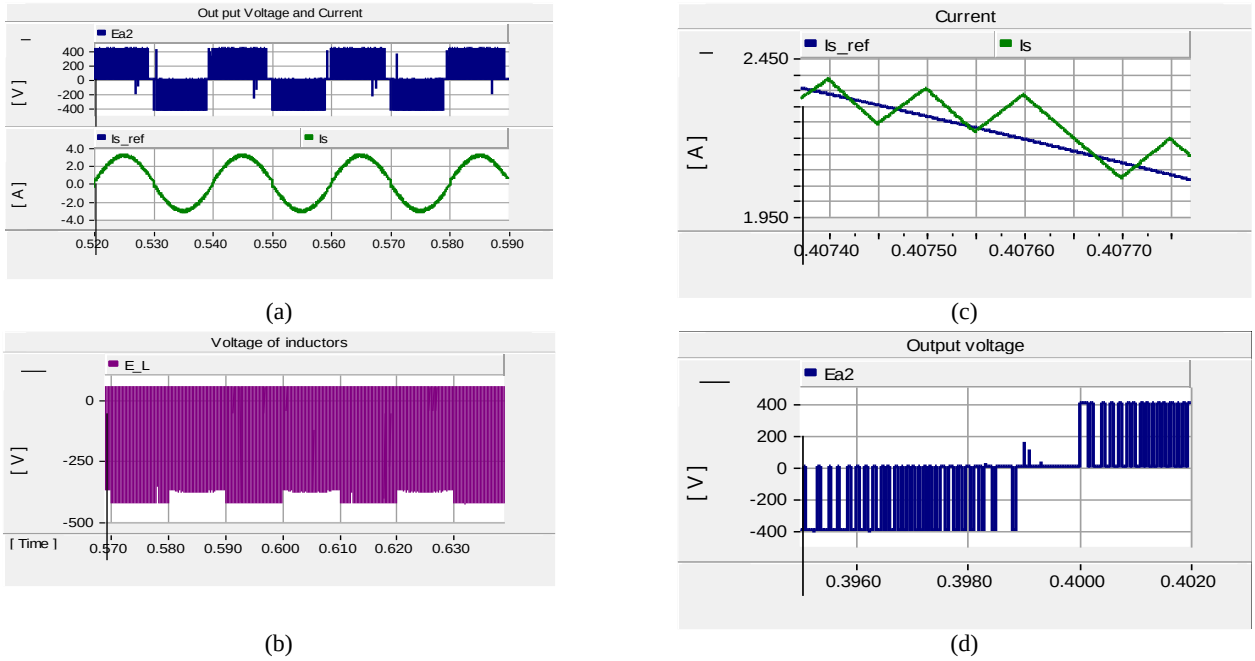


Fig. 12 Simulation results of the topology (a) injection current (b) voltage of inductor (c) enlarged of injection current (d) enlarged of output voltage.

Table 2 Experimental parameters.

Parameter	symbol	Value
Input Voltage	V_{in}	100 V
Load Resistance (R)	R_l	50 Ω
Load Inductance (L)	L_l	30 mH
DC bus capacitor	C_{dc}	940 uF
Topology Inductor	L	10 mH

output voltage and the output current are shown in Fig. 14. The voltage of dc link and input voltage are shown in Fig. 15. As shown in Fig. 14, the output voltage has three levels as V_d, 0, and $-V_d$, so a good differential mode characteristic has been achieved. As it can be seen in Fig. 14, it is clear that the output current and voltage of the proposed inverter are highly sinusoidal due to the three-level inherency of the output voltage. The RMS value of the current is equal to 2A, and the output power is 200 W. In Fig. 16 amplitudes of harmonics and fundamental component and THD of output voltage and current are shown. THD amplitude of voltage and current are about 2% and 5% for three level proposed inverter.

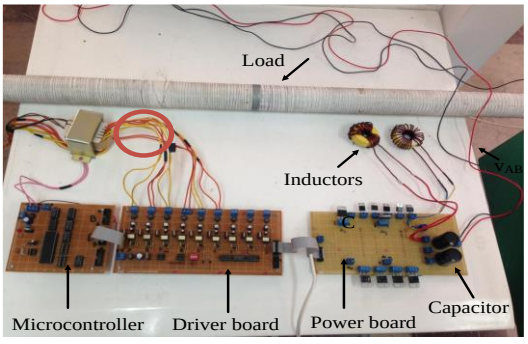


Fig. 13 Photograph of a prototype.

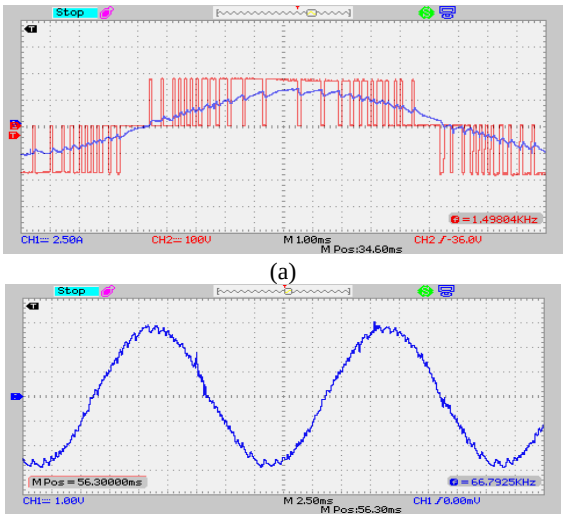
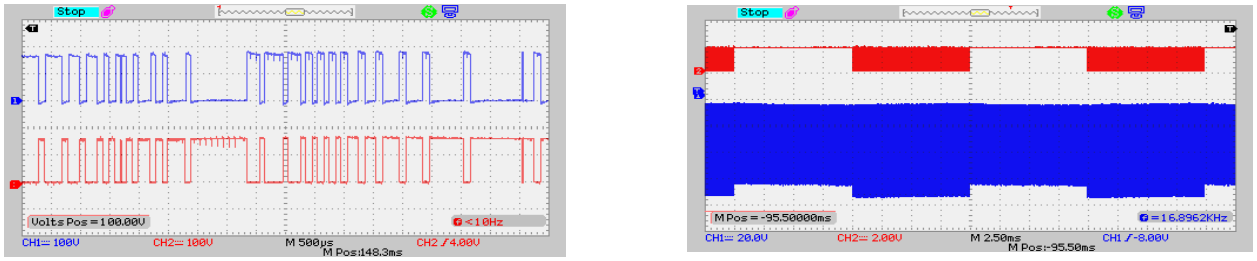


Fig. 14 Experimental waveforms of the proposed topology. (a) output current (i_{out}) [2.5 A/div] and output voltage (v_{Bn}) [100V/div] (b) output current (i_{out}) [1 A/div], time [2ms/div].

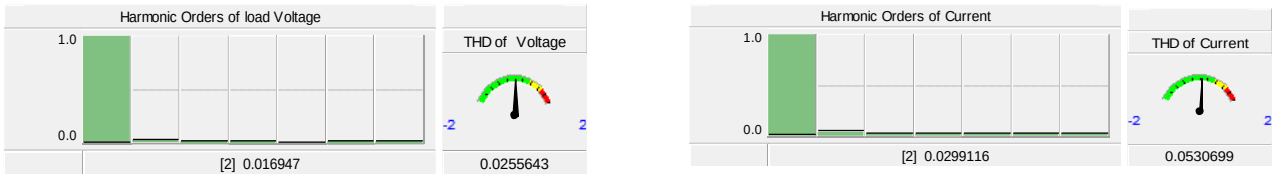
7 Comparison of the structures with the other topologies

Table 3 shows comparison of the transformerless inverter structures with respect to number of semiconductor devices and passive elements. The proposed inverter has fewer semiconductors and passive elements than the other topologies. A comparison of the RMS leakage current, THD of the inverter output voltage and efficiency of the different PV inverter topologies with the proposed topology are accomplished in Table 3. The considered converters were H5, HERIC, ANPC, H6, [20], [21] and [22]. The THD of generated



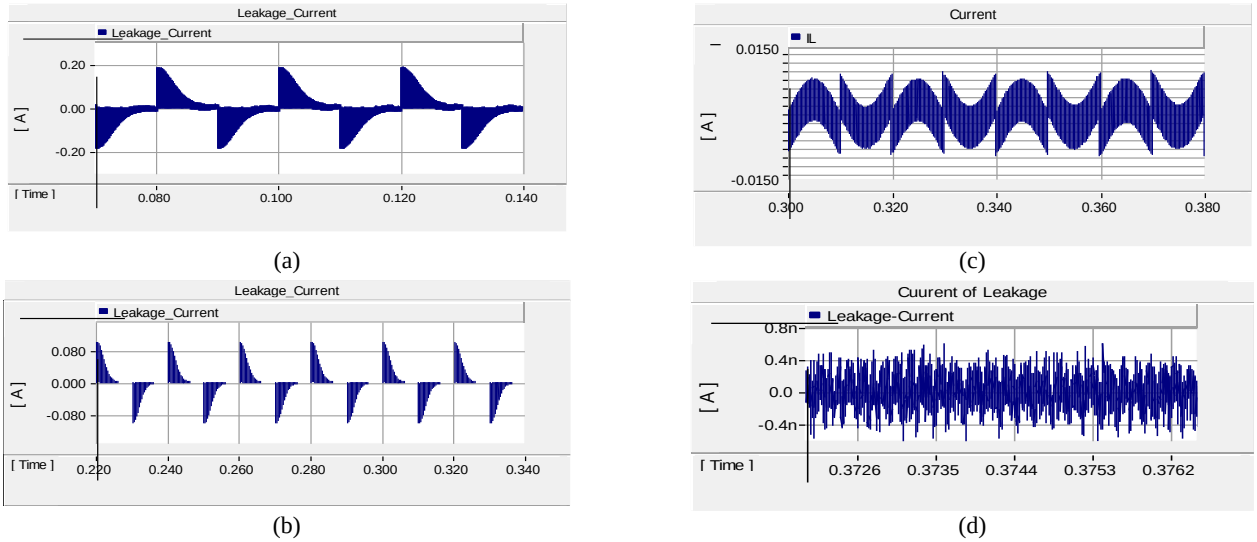
(a) (b)

Fig. 15 Experimental waveforms of the proposed topology. (a) Top to bottom: voltage of switches [100V/div] (b) voltage of switch (S_1) [2V/div] and voltage of inductor [20 V/div], time [2.5ms/div].



(a) (b)

Fig. 16 Amplitude of THD and harmonics of output (a) voltage and (b) current.



(a) (c)

(b) (d)

Fig. 17 Leakage current ($i_{leakage}$) in some PV inverters topologies: (a) [20] (b) H5 [21], (c) [22], and (d) Proposed topology.

Table 3 Comparison of the proposed converter with other topology.

Converter	Diodes	Switches	C_f	L_f	Efficiency, %	THD (%)	$i_{leakage}$ (mA)
H5	0	5	1	3	96.32	2	80
HERIC	0	6	1	3	95.7	1.9	95
ANPC [18]	0	6	2	2	96.45	1.8	70
H6 [19]	2	6	2	2	97.6	1.4	85
[20]	3	7	3	3	95.2	4.8	100
[21]	0	6	2	3	92.77	2	90
[22]	2	7	3	3	96	2.5	20
Proposed	2	6	1	2	95.12	2.5	1.5×10^{-5}

inverter output voltage is 2.5%, which confirms high quality of produced output voltage. The magnitude of the leakage current $i_{leakage}$, for these topologies is shown in Fig. 15. All these topologies have a very low leakage current. As shown in Fig. 17(a), the proposed topology in [20] has the biggest leakage current, compared with the other topologies as illustrated in Fig. 17(b) and Fig. 17(c).

8 Conclusion

A novel transformerless inverter has been proposed in this paper for single phase grid connected PV system. The leakage current is eliminated due to the common ground. In addition, the inverter can be realized with minimal number of components; hence higher power density can be achieved at lower design cost. This

topology generates a three level voltage has low core losses of the output filter at its output terminals with high voltage gain. The negative terminal of the proposed inverter is directly connected to the ground, hence the leakage current is well suppressed with only one filter inductor unlike other topologies. Compared to the other existing transformerless two stage topologies, dc input voltage can be lower than the grid voltage. Compared with other existing transformerless topologies, performance demonstrated by the proposed inverter are presently unmatched, as quantified through detailed theoretical and comparative analysis supported by simulation and experimental results.

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