A New ZVZCS Isolated Dual Series Resonant DC-DC Converter with EMC Considerations

A. Nemati* and M. Pakdel**

Abstract: A novel ZVZCS isolated dual series-resonant active-clamp dc–dc converter is proposed to obtain high efficiency. The proposed converter employs an active-clamp technique, while a series-resonant scheme controls the output voltage with the complementary pulse width modulation controller. The active-clamp circuit serves to recycle the energy stored in the leakage inductance or the magnetizing inductance and provides zero-voltage and zero-current turn-on and turn off switching. The voltage stresses of the main switch are clamped. The voltage transient spikes across the dual series active clamp circuit and the current stress of the current-fed side switches are limited by auxiliary active clamping circuits on both sides, and ZVZCS is achieved. The operating principles and design considerations are discussed and verified by simulations using PSIM software. Also, the EMI reduction techniques from EMC point of view in the circuits related to converters has been pointed out.

Keywords: Converter, EMC, Series-Resonant, Soft-Switching.

1 Introduction

In switching mode power supplies, as the switching frequency increases for high power density and with small size, switching losses associated with the turn-on and turn-off of the devices in the power converter are increased. These losses are so significant that the operations of the power converters at high frequency are limited. To overcome these problems, a number of full, quasi-, and multi-resonant dc–dc converter topologies have been investigated in [1], [2]. However, although resonant mode power conversion achieves low switching loss at high frequency compared to the pulse-width modulation (PWM) converter, these converters have some difficulties such as size reduction, EMI noise, and filter design because a wide variety of switching frequency is needed to control the output voltage. Also, the resonant converters typically have large component stresses due to high peak currents and voltages. Therefore, the trend in power processing technology has been toward combining the simplicity of PWM converters with the soft-switching characteristics of the resonant converters [3]–[10].

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* The Author is with Young Researchers Club, Islamic Azad University- Tehran South Branch, Tehran-Iran.
E-mail: nemati_abbas@yahoo.com
** The Author is with Department of Electrical and Electronic Engineering, Islamic Azad University-Miyaneh Branch, Miyaneh-Iran.
E-mail: majidpakdel@yahoo.com

As discussed in [11], the phase-shifted zero-voltage switching full-bridge converter is one of the most attractive techniques, as it allows all switches to operate at zero-voltage turn-on switching (ZVS) by utilizing the leakage inductance of the power transformer without an auxiliary switch [12]-[14]. However, the complexity of the full-bridge is almost the highest due to its increased switches and complicated control. Therefore, the active-clamp circuit and the half-bridge circuit composed of two switches and operated by the asymmetrical PWM controller are other typical examples to successfully realize ZVS for the switches by utilizing leakage inductance, magnetizing inductance, and parasitic capacitance [15]–[21]. In particular, the forward converters and the flyback converters using these circuits provide the zero-current turn-off switching (ZCS) of the output diodes by the resonant-current formed by the leakage inductance of the transformer and the clamp capacitor (or blocking capacitor). However, since these converters transfer the input energy to the output stage, when the main switch is only in the on-state or off-state, the transformer utilization is reduced in comparison with the dc–dc converter such as the push–pull, full-bridge converters.

In addition, dc–dc converters such as the conventional forward and flyback converters have a severe difficulty in surge occurrence due to leakage inductance of the transformer and the reverse-recovery problem of output diodes. To absorb the surge energy and achieve the ZVS operation, the active-clamp technique was proposed and its stability was analyzed

[22]–[24]. Forward converters and flyback converters using active-clamp circuits are the suitable topologies to achieve high efficiency at higher frequency for low and medium power applications. Active-clamp circuits were introduced as a resetting technique for the transformer of the forward converter and an active snubber in a flyback converter. Moreover, these circuits have been used as a soft-switching technique in PWM converters. Thus, the active-clamping technique has been proven to be an important component/factor for PWM converters.

In this paper, a ZVZCS isolated DC-DC converter [25] and a dual series resonant active-clamp converter [11] are combined to form a very effective zero-voltage and zero current switching converter with higher efficiency. So, the proposed topology has both advantages in comparison with the converters proposed in [11], [25]. The switches used in the proposed dc–dc converter are operated by a complementary PWM controller at the constant switching frequency. In the proposed converter, the active-clamp circuit of the primary side provides the turn-on and turn-off ZVZCS of the switches and clamps the voltage spike across the switches. Moreover, since the proposed dual series-resonant circuit provides two resonant-current paths, energy through the power transformer, regardless of the switch state, is delivered.[26] The voltage stresses across the output diodes are clamped to the output voltage of the converter. Thus, the proposed dual series-resonant active-clamp converter can reduce the voltage stress, current stress, and the switching loss of the switching devices. Also, the voltage transient spikes across the dual series activate clamp circuit and the current stress of the current-fed side switches are limited by auxiliary active clamping circuits on both sides, and ZVZCS is achieved.

The operating principles and design considerations are discussed and verified by simulations using PSIM software.

2 Principles of Circuit Operation

The ZVZCS isolated dual series-resonant dc–dc converter is proposed as shown in Fig. 1. This converter is composed of a dual series-resonant circuit and an active-clamp circuit. In this section, a detailed analysis and design concept for the turn-on and turn-off ZVZCS operation of switches and the turn-off ZCS operation of the output diodes are presented. To analyze the steady-state operation of the proposed converter shown in Fig. 1, several assumptions are made during one switching period T_S (T_S is selected 100 kHz and is the switching frequency of switches S_1 and S_2 and S_5).

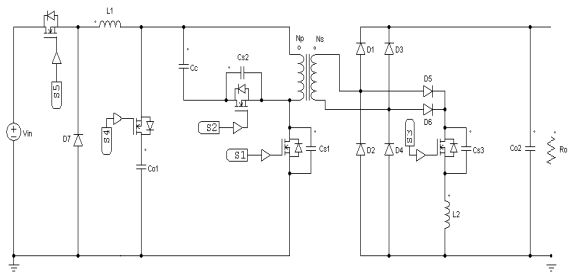

Fig. 1 Proposed ZVZCS isolated dual series-resonant converter.

1) Main switch S_1 and auxiliary switch S_2 are operated by an asymmetrical PWM method with a short dead time and the duty ratio D is based on the switch S_1.

2) All switches, S_1 and S_2, are ideal except for their output capacitances C_{S1}, C_{S2} and their body diodes.

3) The ripple component of the clamp capacitor voltage V_C is negligible because the clamp capacitor C_C has a large value. Then, the average voltage across C_C is, (DVin)/(1−D).

The steady-state operation of the proposed dc–dc converter includes eight modes during a switching period Ts. The equivalent circuits in each mode are described in Fig. 2.

Mode 1: At this mode, switches S_1, S_2, S_3 and S_5 are turned on. Switches S_1, S_2, S_3 and S_5 reverse bias diodes and the output diodes D_1 and D_3 are maintained to the off-state. Also, the capacitor C_C is charged through resonant circuit.

Mode 2: At this mode, after $1\mu s$, switch S_4 is turned on and switch S_2 is turned off after $2\mu s$. Switches S_1, S_3 and S_5 are maintained to on-state also switch S_2 reverse diode is turned on and the output diodes D_1 and D_3 are maintained to the off-state. Also, the resonant circuit is formed by the capacitor C_C and the primary magnetizing inductance of transformer and the current is oscillated among the resonant circuit.

Mode 3: At this mode, switch S_3 is turned off (the switching frequency of switches S_3 and S_4 gate drive signal is selected 200 kHz). The diode D_1 is turned on and the transformer secondary current is flowed to the load. Also, the oscillating current is flowed among the resonant circuit.

Mode 4: At this mode, after $1\mu s$, switch S_4 is also turned off and the capacitor C_{O1} is charged through switch S_4 reverse bias diode. Also, the oscillating current is flowed among the resonant circuit.

Mode 5: At this mode, switches S_1 and S_5 are turned off and switch S_3 is turned on and the capacitor C_C is discharged through the resonant circuit and in this mode the second of transformer is short-circuited through switch S_3 and inductor L_2.

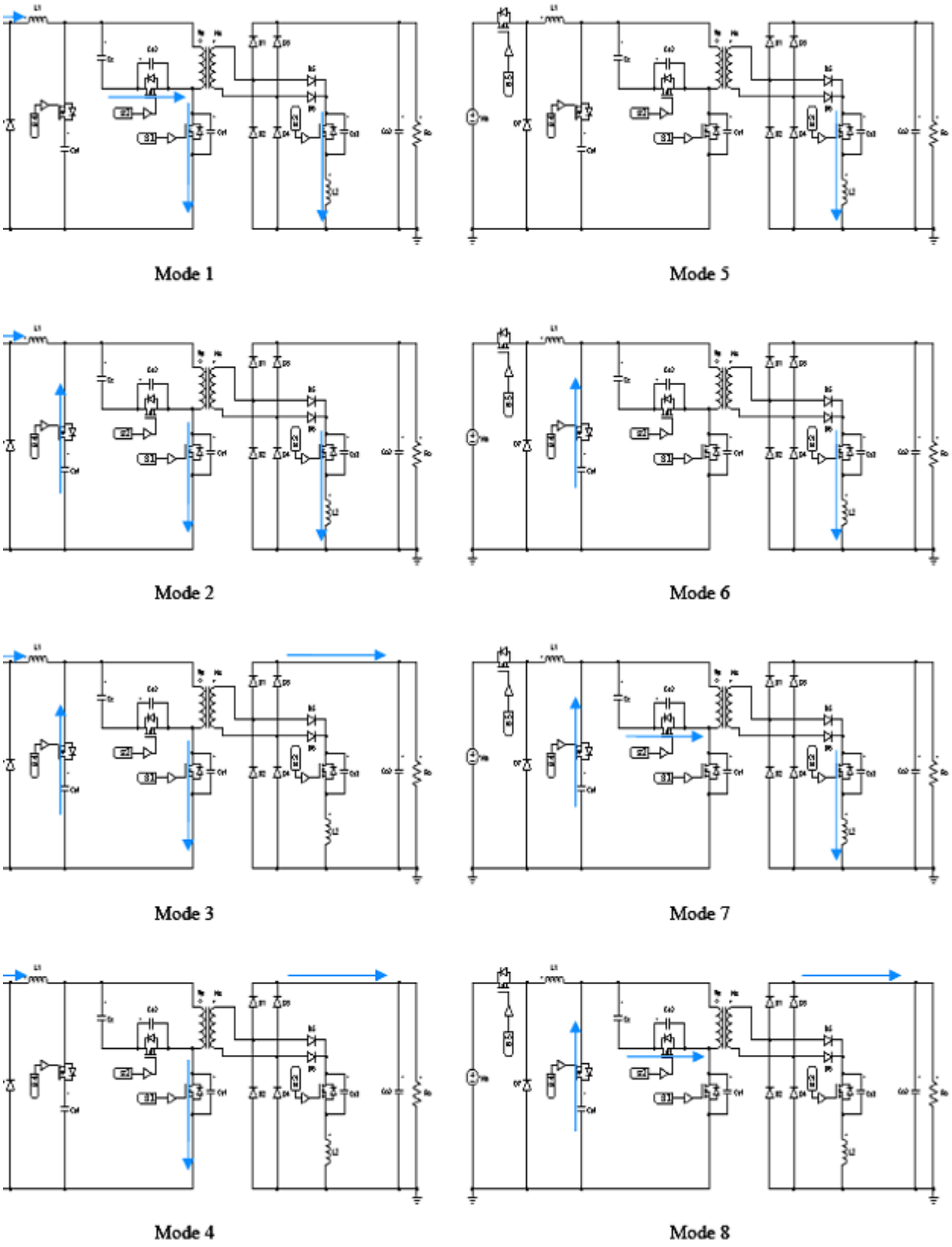

Fig. 2 Equivalent Circuit of Operation Modes.

Mode 6: At this mode, switch S_4 is turned on after $1\mu s$, and the capacitor C_{O1} is also discharged through the resonant circuit.

Mode 7: At this mode, switch S_2 is turned on and the capacitor C_C is charged through the resonant circuit.

Mode 8: At this mode, switch S_3 is turned off and the current is flowed to the load.

3 Analysis of Circuit Parameters

In this section, the design equations of the proposed ZVZCS isolated dual series-resonant dc–dc converter using the active-clamp mechanism operated by the complementary PWM controller are introduced. As in [11], the ripple component of the clamp capacitor C_C voltage V_C can be neglected by the large clamp capacitor value. Therefore, the average voltages across switches S_1 and S_2 are the sum of the dc-input voltage V_{in} and the average clamp capacitor voltage V_C is as follow [11]:

$$V_{S1} = V_{S2} = V_{in} + V_C = \frac{1}{1-D} V_{in} \tag{1}$$

Thus, if voltages V_{S1} and V_{S2} are determined by considering the voltage-rating, and the voltage-margin of the switches S_1, S_2 and the dc-input voltage V are selected, the duty ratio D can be calculated from (1).

If the leakage inductance of the transformer is a very small value compared to the magnetizing inductance, the voltage transfer function of the proposed converter then becomes that of an isolated boost converter. Therefore, although this paper does not manage the step-up applications, the proposed converter can be considered as the isolated boost converter suitable for the step-up applications. Turns ratio n of the transformer is thus obtained as [11]:

$$n = \frac{V_o}{V_{in}}(1-D) \tag{2}$$

The soft switching of the auxiliary switch S_2 is naturally achieved by the stored energy in the leakage inductance L_{lk} and the magnetizing inductance L_m. However, The ZVS design of the main switch S_1 is determined by the magnetizing inductance Lm and the output power P_O. If the maximum output power $P_{O\max}$ of the converter is selected, from the turn-on ZVS condition [27] to meet the soft switching of the main switch S_1, the magnetizing inductance value L_m can be determined as:

$$L_m \langle \frac{D(1-D)^2 V_o^2}{2 n^2 f_S P_{o,\max}} \tag{3}$$

where f_S is the switching frequency? The critical angular resonant frequency ω_{rc} for the turn-off ZCS design of the output diodes D_1 and D_2 is determined according to the duty ratio D. If the duty ratio D is smaller than 0.5 at the selected constant input voltage V_{in}, the critical angular resonant frequency ω_{rc} can be obtained as follows [11]:

$$\omega_{rc} = \frac{\pi}{D} f_S \tag{4}$$

4 EMC Consideration

For EMI reduction from EMC point of view in converters and related circuits can be used from the following methods [28]:

a. use of the common mode current, ferrite-bead and optocoupler on the transmission lines,

b. use of the suitable input filtering;

c. use of the trace termination to do impedance matching in transmission lines between source, transmission line and load Impedances;

d. EMI reduction through reduction of clock signal edge rate or increase of its rise/fall time. With decreasing the clock signal edge rate can delete many of the clock signal undesirable harmonics in

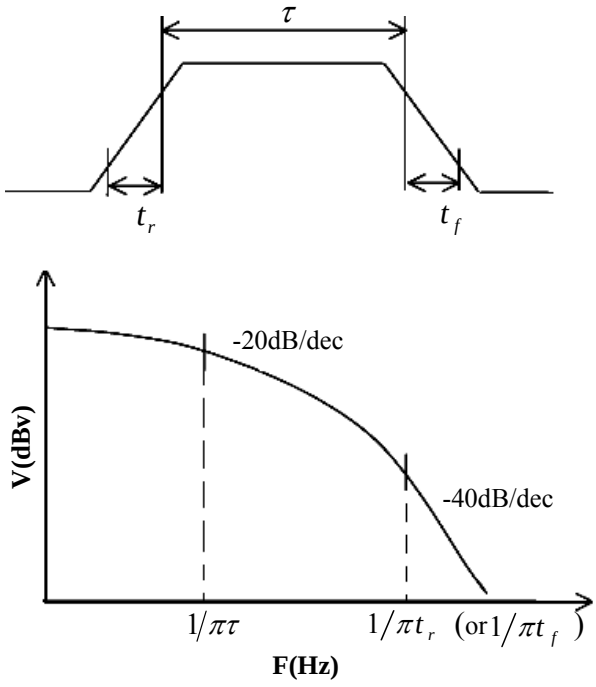

Fig. 3 Clock signal with related Fourier transform.

Frequency Spectrum, specially in radio frequency (RF) according Fig 3.

e. EMI reduction through reduction of the line length.

5 Simulation Results

To verify the theoretical analysis of the proposed topology, the simulation results using PSIM software are given. The proposed topology and control strategy in PSIM workspace is shown in Fig. 4, the following parameters have been chosen in simulation circuit: $V_{in} = 200V$, $L_1 = 4\mu H$, $C_{O1} = 560\ \mu F$, $C_C = 2.2\,\mu F$ $L_2 = 10\,\mu H$, $C_{S1} = C_{S2} = C_{S3} = 1nF$, $L_m = 500\ \mu H$ $N_P / N_S = 40/14$, $C_{O2} = 560\ \mu f$, $R_o = 1\Omega$.

The current and voltage across the switch and drive signal ZVZCS waveforms of switches S_1, S_2, S_3, S_4 and S_5 are shown in Figs. 5-9 respectively. Also, the waveform of output voltage, V_{out}, is shown in Fig. 10. The output power of the ZVZCS isolated dual series resonant dc-dc converter is about $650W$. As shown in Figs. 4-9, the proposed topology for dc-dc converter has lower power losses and higher efficiency and soft-switching zero-voltage or zero-current or both of the conditions take place in turn on and turn off of all the switches.

6 Experimental Results

Fig. 11 illustrates the experimental circuit of the study and figures 12-18 show the obtained results of experimental circuit of the present study. In this circuit as discussed in part 4, the EMC Techniques such as input filtering, clock signal edge rate reduction and using common mode choke, ferrite bead and optocoupler have been used for EMI reduction. The clock signal frequency is 50 kHz and is shown in Fig. 12. The voltage V_{DS} for switches S_1, S_2, S_3, S_4 and S_5 are shown in Figs. 13-18. Also, the DC output voltage is shown in Fig. 18.

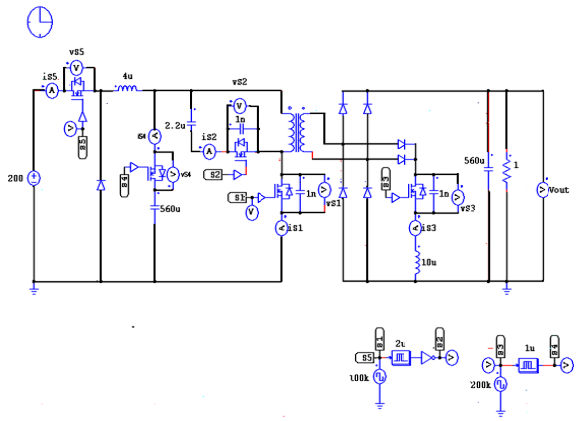

Fig. 4 The proposed topology and control strategy using PSIM software.

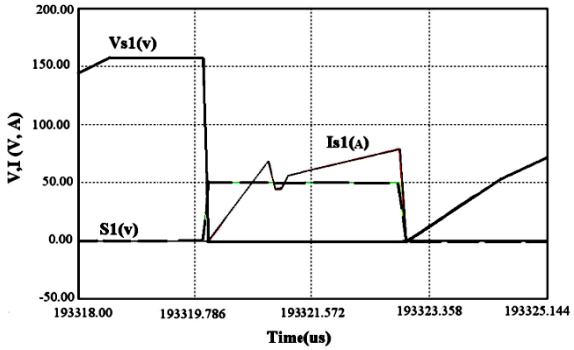

Fig. 5 ZVZCS waveforms of I_{S1} , V_{S1} , and S_1 drive signal.

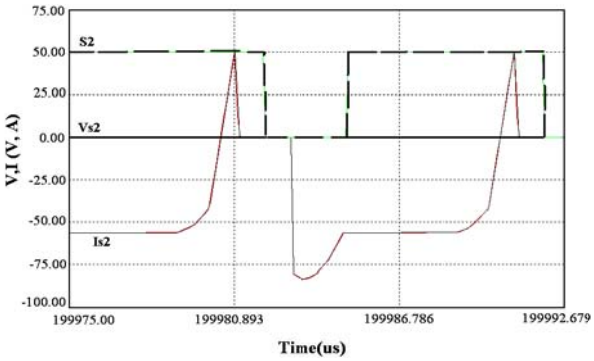

Fig. 6 ZVZCS waveforms of I_{S2} , V_{S2} , and S_2 drive signal.

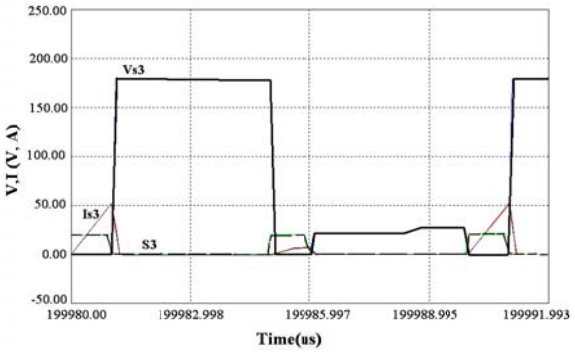

Fig. 7 ZVZCS waveforms of I_{S3} , V_{S3} , and S_3 drive signal.

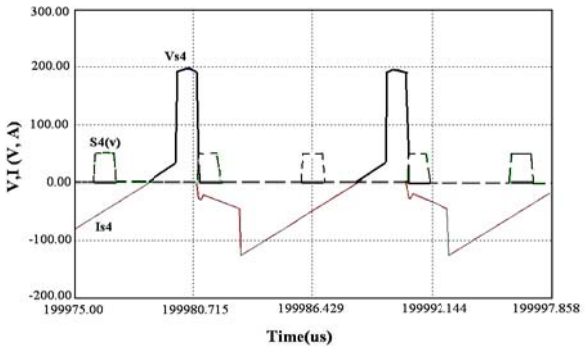

Fig. 8 ZVZCS waveforms of I_{S4} , V_{S4} and S_4 drive signal.

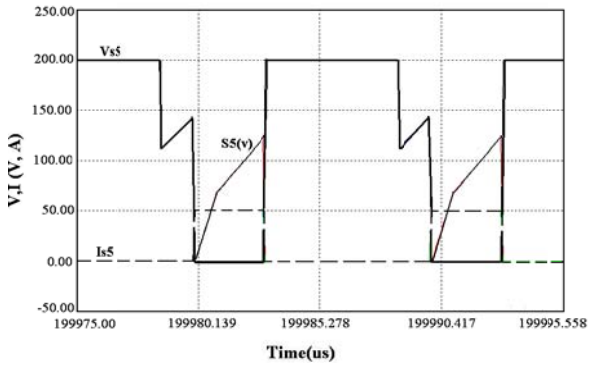

Fig. 9 ZVZCS waveforms of I_{S4} , V_{S4} and S_5 drive signal.

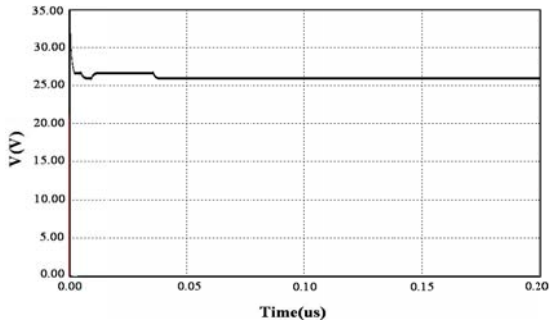

Fig. 10 Waveform of V_{out} .

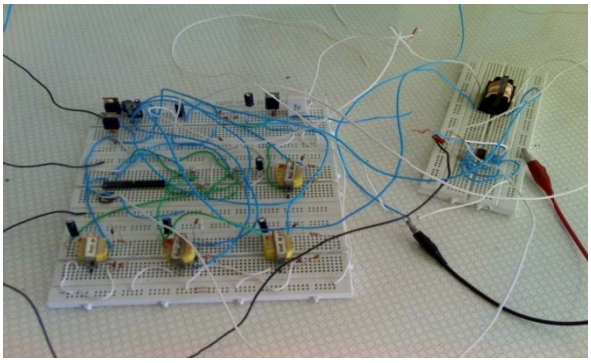

Fig. 11 Experimental Circuit.

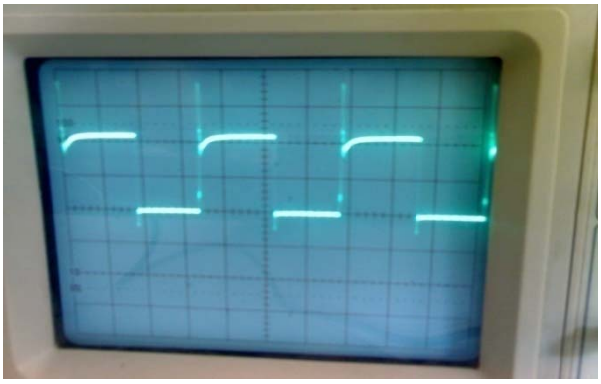

Fig. 12 Clock Signal.

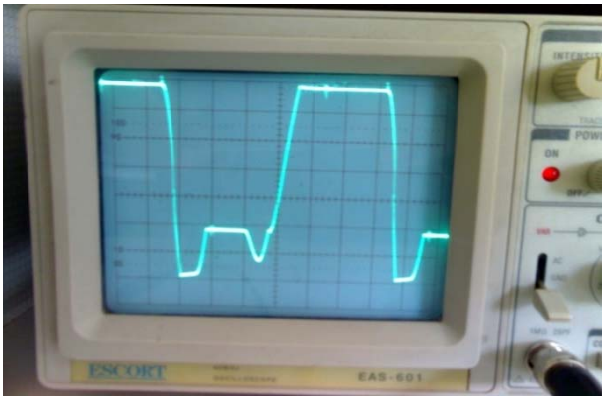

Fig. 13 V_{DS} for switch S_1 .

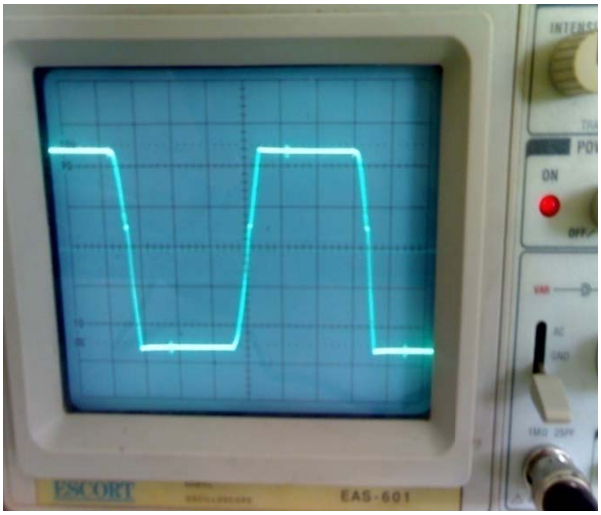

Fig. 14 V_{DS} for switch S_2 .

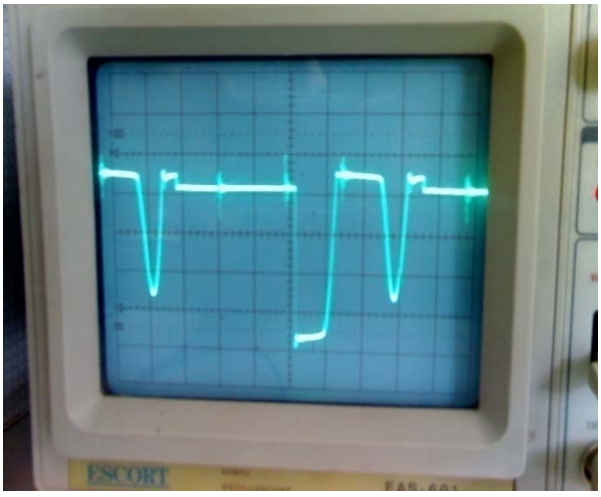

Fig. 15 V_{DS} for switch S_3 .

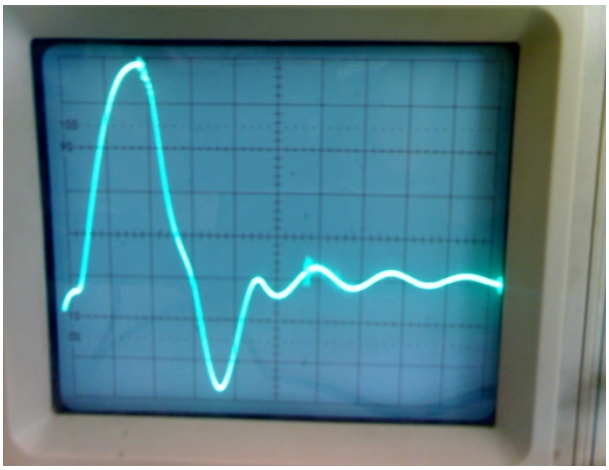

Fig. 16 V_{DS} for switch S_4 .

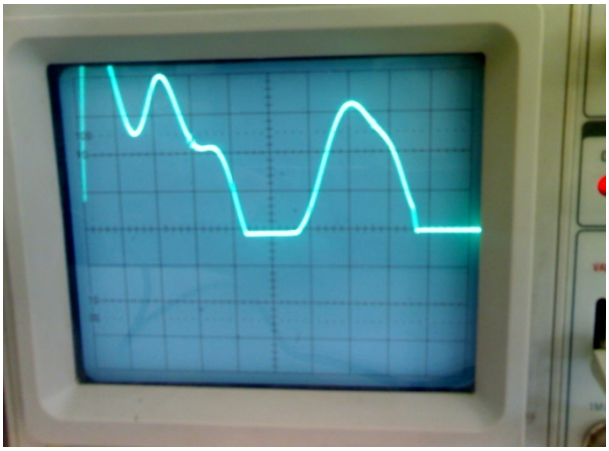

Fig. 17 V_{DS} for switch S_5 .

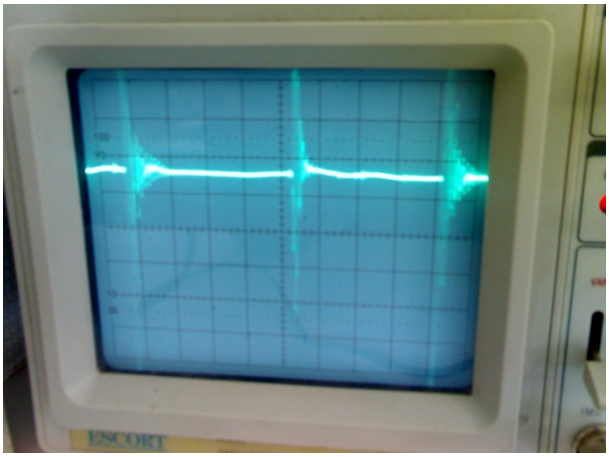

Fig. 18 Waveform of DC output voltage (V_{out}).

7 Conclusion

A ZVZCS isolated dual series resonant dc-dc converter with high efficiency has been proposed. Analysis, design, and simulation and experimental results for the proposed converter have also been presented. This proposed converter combines the active-clamp circuit and the dual series-resonant circuit across the power transformer proposed in [12] with the topology proposed for soft switching dc-dc converter in [25]. The dual series-resonant circuit provides two resonant-current paths formed by the leakage inductance of the power transformer and the resonant capacitors. In addition, the turn-on and turn-off ZVS and ZCS mechanism of the switches by the active-clamp and auxiliary input and output switches, they reduce the switching losses and the reverse-recovery losses. Therefore, the proposed converter provides high efficiency at the full load. EMC Important techniques used in the converter circuit reduce EMI and increase performance in the circuit.

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Abbas Nemati, He received the M.Sc. degree in Electronic Engineering from the Islamic Azad University Tehran South Branch in 2005. He has published the first book in EMC Engineering that published by Amirkabir University of Technology, Tehran, Iran. He is the faculty member at the Department of Electrical and Electronics Engineering and the head of Young Researchers Club in Islamic Azad University Miyaneh Branch; He teaches the professional lessons of the B.Sc, degree in Electronics and Communication engineering in Islamic Azad University Miyaneh Branch. He also is the member of Shiny Talent Office and Young Researchers Club in Islamic Azad University Tehran South Branch. His research interests include EMC, EMI Reduction, high-power PWM converters, modeling and control of power converters, microcontrollers and electronic drives. He has published 5 IEEE technical papers.

Majid Pakdel He received the B.S. degree from the Amirkabir University of Technology, Iran, in 2005 and the M.S. degree from the Isfahan University of Technology, Iran, in 2007. He is an instructor at the Department of Electrical and Electronics Engineering, Islamic Azad University, Miyaneh Branch. His research interests include high-power PWM converters, modeling and control of power converters, applied digital control, finite element analysis, microcontrollers and electrical drives. He has published one journal and 12 IEEE technical papers.