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Research Paper

New Cascaded Multilevel Inverter With Reduced Power Electronic Components

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Abstract: In this paper, a new structure for cascade multilevel inverter is presented which consists of a series connection of several sub-multilevel units. Each sub-multilevel unit comprises of eight unidirectional switches, two bidirectional switches, and six DC voltage sources. For the proposed cascade topology, two algorithms are presented to produce all possible levels at the output voltage waveform. The required analysis of the voltage rating on the switches is provided. In order to verify the performance of the proposed inverter, the experimental results for a 15-level inverter are provided. The experimented 15-level inverter is compared with the other presented inverters in literature in terms of the number of DC voltage sources, switches, drivers, and blocked voltage by switches. The results of comparisons indicate that the experimented 15-level inverter requires lower power electronic elements. Moreover, the blocked voltage on the switches of the proposed topology is less than other topologies.

Keywords: Multilevel Inverter, Blocked Voltage, Harmonic Distortion, Fundamental Frequency Switching.

1 Introduction

In recent years, the application of multilevel inverters in electrical industry such as renewable energy sources, machine drives, and power quality devices have been increased. Multilevel inverter is a power electronic system which can produce a stepped waveform at output voltage. As the number of output voltage levels is increased, the total harmonic distortion of output voltage is increased and the voltage stress on semiconductors is reduced [1-3]. Two-level inverter was the first topology which consists of two power switches and one DC voltage sources. This topology is suitable for low voltage applications. The voltage stress on the switches of two-level inverter is high and equal to the amplitude of input DC voltage source. Moreover, the switching losses and harmonic distortion of output voltage and current waveforms are high [4, 5]. To solve these problems, conventional multilevel inverters were introduced which have been named

- Flying capacitor multilevel inverter,
- Diode-clamped multilevel inverter,
- Cascade multilevel inverter.

The mentioned structures use similar numbers of switches. However, the number of on-state switches in current path in the flying-capacitor and diode-clamped multilevel inverters is less than cascade topology which reduce the conduction and switching losses. Using high numbers of capacitors and diodes are the main disadvantages of flying capacitor and diode-clamped multilevel inverters. Also, balancing the voltage of capacitors in flying capacitor and diode-clamped multilevel inverters is another disadvantage. The cascade multilevel inverter uses a large number of DC voltage sources for producing higher levels which increase the circuit size and converter cost [6-8].

In order to improve, the power electronic parameters in conventional multilevel inverters, many structures have been presented by researchers. A basic ladder structure has been presented in [9] which include several DC voltage sources along with common-emitter bidirectional switches. In this structure, in order to

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produce any levels, there are only four switches in current path. However, this topology requires many transistors and the voltage on switches is high. In [10], a new structure for multilevel inverter has been suggested which need low number of transistors and can be used in low voltage applications. In this topology, the number of on-state switches in current path increase with increasing the number of output voltage levels. Another multilevel inverter has been introduced in [11] which require lower transistors and the power loss is increased by increasing the number of output voltage levels. In order to reduce the number of drivers in the presented structures in [9-11], a ladder multilevel inverter has been presented in [12] which consists of several bidirectional switches and DC voltage sources. In this topology, by increasing the number of levels, the voltage on bidirectional switches increases which limits its applications in high voltage applications.

In order to improve the power electronic parameters in the above mentioned structures, other structures have been presented in [13-21] which are the combination of presented multilevel inverters in [9-11]. The presented structures in [9-11] are not suitable candidate for high voltage applications. In these structures, there are four high voltage switches which restrict their applications in high voltage applications. However, the presented structures in [15] and [16] are suitable for low voltage applications. All presented multilevel inverters in [9-16] require the same number of DC voltage sources.

In [17], another cascade multilevel converter topology based on series connection of several stages has been proposed in which each stage consists of two same basic units which are connected to each other using two unidirectional switches. This structure can produce any levels at output voltage waveform. In [18], another improved H-bridge multilevel converter topology has been proposed which is able to produce all levels. This topology uses a large numbers of IGBTs. In [19], a new symmetric multilevel converter structure with low voltage on switches and DC source has been presented. Other symmetric and asymmetric types for multilevel converters have been proposed in [20-21].

In this paper, a new cascade multilevel inverter based on the cascaded connection of 15-level inverters has been proposed. The performance of the proposed structure is analyzed using a look-up table and mathematical analysis of voltage on switches. The proposed 15-level inverter is compared with proposed 15-level inverters in [9-21] in terms of the number of transistors, drivers, DC sources, and on-state switches. Also, the performance of the proposed 15-level inverter is evaluated using experimental setup.

2 Proposed Sub-Multilevel Inverter

The structure of the proposed sub-multilevel inverter is indicated in Fig. 1. As shown in this figure, the proposed structure comprises six unidirectional switches (S_1, S_3, S_6, S_8, S_9, and S_{10}), four bidirectional switches (S_2, S_4, S_5, and S_7) and six DC voltage sources. The proposed topology can be used for any values of resistive and inductive loads. The unidirectional switch consists of an IGBT along with an anti-parallel diode which requires only one gate driver circuit. The type of used bidirectional switch is common-emitter which includes series connection of two unidirectional switches. The used bidirectional switch requires one driver and can withstand both positive and negative voltage levels. By selecting the values of DC voltage sources as $V_1=V_{dc}$, $V_2=2V_{dc}$, and $V_3=4V_{dc}$, the proposed structure can produce 15 levels at output voltage waveform. The generated levels are 0, $\pm V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, $\pm 5V_{dc}$, $\pm 6V_{dc}$, and $\pm 7V_{dc}$. The switching states of the proposed 15-level inverter are shown in Table 1. In this table, 0 and 1 mean that the switches are in OFF and ON states, respectively. As shown in this table, there are two states for generating the zero level. According to this table, it is clear that there are only three switches in current path at any levels which reduce the power losses such as switching and conduction losses. The value of blocked voltage by switches is an important parameter that affects the inverter cost. The standing voltage by the switch in OFF-state is named the blocked voltage by switch. The values of blocked voltage on the switches in the proposed 15-level inverter are calculated as follows:

$$V_{S4}=V_{S5}=V_{S9}=V_{S10}=2(V_1+V_2+V_3) \quad (1)$$

$$V_{S4}=V_{S5}=2(V_1+V_2)+V_3 \quad (2)$$

$$V_{S7}=V_1 \quad (3)$$

$$V_{S6}=V_{S8}=2V_1 \quad (4)$$

$$V_{S2}=V_2 \quad (5)$$

$$V_{S1}=V_{S3}=2V_2 \quad (6)$$

Then, the total blocked voltage by all switches is:

$$V_{S,T}=61V_{dc} \quad (7)$$

3 Proposed Cascade Multilevel Inverter

There are four switches in the structure of the proposed sub-multilevel inverter which withstand maximum value of output voltage. This feature causes

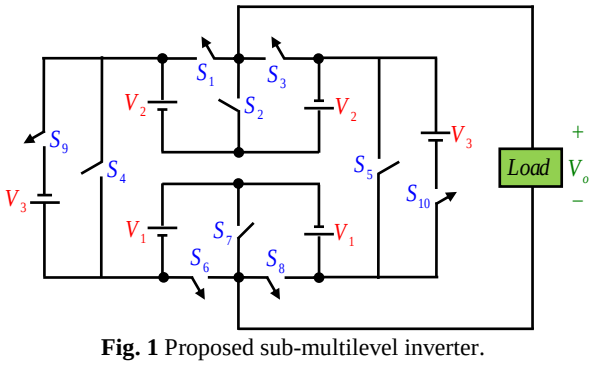


Fig. 1 Proposed sub-multilevel inverter.

Table 1 The switching states of proposed 15-level inverter.

States	ON and OFF switches										Output voltage (V_o)
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	
1	0	0	1	0	1	0	0	1	0	0	0
	1	0	0	1	0	1	0	0	0	0	
2	0	0	1	0	1	0	1	0	0	0	V_{dc}
3	1	0	0	1	0	0	1	0	0	0	$-V_{dc}$
4	0	1	0	0	1	0	0	1	0	0	$2V_{dc}$
5	0	1	0	1	0	1	0	0	0	0	$-2V_{dc}$
6	0	1	0	0	1	0	1	0	0	0	$3V_{dc}$
7	0	1	0	1	0	0	1	0	0	0	$-3V_{dc}$
8	0	0	1	0	0	0	0	1	0	1	$4V_{dc}$
9	1	0	0	0	0	1	0	0	1	0	$-4V_{dc}$
10	0	0	1	0	0	0	1	0	0	1	$5V_{dc}$
11	1	0	0	0	0	0	1	0	1	0	$-5V_{dc}$
12	0	1	0	0	0	0	0	1	0	1	$6V_{dc}$
13	0	1	0	0	0	1	0	0	1	0	$-6V_{dc}$
14	0	1	0	0	0	0	1	0	0	1	$7V_{dc}$
15	0	1	0	0	0	0	1	0	1	0	$-7V_{dc}$

the suggested sub-multilevel inverter to be used in low voltage applications. Also, the proposed sub-multilevel can generate only 15 levels which is a limitation for generating higher numbers of levels. In order to increase the number of levels and using in high voltage applications, a new cascade multilevel inverter is presented which is illustrated in Fig. 2.

The values of DC voltage sources in the suggested cascade inverter determine the number of generated levels at output voltage waveform. For this aim, two new algorithms for selecting the values of DC sources are presented as follows.

2.1 Proposed First Algorithm

In this algorithm, the values of DC voltage sources are adjusted as follows:
First Sub-multilevel:

$$V_{1,1}= V_{1,2}=\ldots= V_{1,n} =V_{dc} \quad (8)$$
$$V_{2,1}= V_{2,2}=\ldots=V_{2,n}=2V_{dc} \quad (9)$$
$$V_{3,1}= V_{3,2}=\ldots= V_{3,n}=4V_{dc} \quad (10)$$

Using the proposed first algorithm, the number of levels at output load will be:

$$N_{level} = 14n+1 \quad (11)$$

where n is the number of used sub-multilevel inverter in the suggested cascade inverter. In this algorithm, the cascade topology consists of several similar sub-multilevel units.

2.2 Proposed Second Algorithm

By the use of this algorithm, the magnitudes of DC voltage sources are computed using the following equations:
First Sub-multilevel:

$$V_{1,1}=V_{dc} \quad (12)$$

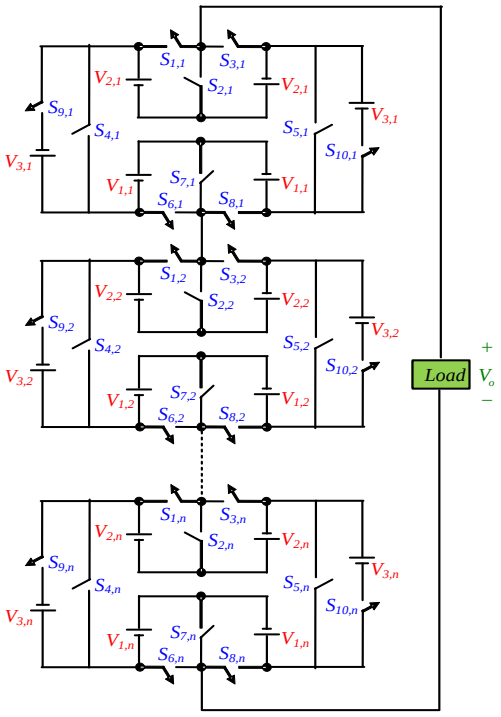


Fig. 2 Proposed cascade multilevel inverter.

$$V_{2,1}=2V_{dc} \quad (13)$$
$$V_{3,1}=4V_{dc} \quad (14)$$

Second Sub-multilevel:

$$V_{1,2}=8V_{dc} \quad (15)$$
$$V_{2,2}=16V_{dc} \quad (16)$$
$$V_{3,3}=32V_{dc} \quad (17)$$

n^{th} Sub-multilevel:

$$V_{1,n}=8^{n-1}V_{dc} \quad (18)$$
$$V_{2,n}=2\times8^{n-1}V_{dc} \quad (19)$$
$$V_{3,n}=4\times8^{n-1}V_{dc} \quad (20)$$

By adjusting the amplitude of DC sources using the proposed algorithm, the number of levels will be:

$$N_{level} = 15^n \quad (21)$$

In this algorithm, the proposed cascade topology comprises of several different sub-multilevel units. The value of blocked voltage on the switches of proposed cascade inverter is calculated as follows:

$$V_{S\,4,i} =V_{S\,5,i} =V_{S\,9,i} =V_{S\,10,i} = 2(V_{1,i} +V_{2,i} +V_{3,i}) \quad i =1,2,...,n \quad (22)$$
$$V_{S\,4,i} =V_{S\,5,i} = 2(V_{1,i} +V_{2,i}) +V_{3,i} \quad i =1,2,...,n \quad (23)$$
$$V_{S\,7,i} =V_{1,i} \quad i =1,2,...,n \quad (24)$$
$$V_{S\,6,i} =V_{S\,8,i} = 2V_{1,i} \quad i =1,2,...,n \quad (25)$$
$$V_{S\,2,i} =V_{2,i} \quad i =1,2,...,n \quad (26)$$
$$V_{S\,1,i} =V_{S\,3,i} = 2V_{2,i} \quad i =1,2,...,n \quad (27)$$

4 Experimental Results

In this section, the structure of proposed 15-level inverter is implemented to prove the validity of the given theories. The photo of implemented setup is shown in Fig. 2. The obtained results are evaluated for verifying the performance of suggested 15-level inverter. In order to control the used switches, the fundamental frequency switching strategy is used. The values of R-L load and DC voltage sources are summarized in Table 2.

The output voltage waveform of experimental 15-level inverter is shown in Fig. 3. As shown in this figure, this topology can produce 15 levels and the maximum value of output voltage is 70V. Fig. 3 indicates the output current waveform is similar to the sinusoidal waveform due to the using higher value of inductive load. The maximum magnitude of output current is 1.2A. The waveforms of blocked voltage by the switches S_9, S_{10}, S_2, and S_5 are shown in Fig. 4. According to this figure, the voltage on switches S_9 and S_{10} is positive which proves these switches should be unidirectional. The maximum blocked voltage by the switches S_9 and S_{10} is equal to 140V. According to Fig. 4, the voltages on the switches S_2 and S_5 consist of both positive and negative levels. It means that these switches should be designed as bidirectional. The maximum blocked voltage by the switches S_2 and S_5 are 100V and 100V, respectively. The sum maximum values of blocked voltage by all switches are 610V. The obtained results from experimental prove the mathematical analysis and performance of the proposed 15-level inverter.

Table 2 The values of parameters in the implemented 15-level inverter.

Parameter	Value
R	50mH
L	80Ω
V_1	10V
V_2	20V
V_3	40V

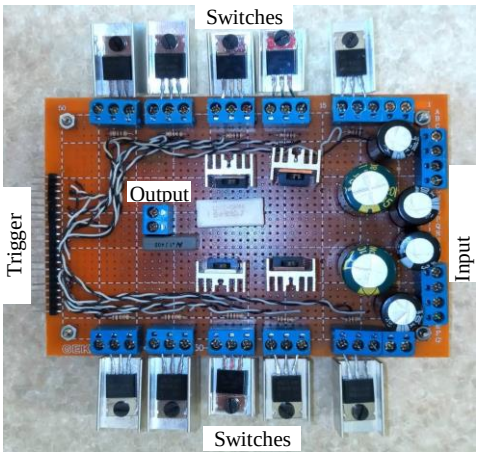


Fig. 3 The photo of implemented setup.

Table 3 indicates the number of IGBTs, drivers, DC voltage sources, and on-state switches in current path for different topologies. This table proves that the proposed topology requires the least numbers of IGBTs compared to other topologies. Also, the number of used drivers in the proposed topology is equal to [16] and

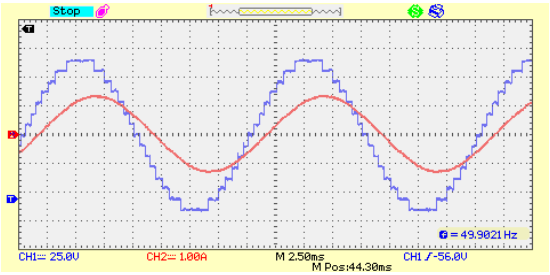
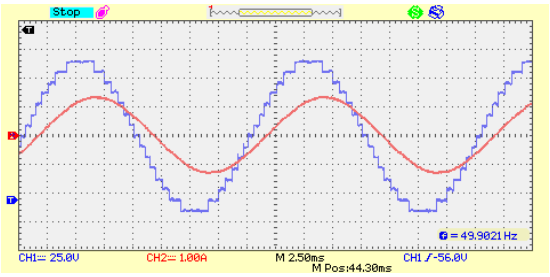
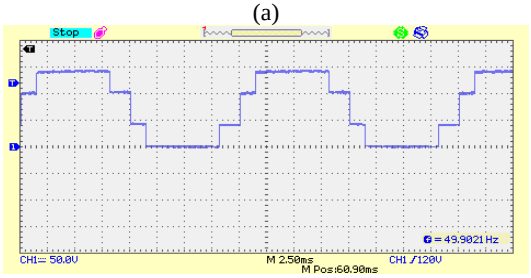


Fig. 4 The output voltage and current waveforms.



(a)



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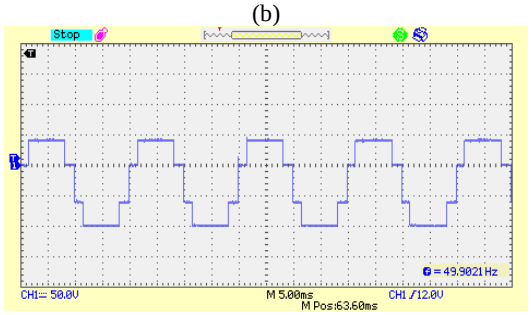
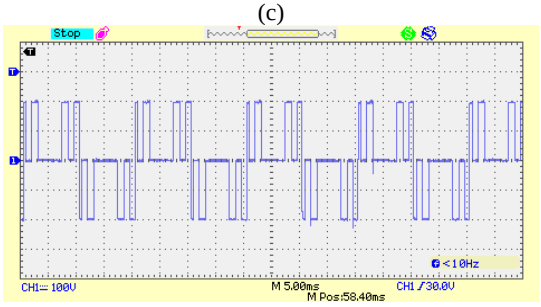


(c)



(d)

Fig. 5 The waveform of voltage on switches in the experimental 15-level inverter; a) S_9, b) S_{10}, c) S_2, and d) S_5.

Table 3 Comparison of proposed 15-level inverter with other structures.

Structure	Parameters					
	N_{level}	IGBTs	Drivers	DC voltage sources	On-state switches	Total Voltage on Switches
Symmetric CHB	15	28	28	7	14	$28V_{dc}$
Binary CHB	15	12	12	3	6	$28V_{dc}$
[7]	13	14	14	6	6	$22V_{dc}$
[8]	15	16	10	7	4	$52V_{dc}$
[9]	15	32	16	7	4	$88V_{dc}$
[10]	15	18	18	7	11	$46V_{dc}$
[11]	15	19	19	7	11	$33V_{dc}$
[12]	15	19	11	7	4	$42V_{dc}$
[13]	15	16	16	7	9	$52V_{dc}$
[14]	15	16	16	7	8	$28V_{dc}$
[15]	15	18	12	7	7	$47V_{dc}$
[16]	15	14	10	7	3	$40V_{dc}$
[17]	17	20	16	8	6	$28V_{dc}$
[18]	17	18	18	8	9	$32V_{dc}$
[19]	15	28	16	7	4	$88V_{dc}$
[20]	15	12	12	7	6	$38V_{dc}$
[21]	15	21	21	7	14	$21V_{dc}$
Proposed	15	14	10	6	3	$28V_{dc}$

less than the other topologies. Reduction of IGBTs and drivers in the proposed topology causes the circuit size and cost to be reduced. Based on this table, all proposed 15-level inverters in [8-21] requires seven and more DC voltage sources. However, the structure of the proposed 15-level inverter requires six DC voltage sources. Moreover, the comparison results indicate that the number of on-state switches in current path of the proposed 15-level inverter is equal to [15] and less than other topologies which reduce power losses. The comparison results indicate that the structure of the proposed 15-level inverter requires the least number of power electronic components compare to the proposed topologies in [7-21] and conventional cascade topology.

5 Conclusion

In this paper, a new structure for 15-level inverter was introduced firstly. Then, a cascade inverter based on the 15-level inverter was introduced. Two algorithms for selecting the amplitude of DC voltage sources were proposed. The proposed 15-level inverter was compared with traditional multilevel inverters. The comparison results show that the proposed topology requires the least number of transistors, drivers, and DC voltage sources which causes the converter cost and volume to be reduced. Also, the number of on-state switches in current path in the structure of proposed topology is less than other topologies which causes the efficiency of the presented 15-level inverter to be high. In order to verify the performance of the proposed 15-level inverter, the experimental results using a setup circuit are presented.

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