A New Topology of Bidirectional Buck-Boost dc/dc Converter with Capability of Soft Switching and input Current Ripple Cancellation

E. Babaei*(C.A.), Z. Saadatizadeh* and S. Laali*

Abstract: In this paper, a new bidirectional buck-boost dc-dc converter with capability of soft switching and zero input current ripple is proposed. The coupled inductor is used in the proposed converter to eliminate the input current ripple. In the proposed converter, zero voltage switching (ZVS) and zero current switching (ZCS) can be obtained for the main and auxiliary switches, respectively. In addition, the proposed topology is analyzed in all operating modes and all equations of voltage and current for components are obtained. Moreover, the required conditions for soft switching operation and also achieving zero input current ripple are calculated. Finally, the accuracy performance of the proposed converter is reconfirmed through simulation results in EMTDC/PSCAD software program.

Keywords: Bidirectional dc-dc Converter; Active Snubber; Zero Voltage Switching; Zero Input Current Ripple.

1 Introduction

Nowadays, the bidirectional dc-dc converters with capability of soft switching have received more attentions because of low losses. Moreover, the converters that are able to eliminate the input current ripple have most importance. In [1-4], several high power full-bridge isolated dc-dc converters with the capability of soft switching have been presented. In these converters, the input current value is equal to the switches current value for the high value of duty cycle. In addition, the high value of input current ripple is made by turning on and off the switches. In [5], a buck-boost bidirectional dc-dc converter based on coupled inductor has been presented. In this converter, the soft switching is obtained by using the resonance condition between coupled inductor and capacitors. The resonance frequency must be less than the switching frequency. Moreover, the converter has considerable ripple in input current. A new three-phase bidirectional dc-dc converter has been presented in [6]. The drawback of this converter is high input current ripple. In [7-9], several methods to eliminate the output voltage ripple in the buck and buck-boost dc-dc converters have been presented. In these topologies, in order to eliminate the output voltage ripple, the minimum values of inductor and capacitor have been calculated. In these topologies, due to hard switching its losses are inevitable. The isolated bidirectional dc-dc converters have higher voltage losses and lower efficiency in comparison with the nonisolated bidirectional dc-dc converters [10-12]. In [13], a dc-dc converter based on coupled inductors with three windings and high voltage gain has been presented. In this topology, the coupled inductors are used to generate high voltage gain and used switches are operating at ZCS. In addition, this topology has low voltage stress in high power applications. In [14], a bidirectional dc-dc converter with capability of soft switching has been presented. This topology is able to provide ZVS for all switches by using auxiliary circuit. This circuit includes of additional inductor and capacitor. In addition, high value of circulating current without considering the value of the load is crossed from auxiliary inductor and capacitor. This is the main problem of this topology that leads to high conductive losses of converter. In [15], a bidirectional dc-dc converter with the capability of soft switching and zero input current ripples has been presented. The problem of this converter is its high inductive losses due to high circulating current in all operating modes of the converter. In [16], a bidirectional four-phase dc-dc converter has been presented. In this topology, elimination the input current ripple of the conventional bidirectional dc-dc converter is considered. High
number of used switching elements and inductors in input side are disadvantages of this converter. In order to overcome the high inductive losses and circulating current in the bidirectional dc-dc converters with soft switching, the dc-dc converter with soft switching technique has been presented in [17]. In this topology, the crossed current from the auxiliary circuit is extremely decreased in comparison with the conventional converters because of operating the active snubber in the short time intervals. As a result, the inductive losses in the main switches and auxiliary circuits are extremely decreased and the efficiency of the converter is increased. In [18] a bidirectional dc-dc converter has been presented. This converter uses the coupled inductor for achieving zero voltage switching. It has the input current ripple for all the time during a switching period.

In this paper, a new bidirectional buck-boost dc-dc converter to eliminate input current ripple in all ranges of duty cycles is proposed. The proposed converter is completely analyzed in different operating modes in buck and boost operations. In addition, the voltage gain, the current and voltage equations of all elements are calculated. Finally, the accuracy performance of the proposed converter is reconfirmed through simulation results in EMTDC/PSCAD software program.

2 Proposed Converter

The power circuit of the proposed bidirectional converter is shown in Fig. 1. This topology can operate as the buck and boost dc-dc converter. The diodes of $D_1$, $D_2$, $D_3$, and $D_4$ are the internal diodes of the switches $S_1$, $S_2$, $S_5$, and $S_6$. The capacitors of $C_1$ and $C_2$ are the parasitic capacitors of the switches $S_1$ and $S_2$, respectively. The lossless active snubber consists of an auxiliary inductor $L_2$, a capacitor $C_3$, clamping diodes of $D_3$ and $D_4$, and the auxiliary switches of $S_3$ and $S_4$. The voltage of capacitor $C_4$ is considered as a voltage source $V_{c4}$ in the time interval of switching if high value of the capacitance is considered. In order to decrease the circulating current of the lossless active snubber and providing the soft switching conditions for the switches of $S_3$ and $S_4$, the active snubber will be in the circuit for the short time interval. The diodes of $D_5$ and $D_6$ act as the clamping voltage in the auxiliary switches of $S_3$, $S_4$ and the clamping diodes of $D_3$ and $D_4$ from the snubber circuit. In order to turning on the switch $S_1$ in ZVS state for the boost operating mode, firstly, the internal diode is turned on and after short time interval of applying trigger pulse to it, by changing the current direction of the diode this switch is turned on. The same condition is valid for $S_2$ in buck operating mode. In this mode, the internal diode of the switch $S_1$ is conducted for a long time interval and the ZVS is usually made in this switch. The same condition is valid for $S_2$ in the boost operating mode. The coupled inductors with the inductance of $L_p$ for the primary winding, $L_s$ for the secondary winding and $M$ for the coupling inductance are used to eliminate the input current ripple. The voltage of $V_{c3}$ is equal to the voltage source $V_i$ in the time interval of switching if the value of the capacitance is considered high enough. As a result, the inductors of $L_p$ and $L_s$ are connected in parallel and their voltage are same, so, their equivalent inductance is lower than the voltage of $L_p$ and $L_s$ separately.

2.1 Boost Operating State

The voltage and current waveforms of the proposed converter in boost operating mode are shown in Fig. 2. The equivalent circuits of the proposed converter by replacing the transformer model of the coupled inductors are shown in Fig. 3. The coupling factor, the value of inductances $L_s$ and $L_p$ are defined as follows:

$$K = \sqrt{\frac{M}{L_p L_s}}$$ (1)

$$L_s = (1 - K^2)L_p$$ (2)

$$L_p = K^2 L_s$$ (3)

As the transformers ratio ($n$) is equal to the division of the number of the primary winding $N_p$ to the number of the secondary winding $N_s$, the effective ratio $N_e$ is calculated as follows:

$$N_e = \sqrt{\frac{L_s}{L_p}} = nK$$ (4)

First Operating Mode ($t_0 \leq t < t_1$):

The equivalent circuit of the first operating mode is shown in Fig. 3(a). In this operation, the parasitic capacitor $C_2$ is charged and the parasitic capacitor $C_3$ is discharged. As the time interval of this operation is very low, it is possible to consider the current values of the inductances $i_{L2}$, $i_{Lm}$ and $i_{L3}$ equal to their minimum values $-I_{L2}$, $I_{L2}$ and $I_{L2}$, respectively. According to the fact that the voltage of capacitor $C_2$ has to be discharged completely to the zero value in this operating mode, the diode of $D_1$ is turned on. The time interval of the first operating mode ($T_1$) is calculated as follows:

$$T_1 = \frac{n(C_1 + C_3) V_n}{nI_{L2} - (n-1)I_{L2} - I_{L2}}$$ (5)

Second Operating Mode ($t_1 \leq t < t_2$):

The equivalent circuit of this mode is shown in Fig. 3(b). The switch of $S_1$ is turned on in the ZVS state. Based on the equivalent circuit, the voltage of the
inductors $L_m$, $L_k$ and $L_2$ are equal to $V_i/n$, $v_{ip} - v_{im}$ and $V_{C4}$, respectively. The current of these inductors are linearly increased. So according to the auxiliary circuit in the input section we have $v_{ip} = v_{im} = n v_{im} = V_i$.

Therefore it can be written:

$$i_{im} = \frac{V_i}{n L_m} (t - t_1) + i_{m2} \quad (6)$$

$$i_{ik} = \frac{(n-1)V_i}{n L_k} (t - t_1) + i_{k2} \quad (7)$$

$$i_{ps} = i_{ik} \left(1 - \frac{1}{n}\right) + \frac{i_{im}}{n} + \left[\left(\frac{n-1}{n}\right)^2 \frac{v_{ip} + V_i}{L_k} + \frac{V_i}{n' L_m}\right] (t - t_3)
+ \left(\frac{n-1}{n}\right) i_{l2} + \frac{i_{l2}}{n} \quad (8)$$

$$i_{l2} = -i_{l2} + \frac{V_{C4}}{L_2} (t - t_4) \quad (9)$$

The current $i_{s1}$ is equal to sum of the current of the inductors $i_{ps}$ and $i_{l2}$ based on Eqs. (8) and (9).

Third Operating Mode ($t_2 \leq t < t_3$):

The equivalent circuit of the proposed converter in this operating mode is shown in Fig. 3(c). When the current of $i_{l2}$ and so the voltage of $v_{l2}$ are equal to zero, the switch of $S_4$ is turned off in ZCS state. The current of the switch $S_1$ is equal to the current of $i_{ps}$ from (8).

Fourth Operating Mode ($t_3 \leq t < t_4$):

The equivalent circuit of the proposed converter in this operating mode is shown in Fig. 3(d). As the voltage $v_{l2}$ is equal to $V_{C4}$, therefore it can be written:

$$i_{l2} = \frac{V_{C4}}{L_2} (t - t_4) \quad (10)$$

The current of $i_{s1}$ is equal to sum of the current of $i_{ps}$ from Eq. (8) and the current of $i_{l2}$ from Eq. (10).

By considering Eqs. (6), (7) and (10) and Fig. 2, it is obtained that:

$$I_{s1} = I_{m2} + \frac{V_i}{n L_m} DT \quad (11)$$

$$I_{s1} = I_{k2} + \frac{(n-1)V_i}{n L_k} DT \quad (12)$$

---

Fig. 1 The proposed bidirectional dc-dc converter with soft switching.

Fig. 2 The waveforms of the proposed converter in the boost operation.
\[ I_{n1} = \frac{V_{C1}}{L_2} \delta T_s \]  

(13)

where \( D \) is the duty cycle and \( \delta T_s \) is the time interval that the auxiliary inductance of \( L_2 \) is charged.

Fifth Operating Mode \((t_5 \leq t < t_4)\):

The equivalent circuit of this operating mode is shown in Fig. 3(e). The capacitor \( C_2 \) is charged and the capacitor \( C_1 \) is discharged. As the time interval of this operating mode is very short, it is possible to consider the current value of the inductors \( i_{L1}, i_{L2} \) and \( i_{L3} \) equal to zero.
to their maximum values as \( I_{s1}, I_{m1} \) and \( I_{s1} \), respectively. Similar to first mode, the time interval of the fifth operating mode \( T_5 \) is calculated as follows:

\[
T_5 = \frac{n(C_i + C_s)V_i}{nI_{s1} + I_{m1} + (n-1)I_{s1}}
\]

(14)

Sixth Operating Mode \((t_6 < t < t_7)\):

The equivalent circuit of this operating mode is shown in Fig. 3(f). The switch \( S_2 \) turn on at ZVS state. The voltage of the inductors \( L_m, L_k \) and \( L_2 \) are equal to \( (V_i - V_H)/n \), \( V_{ip} - V_{lm} \) and \( V_{c4} - V_H \), respectively. Based on auxiliary circuit at the input section of the converter, it is resulted that \( V_{ip} = V_{es} = nV_{lm} = V_i - V_H \). Therefore, it can be written:

\[
i_{m6} = \frac{(n-1)(V_i - V_H)}{nL_m}(t - t_7) + I_{m1}
\]

(15)

\[
i_{s6} = \frac{(n-1)(V_i - V_H)}{nL_k}(t - t_7) + I_{s1}
\]

(16)

\[
i_{ps} = \frac{n}{n} + \frac{i_{m6}}{n}
\]

(17)

\[
i_{s2} = \frac{(V_{c4} - V_H)}{L_2}(t - t_7)
\]

(18)

The current \( i_{s2} \) is equal to sum of the current \( -i_{ps} \) from Eq. (17) and current \( -i_{s2} \) from Eq. (18).

Seventh Operating Mode \((t_7 < t < t_8)\):

The equivalent circuit of this operating mode is shown in Fig. 3(g). This operating mode is started when the current of \( i_{s2} \) and the voltage of \( v_{s2} \) are equal to zero. The switch of \( S_1 \) is turned off in ZCS state. The current of the switch \( S_2 \) is equal to current \( -i_{ps} \) from Eq. (17).

Eighth Operating Mode \((t_8 < t < t_9)\):

The equivalent circuit of this operating mode is shown in Fig. 3(h). As the voltage value of \( L_2 \) is equal to \( V_{c4} - V_H \) so, it is resulted that:

\[
i_{s8} = \frac{V_{c4} - V_H}{L_2}(t - t_8)
\]

(19)

The current \( i_{s8} \) is equal to sum of the current \( -i_{s2} \) from Eq. (19) and current \( -i_{ps} \) from Eq. (17). According to Fig. 2 and by considering Eqs. (15), (16) and (19), it is resulted that:

\[
i_{m8} = I_{m1} + \frac{V_i - V_H}{nL_m}(1-D)T_s
\]

(20)

\[
i_{s8} = I_{s1} + \frac{(n-1)(V_i - V_H)}{nL_k}(1-D)T_s
\]

(21)

\[
-I_{s2} = \frac{V_{c4} - V_H}{L_2} \delta T_s
\]

(22)

2.2 Buck Operating State

The voltage and current waveforms of the proposed topology in buck operating mode are shown in Fig. 4. By comparing Figs. 2 and 4, it is clear that the converter’s waveforms in the buck and boost operating modes are same and only the currents’ direction of \( L_m, L_k \), \( S_1 \) and \( S_2 \) are changed. The equivalent circuits of the converter in buck operating mode are as same as the boost operating mode. Table 1 summarizes the equations of the converter for buck operation.

<table>
<thead>
<tr>
<th>Operating Modes</th>
<th>Equations</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st Mode ((t_1 &lt; t &lt; t_2))</td>
<td>( T_1 = \frac{n(C_i + C_s)V_i}{nI_{s1} + I_{m1} + (n-1)I_{s1}} )</td>
</tr>
<tr>
<td>2nd Mode ((t_2 &lt; t &lt; t_3))</td>
<td>( i_{m3} = -I_{m1} + \frac{V_i}{nL_m}(t - t_3) )</td>
</tr>
<tr>
<td>3rd Mode ((t_3 &lt; t &lt; t_4))</td>
<td>( i_{ps} = \frac{n}{n} + \frac{i_{m3}}{n}, i_{s3} = \frac{(n-1)V_i}{nl_k}(t - t_3) )</td>
</tr>
<tr>
<td>4th Mode ((t_4 &lt; t &lt; t_5))</td>
<td>( i_{s4} = \frac{V_i}{nl_m}(I_{s1} - (n-1)I_{s1}) )</td>
</tr>
<tr>
<td>5th Mode ((t_5 &lt; t &lt; t_6))</td>
<td>( i_{m5} = -I_{m1} + \frac{V_i}{nl_k}(t - t_6) )</td>
</tr>
<tr>
<td>6th Mode ((t_6 &lt; t &lt; t_7))</td>
<td>( i_{s6} = \frac{(n-1)(V_i - V_H)}{nL_m}(t - t_6) )</td>
</tr>
<tr>
<td>7th Mode ((t_7 &lt; t &lt; t_8))</td>
<td>( i_{m7} = -I_{m1} + \frac{V_i}{nl_k}(t - t_7) )</td>
</tr>
<tr>
<td>8th Mode ((t_8 &lt; t &lt; t_9))</td>
<td>( i_{s8} = \frac{(n-1)(V_i - V_H)}{nL_m}(t - t_8) )</td>
</tr>
</tbody>
</table>
Fig. 4 Waveforms for Buck operation.

3 Auxiliary Capacitor Voltage Calculation

By applying the voltage balance law for $L_2$, the following equation is obtained:

$$V_{C4} = (\delta T_s + \delta \alpha T_s) V_{i_2} - V_{i_1}$$

where $\delta T_s$ and $\delta \alpha T_s$ are the time intervals between $t_1$ to $t_2$ and $t_5$ to $t_6$, respectively. By considering the current balance law for $C_4$, we have:

$$\frac{1}{2} (\delta T_s + \delta \alpha T_s) I_{i,2} = \frac{1}{2} (\delta T_s + \delta \alpha T_s) I_{i,1}$$

(24)

Based on Eqs. (23) and (24), the voltage of the capacitor $C_4$ for the buck and boost operating modes is obtained as follows:

$$V_{C4} = \frac{V_i}{2}$$

(25)

By replacing Eq. (25) into Eqs. (13) and (22), the current values of $I_{i,1}$ and $I_{i,2}$ are obtained by:

$$I_{i,1} = I_{i,2} = \frac{V_i}{2L_s} \delta T_s$$

(26)

The current of $i_{L2}$ is independent to the load value, therefore, the voltage of $V_{C4}$ is also independent to the load value.

4 Main Inductor Current Calculation

By applying KCL in Fig. 2, it is resulted that:

$$i_{L1} - i_{L2} = -n I_i$$

(27)

As the average current value of the capacitor $C_1$ is equal to zero and by considering Fig. 1, the value of current $i_{L2}$ is equal to $-i_{L1}$. So, it is resulted that the average values of $i_{L1}$ and $i_{L2}$ are equal to $I_i$. Therefore based on Fig. 2, it can be written:

$$I_i = (I_{i,1} + I_{i,2}) = \frac{I_{i,1} + I_{i,2}}{2}$$

(28)

By replacing the value of current $I_{n2}$ from Eq. (28) into Eq. (11) we have Eqs. (29)-(30). By replacing the value of current $I_{n2}$ from Eq. (28) into Eq. (21) we have Eqs. (31)-(32).

$$I_{n1} = I_i + \frac{V_i}{2nL_m} DT_s$$

(29)

$$I_{n2} = I_i - \frac{V_i}{2nL_m} DT_s$$

(30)

$$I_{k1} = I_i - \frac{(n-1)V_i}{2nL_m} DT_s$$

(31)

$$I_{k2} = I_i + \frac{(n-1)V_i}{2nL_m} DT_s$$

(32)

According to above equations, the input current ripple is equal to:

$$\Delta I_{L1} = I_{i,1} - I_{i,2} = \frac{(n-1)V_i}{nL_m} DT_s$$

(33)

5 Input Current Ripple Elimination

It is pointed out that it is impossible to calculate the input current ripple elimination because the time intervals of the first and fifth operating modes are very short. for second, third and fourth operating modes, the voltage values of the primary and secondary windings of the coupled inductors are equal to $V_i$. As a result it is obtained that:

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is equal to the
in the buck operating
is
from Eq. (42). It is possible to elimi-
(43)
are equal to
1
transformer ratio value as 1
1
current is passed from 1
don. Therefore, at the beginning of the second operating
time of 1
7 ZVS Condition For Main Switches
6 Voltage Gain Calculation
The average value of the inductor \( L_p \) is equal to the
zero based on the balance law in steady state. As a result, the value of voltage gain is calculated as follows:
\[
\frac{V_{g}}{V_{f}} = \frac{1}{1 - D}
\]
(38)

7 ZVS Condition For Main Switches
After the end of first operating mode, firstly the
diode \( D_1 \) is turned on and then the switch \( S_1 \) is turned on.
Therefore, at the beginning of the second operating mode the current of diode \( D_1 \) is positive and the current \( i_{S1} \) is negative. As shown in Fig. 2 and based on the current values at the time of \( t_1 \), the required conditions for the ZVS is obtained as follows:
\[
i_{PS}|_{t_{eq}} - I_{S1} < 0
\]
(39)
\[
T_{dead} < T_{D01}
\]
(40)
where \( T_{dead} \) is the dead time for the switches \( S_1 \) and \( S_2 \) to operate in the ZVS state. \( T_{D01} \) is the reverse bias time of switch \( S_1 \). In this time interval, by decreasing the voltage value of the switch \( S_1 \) to zero, the reverse current is passed from \( D_1 \). By considering the time of \( T_{dead} \) and before the current direction of the inside diodes of the switches \( S_1 \) and \( S_2 \) are changed, the required pulses have to be applied to these switches. In addition, the time interval between \( t_0 \) and \( t_1 \) has to be eliminated because this time interval is very short in comparison with the times of \( T_{dead} \) and \( T_{D01} \). The value of current \( i_{S1} \) in the second operating mode is equal to the sum of \( i_{PS} \) and \( i_{S2} \) from (8) and (9), respectively. As a result, in this operating mode, the minimum value of \( i_{S1} \) based on Fig. 2 is calculated as follows:
\[
\frac{V_{g}}{L_L} - V = \frac{V_{g}}{L_L} - \frac{V_{g}}{L_L} + \frac{V_c}{L_2} - I_{S1} = \frac{n - 1}{n} I_{S1}
\]
(41)
\[
\frac{I_{S2}}{n}
\]
By considering \( T_{dead} = T_f/100 \) in the boost operation state, the ZVS condition for the switch \( S_1 \) is obtained as follows:
\[
\delta T_f > \frac{2L_2(1 - D)P}{n V_f^2}
\]
(42)
\[
\frac{L_2(1 - D)}{n^2} \left( D - \frac{1}{50} T_f \right) \left( \frac{n - 1}{n} \right) \left( \frac{1}{L_2} + \frac{1}{L_{sw}} \right) + \frac{T_f}{100}
\]
In boost performance state and at the end of fourth operating mode the switch \( S_1 \) is turned off. After the time of \( T_f \) which is very short, the diode of \( D_2 \) is turned on and very high current is passed from it. As a result, the ZVS state is always existed for the switch \( S_2 \). Therefore, in boost operation, the ZVS for the switches of \( S_1 \) and \( S_2 \) at the high power is obtained by regulating the time of \( \delta T_f \) from Eq. (42).

Similarly, the ZVS state for switch \( S_2 \) in the buck operating mode is made by the following conditions:
\[
i_{PS}|_{t_{eq}} - I_{S2} < 0
\]
(43)
\[
T_{dead} < T_{D02}
\]
(44)
where \( T_{D02} \) is the time that the main switch of \( S_2 \) is in reverse bias state and its current is passed from diode \( D_2 \). It is possible to eliminate the time interval between \( t_4 \) and \( t_5 \) because this time is very short in comparison with the times of \( T_{dead} \) and \( T_{D01} \). The current of \( i_{S2} \) in the sixth operating mode is equal to sum of the currents \( i_{S2} \) and \( i_{S2} \) from Eqs. (17) and (18). As a result, the minimum value of the current \( i_{S2} \) in the sixth operating mode based on Fig. 5 is calculated as follows:
\[
\frac{V_{g}}{n L_L} - V = \frac{V_{g}}{n L_L} - \frac{V_{g}}{n L_L} + \frac{V_c}{L_2} - I_{S1} = \frac{n - 1}{n} I_{S1}
\]
(45)
\[
\frac{I_{S2}}{n}
\]
By considering \( T_{dead} = T_f/100 \) in the buck operating state, the ZVS state for the switch \( S_2 \) is obtained as follows:

As shown in this figure the performance region of ZVS state for different values of $P_1 = 50 \text{ W}, 100 \text{ W}, 150 \text{ W}$ is different. Moreover, in order to compensate the reduction which is made based on increasing the value of $P_1$, the time interval of $\delta T_s$ for the constant value of $L_2$ has to be increased and or it is possible to decrease the value of inductor $L_2$ for the constant value of time interval $(\delta T_s)$ to obtain the ZVS performance.

In [A18] the ZVS operating conditions for the switches $S_1$ and $S_2$ are obtained by using $T$ equivalent circuit of the coupled inductors and based on the ripple value of the inductor $L_3$. In other word, after the dead time between turning on and off states of two main switches (in this state the voltage of the main switch will be equal to zero because of the charging and discharging the interval capacitors of the main switches), the internal diode of the switch $S_1$ is conducted while its current is positive and required pulses is applied to this switches. After very short time, the switch of $S_1$ is turned on in the ZVS state when the diode current will be zero. In this paper, the current ripple value of the inductor $L_3$ based on the converter circuit parameters is obtained. It is considered that the value of the $\Delta I_3$ has to be high when the value of $I_{j,\text{max}}$ (that is equal to $I_{j,\text{max}}$ for instance in the buck operating mode and for low load) is very big. As shown in the current waveforms of $i_{j_1}$, the current of the inductor $L_1$ consists of ripple in all time intervals and the current ripple value $r_1$ is equal to 40% of the average load current.

In the proposed converter, by determining the parameters of the coupled inductors based on (33), (36) and (37), the required condition for zero input current ripple is obtained. It is important to note that it is possible to obtain ZVS operating state for the main switches of the proposed converter by using auxiliary circuit that consists of auxiliary switches $(S_3, S_4)$, inductor $L_2$ and capacitor $C_1$. According to this condition, (42) and (46) show the ZVS operating state for the power switches in the boost and buck operating modes. In other word, by adjusting the time interval of $\delta T_s$ from Fig. 5, the ZVS operating state is obtained. In the proposed topology as same as presented topology in [A17], the required time for charging and discharging of the parasitic capacitor has to be less than the dead time of the main switches. In this condition, it is possible to turn on the internal diode of these switches when the positive currents are passed from them.

The voltage gain of the proposed topology and presented topology in [18] is as same as the voltage gain of the conventional buck and boost converters. In both...
converters, 4 switches are required. In the presented topology of the attached paper, one the switches of  $S_{s1}$ and or $S_{s2}$ are always turned on (the switch $S_{s1}$ is only turned on in the buck state and the switches $S_{s2}$ is only turned on in the boost state). These switches are lossless. In this topology, two auxiliary switches ($S_{a1}, S_{a2}$) are always turned off in the ZCS state and so their losses are only considered in turning on state of the switches.

Table 2 Comparing the proposed topology with the presented bidirectional converter in [17].

<table>
<thead>
<tr>
<th></th>
<th>Proposed converter</th>
<th>Presented topology in [17]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{V_{in}}{V_{o}}$</td>
<td>$\frac{V_{in}}{V_{o}} \cdot \frac{1-D}{1-D}$</td>
<td>$\frac{V_{in}}{V_{o}} \cdot \frac{1-D}{1-D}$</td>
</tr>
<tr>
<td>$V_{i1}$</td>
<td>$V_{i1} = \frac{V_{in}}{2}$</td>
<td>$V_{i1} = \frac{V_{in}}{2}$</td>
</tr>
<tr>
<td>$V_{o1}$</td>
<td>$V_{o1} = \frac{V_{in}}{2}$</td>
<td>$V_{o1} = \frac{V_{in}}{2}$</td>
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<tr>
<td>$I_{s1}, I_{s2}$</td>
<td>$I_{s1} = I_{s2} = \frac{V_{in}}{2} \cdot \frac{D}{I_{s}}$</td>
<td>$I_{s1} = I_{s2} = \frac{V_{in}}{2} \cdot \frac{D}{I_{s}}$</td>
</tr>
<tr>
<td>$I_{a1}, I_{a2}$</td>
<td>$I_{a1} = I_{a2} = \frac{V_{in}}{2} \cdot \frac{D}{I_{s}}$</td>
<td>$I_{a1} = I_{a2} = \frac{V_{in}}{2} \cdot \frac{D}{I_{s}}$</td>
</tr>
<tr>
<td>$\delta T$</td>
<td>$\delta T_1 &gt; \frac{2L_s(1-D)D}{nV_{i1}^2}$</td>
<td>$\delta T_1 &gt; \frac{2L_s(1-D)D}{nV_{i1}^2}$</td>
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<tr>
<td>$\delta T_1$</td>
<td>$\delta T_1 &gt; \frac{2L_s(1-D)D}{nV_{i1}^2}$</td>
<td>$\delta T_1 &gt; \frac{2L_s(1-D)D}{nV_{i1}^2}$</td>
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<tr>
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<td>$\delta T_1 &gt; \frac{2L_s(1-D)D}{nV_{i1}^2}$</td>
</tr>
<tr>
<td>$\Delta i$</td>
<td>$\Delta i = \Delta i_{a1} = \frac{V_{i1}}{nI_{a1}} DT_s$</td>
<td>$\Delta i = \Delta i_{a1} = \frac{V_{i1}}{nI_{a1}} DT_s$</td>
</tr>
<tr>
<td>$I_{s1} + I_{s2}$</td>
<td>$I_{s1} = I_{s2} = \frac{V_{in}}{2nI_{a1}}$</td>
<td>$I_{s1} = I_{s2} = \frac{V_{in}}{2nI_{a1}}$</td>
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<tr>
<td>$I_{a1}$</td>
<td>$I_{a1} = I_{a2} = \frac{V_{in}}{2nI_{a1}}$</td>
<td>$I_{a1} = I_{a2} = \frac{V_{in}}{2nI_{a1}}$</td>
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</table>

9 Simulation Results

In order to reconfirm the obtained theoretical analyses and capability of making ZVS for the main switches with the zero input current ripple in the proposed topology, the simulation results in PSCAD/EMTDC software program are used in boost operating mode. The simulation results also can be extracted for buck operating mode. The used parameters in simulation considered as $f_s = 50 kHz$, $D = 0.7$, $V_{in} = 24 V$, $L_s = 40 \mu H$, $L_a = 96 \mu H$, $L_4 = 54 \mu H$, $\delta T_s = 1.6 \mu sec$. $C_3 = 200 \mu F$, $C_4 = 21 \mu F$, $R_H = 128 \Omega$, $C_H = 100 \mu F$. The output power is equal to $P_H = 50 W$.

It is possible to stimulate the switches of the proposed topology by using pulse width modulation control method. For instance, the stimulation signal for switch $S_4$ is obtained by comparing the triangle carrier waveform ($A_0$) with the reference waveform ($A_1$) in a way that if $A_1 > A_0$, the value of the stimulation pulse is equal to 1, otherwise it is equal to 0. After generation the fire pulse of the switch $S_4$, the pulse of the switch $S_1$ is generated by applying the delay time equal to $\delta T_s$. The switches $S_1$ and $S_2$ act in a complementary method to the switches of $S_4$ and $S_1$, respectively. The stimulation pulse of the switches based on the pulse width modulation method is shown in Fig. 6. In addition, Fig. 7 shows the used blocks to generate stimulation pulse in the simulation.

There is other method to stimulate switches that has higher accuracy and leads to better performance of the converter. In this method, the phase shifts are considered for the switches pulses in a way that the fire pulses has to be as same as Fig. 2. This method is used in the simulation. The required phase shifts for the switches in the simulation are shown in Fig. 8. In this method, the values of dead times between the switches $S_1$ and $S_2$ in addition to the switches $S_1$ and $S_2$ based on (5), (14) and by considering the value of the parasitic capacitor equal to $C_1 = C_2 = 0.0005 \mu F$ is carefully adjusted. It is possible to consider the dead time equal to $T_{dead} = T_s / 100$.

Fig. 6 Stimulation of the switches based on pulse width modulation method.
Figs. 9(a) and 9(b) show the capability of ZVS for the main switches $S_1$ and $S_2$. As shown in these figures, by turning on the auxiliary diodes of $D_1$ and $D_2$, their voltage ($v_{s1}$ and $v_{s2}$) are equal to zero. In this condition, the trigger pulses of the switches of $S_1$ and $S_2$ are applied before the direction of the currents $i_{s1}$ and $i_{s2}$ have been changed. As a result, the ZVS is made for the main switches. Figs. 9(c) and 9(d) show the capability of the ZCS for the main switches of $S_3$ and $S_4$ in the turning off times. As shown in these figures, the voltage stress for the switches of $S_3$ and $S_4$ are half of the high voltage source ($V_h$) due to existing clamped diodes of $D_3$ and $D_4$.

The voltage and current values of the capacitor $C_4$ in steady state is shown in Fig. 10. According to Fig. 10 and by considering the ripple voltage value of $\Delta V_{c4}$ that is equal to $V_{c4}/100$, it is resulted that:

$$C_4 \frac{\Delta V_{c4}}{\Delta T} = \frac{2s_{i2}}{\delta T_s}$$  (47)

$$C_4 \frac{V_{c4}/100}{2\delta T_s} = \frac{1}{2} i_{s2} \cdot 2\delta T_s$$  (48)

$$C_4 \frac{V_{c4}/200}{2\delta T_s} = \frac{1}{2} i_{s2} \cdot 2\delta T_s$$  (49)

$$C_4 \frac{V_{c4}/200}{2\delta T_s} = \frac{1}{2} V_{c4} \cdot 2\delta T_s \cdot 2\delta T_s$$  (50)

By considering $\delta T_S = 1.6 \mu$sec. and according to the above equation, the value of the capacitor $C_4$ is determined as follows:

$$C_4 \frac{80/200}{2(1.6\mu)} = \frac{80}{2(40\mu F)} (1.6\mu) \cdot 2(1.6)$$  (51)

By simplifying Eq. (51) $C_4$ is obtained equal to $21 \mu F$.

In addition, the value of the capacitor $C_4$ is determined in a way that it is possible to avoid resonance between $C_4$ and $L_2$ while one of the auxiliary switches is turned on. In other word, it is obtained that:

$$T_s > 2T_c$$  (52)

$$f_s > \frac{1}{2\pi \sqrt{L_2 C_4}}$$  (53)

$$C_4 > \frac{1}{40 \mu (50000 \pi^2)} > 1.013 \mu F$$  (54)

The capacitor voltage charging method is shown in Fig. 11.
Fig. 12 shows the transmission current from the input bridge in the boost operating mode. The current of $i_r$ is equal to $-i_{ls}$. According to Fig. 3, the input current of $i_i$ is equal to sum of the currents $i_{ls}$ and $i_r$. As shown in Fig. 12 and based on circuit's parameters, the sum of the currents $i_r$ and $i_{ls}$ is always equal to the constant dc value in the steady state. As shown in Fig. 13, the input current ripple is equal to $i_i = 0.003A$. This value is lower than the input bridge current ripple ($i_{ps} = 4A$). This point shows that it is possible to generate zero input current ripple without making any problem in ZVS and ZCS operating of the switches. This feature is obtained only by regulating the parameters of coupled inductor. In this condition, the value of the input current stress is reduced. As the capacitor and inductor are used in the input bridge, it is necessary to consider the switching frequency of the converter very higher than the resonance frequency ($1/\sqrt{L_s C_s}$) which is made by the resonance between the inductor $L_s$ and capacitor $C_s$. As a result, the switching frequency is considered 5 times higher than the resonance frequency.

The efficiency of the proposed converter for boost operating mode by considering output power of $P_H = 50W$ is equal to $\eta = 0.986$. Fig. 13 shows the efficiency of the proposed converter in the boost operating mode for different output power. As mentioned before, in order to operate the converter at the ZVS state and increase the output power based on constant value of $\delta T_s$, the value of the inductor $L_s$ has to be decreased or based on the constant value of $L_s$ the value of $\delta T_s$ has to be decreased (According to Fig. 5). In this section, by considering the constant value of $\delta T_s = 1.6 \mu s e c.$ and by increasing the output power, the value of the inductor $L_s$ is only decreased. As shown in Fig. 13, the efficiency of the converter is higher than 98% for the power higher than 40 W. The values of the selected $L_s$ for using different powers in the ZVS operating modes of the converter are shown in Table 3.

**Table 3** The values of the inductor $L_s$ for different output power.

<table>
<thead>
<tr>
<th>$P_H$ (W)</th>
<th>$L_s$ (μH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>100</td>
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<tr>
<td>80</td>
<td>80</td>
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<td>70</td>
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<tr>
<td>20</td>
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</table>

Fig. 13 The efficiency of the proposed converter based on different output power.

10 Conclusion

In this paper, a new dc-dc buck-boost converter with the capability of soft switching and zero input current ripple is proposed. In this topology, ZVS for the main switches of $(S_1$ and $S_2)$ and ZCS for the auxiliary switches $(S_3$ and $S_4)$ are always made. The circulating current is reduced because of operating the lossless active snubber. The proposed Topology in comparison with the conventional Topologies such as poly-phase needs lower number of elements to eliminate the input current ripple. The required conditions for soft switching operating mode and also for eliminating the input current ripple are obtained. Moreover, the equations of the voltage and current of all elements of the proposed topology are calculated in all operating modes. Finally, the correct operation of the proposed topology and also the given theoretical are reconfirmed by simulation results by using PSCAD/EMTDC software.

References


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