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Research Paper

# **Optimal Multiple FCLs Allocation Considering DG Penetration in Meshed Network With Multi-Level Voltages**

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**Abstract:** Increasing the short circuit current due to the penetration of distributed generations (DGs) in various voltage levels and meshed topology is a basic problem in power systems. Using fault current limiter (FCL) is an efficient approach to mitigate the exceeded short circuit levels. In this paper, a new approach is presented for multiple FCLs locating to decrease short circuit levels in meshed networks with several subsystems and multi-level voltages. Modified hybrid genetic algorithm (GA) and sensitivity analysis (SA) are used to determine the type, number, location, and voltage level of FCLs. Also, an effective sensitivity index is proposed, which can reduce the search space for optimal allocation. This method suggests the optimal allocation with the least investment cost in multi-level voltages networks according to the FCL costs. The proposed method is evaluated in the IEEE 30-bus, 57-bus, and 300-bus test systems. Numerical results indicate the accuracy and efficiency of the proposed method.

Keywords: Fault Current Limiter, Short Circuit Current, Allocation, Distribution Generation.

#### 1 Introduction

**C**ONTROL of fault currents level in different points of the network is inevitable, due to the expansion of interconnected networks and high penetration of distributed generation resources (DGs) in power systems. There are important effects of DG penetration in meshed networks, including changing direction and magnitude of fault currents in different points of the network. These issues and increasing the short circuit currents higher than breaking capacity of circuit breakers (CBs) and affecting the protection coordination make the network planners upgrade the equipment and re-coordinate the protective devices.

Fault current limiter (FCL) is an applicable approach to limit the exceeded short circuit currents to acceptable level in different points of the network. This device can mitigate the magnitude of fault current and improve the security and reliability of the power system and facilitate the conditions for the restoration of protective relay coordination. Therefore, with locating FCLs optimally, the equipment that need to be either replaced or upgraded is minimized and postpone new investments to upgrade the system. Considering development of technology in the field of fault current limiters in recent years, more advanced FCLs have been designed and manufactured with distinguished features. Negligible losses during normal condition and applying maximum fault current limitation with the capability of fault detection are some of these features. Among the important FCLs are Superconducting Fault Current Limiters (SFCLs) which consist of superconducting elements, Solid State Fault Current Limiters (SSFCL) which consist of power electronic equipment, and Magnetic Fault Current Limiters (MFCL) [1, 2].

Considering the role of FCL in various studies, many articles have focused on a variety of goals in FCL locating; such as fault current reduction, relay coordination, reliability, stability, and economic issues.

In [3] and [4], FCLs are used to decrease the fault currents magnitude in different points of a system to bearable level for CBs. Also, some studies have minimized the number as well as impedance of required FCLs for mitigating short circuit levels in the

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distribution system [5-7].

Protection coordination can be affected, as well, by the integration of DG. Therefore, the best FCL location with the least impedances has been determined, considering the overcurrent relays coordination with minimum total operation times [8-10]. Furthermore, some references have considered the impact of FCL on network reliability [11, 12]. Since increasing short circuit level has a considerable impact on both availability and failure rate of CBs directly, the impact of FCL on reliability has been analyzed for CBs [13] and reliability of transmission and switching substations [14, 15]. Also, some articles have evaluated the economic benefits of the FCL application. In [16] and [17], the effect of FCL has evaluated on the operation costs of the system. In these references presented analysis is based on the comparison of investment and generation costs of the system with and without FCL. In this regard, in [18] a method based on GA is proposed to determine the number, location, and impedance of FCL for reducing the costs of distribution network protection.

Generally, the major computational methods for locating the FCLs can be classified into two categories: sensitivity analysis (SA) and intelligence techniques. Many studies have used sensitivity analysis to locate the FCLs. Sensitivity index has a significant role in the optimality of the final solution. The indices, such as fault current variation due to changing FCL impedance [5, 11, 13], power changing index [19], rotor's angle index of generator instability studies [20], reliability index [21], and protective coordination indices [22] are mostly used to determine the optimum FCL parameters. Moreover, in many studies computational intelligence techniques are used; e.g. genetic algorithm (GA) [23] and [24], particle swarm optimization (PSO) [12, 25], and a combined of heuristic methods [7, 26]. In addition to these categories, the other non-linear methods have also been used to FCL locating in some references such as [6, 8].

Considering the investment cost in optimal locating of FCLs is important; so that, in addition to the type and impedance size, the installation and maintenance costs of FCLs depend on its location and voltage level directly. Limitations of space and cost of FCL location could have effects on optimal FCL allocation in meshed networks from the economical point of view. Therefore, new techniques are needed and essential to determine the minimum required FCLs that could be installed with the least investment cost. On the other hand, in meshed networks with different voltage levels, DGs with various ratings could be connected to the grid, which leads to change the fault currents and short circuit levels. The fault currents may flow from different paths of another voltage level to the fault point in the multilevel voltages network with DG penetration. Hence, sometimes FCL installation at another voltage level is required to reduce the short circuit levels or mitigate the fault current contribution of DG in other voltage levels. Therefore, in multiple FCL allocation, it is necessary considering the FCL installation in all subsystems with different voltage levels, because the lower costs may be imposed to the network planner for controlling of short circuit levels at all the subsystems.

In this paper, a Hybrid Genetic Algorithm and Sensitive Analysis (HGASA) method is presented to locate the FCLs optimally in multi-level voltages and meshed networks considering DG penetration with various rated capacities and the DGs at all voltage levels are assumed the synchronous-based DG. A main feature of the proposed method is the iterative-based process for assigning and increasing the FCL impedance in various points of the network. The cost function with fixed and variable terms based on different locations and voltage levels is used; so that, all exceeded short circuit levels are mitigated with the lowest investment cost. Also, an efficient sensitivity index is defined to reduce the search space of GA and calculation burden purposefully. Generally, the proposed method, using a combined genetic algorithm and sensitivity analysis, performs an iterative-based allocation for FCLs in multi-level voltages systems.

### 2 DGs Penetration and FCL Installation

In the last two decades, with an impressive growth of DGs technology the behavior of these resources including the fault current contribution and short circuit levels have been changed. This has led planners to pay more attention to the consequences of DGs penetration. Reconfiguration of networks to multiple-fed and meshed topology and changing impedance matrix are among the consequences of DG penetration. This generally increases the fault currents and sometimes it may increase the short circuit levels to more than CBs breaking capacity. DG connection with different ratings in all subsystems with different voltage levels is done according to the regulated instructions and technical constraints in different points of the grid.

DGs may be connected to subsystems with different voltage levels according to their type and rating capacity. A typical instruction and scheme of DG connection to the network are shown in Fig. 1 (instruction of DG connection to the distribution network in Iran [27]). DGs are categorized into five classes according to their nominal capacity and voltage level, which is shown in Table 1. With the connection of each DG in the new bus, one row and one column added to the network impedance matrix. For more DGs penetration, the changes of the impedance matrix have been increased. Also, with high penetration of DGs, the short circuit levels are increased in all points of the network. With increasing the fault current levels, some buses may expose to critical condition. The contribution of each DG to elevate the short-circuit levels in critical buses; depends on the rating and location of DG.



Fig. 1 Typical schemes for DG connection to the network subsystems.

Table 1 Classification of distributed generations based on their connection schemes.

Class	1	2	3	4	5
Nominal power	Up to 20 kW	20-200 kW	200-1000 kW	1-7 MW	7-25 MW
Scheme 1	$\checkmark$				
Scheme 2	$\checkmark$	$\checkmark$			
Scheme 3		$\checkmark$	$\checkmark$	$\checkmark$	
Scheme 4				$\checkmark$	$\checkmark$
Scheme 5					~

The FCL with non-linear impedance is used for controlling fault current levels in power systems which has low impedance at the normal condition and increases its impedance when a fault occurs. Considering the FCL impedance seen by fault current, FCLs could be categorized into three groups: resistive (RFCL), inductive (XFCL), and combination of them (ZFCL). Furthermore, the positions of FCL can be divided into two major categories in the network. FCL installation in series on feeder lines that is one of the most common uses of this device, for mitigating of fault current. Also, the FCL installation series with DG that is a way to reduce the fault current contribution of DG to the network. As shown in Fig. 2, all transmission or feeder lines and DG connection point to the grid with any voltage level at each subsystem are among the candidate locations for installing the FCLs.

## **3** Proposed Method and Formulation

In the proposed method the multiple FCLs allocate in all candidate locations to mitigate the exceeded short circuit level in all critical buses due to DG penetration. The proposed method determines the type, number, impedance size, location, and voltage level of required FCLs; so that, imposes the least cost for installing FCLs according to the FCL costs. The procedure of FCL locating is an iterative-based manner. The impedances of FCLs increase in the best locations among all the candidate locations during the multi-stages of the proposed method; until satisfying all technical constraints. At each stage the best location for FCL installation is determined using the sensitivity analysis. Therefore, the proposed method suggests an optimum route for installing the FCLs impedances in the best locations.



Fig. 2 Candidate locations for FCL installation in the network subsystems.

#### 3.1 Objective Function and Constraints

An objective function is defined as follows to consider both fixed and variable costs of FCL, which depend on the type, size, location, and voltage level of FCLs:

$$\min J = \sum_{V=1}^{N^{\vee}} \sum_{L=1}^{N^{\perp}} \left[ FC_{R}^{L} + \left( IC_{R}^{V} \cdot R_{FCL}^{L} \right) \right] + \left[ FC_{X}^{L} + \left( IC_{X}^{V} \cdot X_{FCL}^{L} \right) \right]$$
(1)

where the objective function is the total cost of multiple FCLs installation in the network with  $N^{\nu}$  voltage levels and  $N^L$  candidate locations. In addition,  $R_{FCL}$  and  $X_{FCL}$ are per-unit impedances of resistive and inductive FCLs, respectively. FC is the fixed cost of FCL installation which consists of the cost for procurement of location and related equipment; depend on FCL type and installation location. Distribution and urban networks have more space limitations than other parts of the system. Also, IC is the incremental cost of an FCL that depends on its impedance, which directly affects the investment and maintenance costs. The incremental cost is expressed as per-unit of FCL impedance, based on its type and voltage level. Furthermore, the reduction of fault currents to allowable ones is considered as technical constraints in the proposed method:

$$I_{f,j} \le I_{f,j}^{\max}$$
  $j = 1, 2, ..., N_{bus}$  (2)

At all buses with any rated voltage, the magnitude of fault current that is shown with  $I_f$ , should be lower than bearable fault current by CBs ( $I_f^{max}$ ). The magnitude of fault current at bus j is calculated according to (3) based on three-phase short circuit calculations in each bus, as the worst-case:

$$I_{f,j} = \frac{V_j}{Z_{jj}} \tag{3}$$

where,  $V_j$  and  $Z_{jj}$  are the pre-fault voltage and Thevenin equivalent impedance of *j*-th bus, respectively.  $Z_{jj}$  is *j*-th diagonal element of the impedance matrix. Adding the FCL with  $\Delta Z_{FCL}$  impedance to the best location at each stage, will change the impedance matrix and short circuit levels, subsequently. Therefore, Thevenin equivalent impedances of buses should be updated after adding the  $\Delta Z_{FCL}$  at each stage. The FCL with impedance  $\Delta Z_{FCL}$  that is installed in series in *L*-th line with impedance  $Z_L$  (transmission line or DG feeder line) can be modeled as equivalent impedance  $Z_P$ , in parallel with impedance  $Z_L$  [7]:

$$Z_{P} = -\frac{Z_{L} \left( Z_{L} + \Delta Z_{FCL} \right)}{\Delta Z_{FCL}} \tag{4}$$

while the FCL with impedance  $\Delta Z_{FCL}$  has been added to the line *L*, located between buses *k* and *m*, the changes in Thevenin equivalent impedance of *j*-th bus can be calculated as follows:

$$\Delta Z_{jj} = -\frac{(Z_{jk} - Z_{jm})^2}{Z_{kk} + Z_{mm} - 2Z_{km} + Z_p}$$
(5)

where  $Z_{jk}$ ,  $Z_{jm}$ ,  $Z_{kk}$ ,  $Z_{mm}$ , and  $Z_{km}$  are the elements of impedance matrix, before adding the FCL to line *L*. Thevenin equivalent impedance of *j*-th bus is updated due to installing FCL as follows:

$$Z_{jj}^{new} = Z_{jj}^{old} + \Delta Z_{jj} \tag{6}$$

Therefore, fault current reduction in j-th bus, due to installing FCL in line L, can be calculated as follows:

$$\Delta I_{f,j} = \frac{V_j}{Z_{jj}} - \frac{V_j}{Z_{jj} + \Delta Z_{jj}}$$
(7)

#### 3.2 Genetic Algorithm and Sensitivity Analysis

In the proposed method optimal routes to adding the FCLs in different location of the network is searched by genetic algorithm purposefully. The cost function is considered as the fitness function and typical chromosome string in GA is shown in Fig. 3. Producing



Fig. 3 Producing a scenario or route to install multiple FCLs using a string of chromosome and sensitivity analysis.

of each chromosome is completed stage by stage and randomly which produces a route to adding FCLs with impedance  $\Delta Z_{FCL}$  at different points of the grid, finally.

In each stage after determining the type, size, and location of FCL, technical constraints are checked. If constraints are not satisfied, adding FCL with new type, size, and location will continue in the next stage, otherwise, adding FCL is terminated. This procedure continues until satisfying all constraints. Next, the fitness of each possible route is calculated according to the cost function. In the following, by applying GA operators, the feasible solutions in the next generations are searched.

Since the sensitivity analysis has a significant role in the optimality of the final response, an efficient sensitivity index is defined to prioritize the best locations and voltage levels for FCLs. It is assumed that after short circuit calculations, N<sub>h</sub> critical buses have short circuit levels more than the breaking capacity of CBs. The per-unit deviation from maximum short circuit level for *j*-th critical bus ( $\Delta I_j^{\text{Margin}}$ ), is determined as follows:

$$\Delta I_{j}^{\text{Margin}} = \frac{I_{f,j} - I_{f,j}^{\text{max}}}{I_{f,j}^{\text{max}}}$$
(8)

This parameter is positive for critical buses and represents the criticality level of them. Moreover, the amount of reduction in short circuit current in *j*-th critical bus due to adding  $\Delta Z_{FCL}$  in line *L* is calculated as follows:

$$\Delta I_{j,L}^{\text{Reduction}} = \frac{I_{f,j} - I_{f,j}^{\Delta Z_{FCL,L}}}{I_{f,j}}$$
(9)

where  $I_{f,j}$  and  $I_{f,j}^{\Delta Z_{PCL,L}}$  are the magnitudes of fault current in *j*-th bus before and after addition of  $\Delta Z_{FCL}$  in *L*-th line, respectively. In the following, the sensitivity index of Average Decrease of Fault Current (ADFC) is defined and calculated for all possible locations of FCL installation. This index represents the average reduction of fault currents in all critical buses, due to installing FCL in line *L*:

$$ADFC_{L} = \frac{\sum_{j=1}^{N_{h}} \left[ \left( \Delta I_{j,L}^{\text{Reduction}} \right) \times \left( \Delta I_{j}^{\text{Margin}} \right) \right]}{N_{h}}$$
(10)

In this index, the amount of deviation from the allowed short circuit level, is considered as the degree of importance for fault current reduction in critical buses. In other words, the reduction of fault current magnitude in the critical bus with more deviation has higher importance. In each stage of the proposed method, the sensitivity analysis is performed and a prioritization is determined for all locations according to the ADFC index. Larger sensitivity index for a location means more effective in reducing fault currents in all critical buses based on their criticality level.

As can be seen, in Fig. 3, at each stage, when the type

and size of  $\Delta Z_{FCL}$  are determined randomly, the ADFC index is calculated for all possible locations. The location with the highest ADFC is selected as the best location for adding the  $\Delta Z_{FCL}$  at each stage. However, in order to search a larger space, proportion to ADFC index, a weighting coefficient is assigned to each candidate location and FCL location is determined through the Roulette Wheel method. The weighting coefficients for all location are calculated at each stage as follows:

$$\omega_{FCL}^{L} = \frac{1}{R_{FCL}^{\max} X_{FCL}^{\max}} \left( \sum_{R_{FCL}=0}^{R_{FCL}^{\max}} \left( \sum_{X_{FCL}=0}^{X_{FCL}^{\max}} ADFC_{L} \right) \right)$$
(11)

where this coefficient represents the average of calculated ADFC indices per all impedances of resistive and inductive FCL in *L*-th line. Generally, in the location with a higher weighting coefficient, installation of FCL (including resistive and inductive impedance with any size), will be obtained the higher ADFC indices averagely. Therefore, the selection probability of any location for FCL installation can be calculated as follows:

$$P_{FCL}^{L} = \frac{\omega_{FCL}^{L}}{\sum_{L=1}^{N^{L}} \omega_{FCL}^{L}}$$
(12)

Consequently, when size and type of FCL are determined according to chromosome string, voltage level and location are selected through sensitivity analysis and Roulette Wheel. Then impedance  $\Delta Z_{FCL}$  is added to the selected location and updated the FCL impedances at each stage:

$$Z_{FCL,L}^{new} = Z_{FCL,L}^{old} + \Delta Z_{FCL,L}$$
(13)

where  $\Delta Z_{FCL,L}$  is per-unit impedance of FCL which is added to location *L*, at each stage. This procedure continues until the short circuit level in all critical buses decreases to the allowed level. In this condition, a route to adding the FCL to the grid is created per each chromosome, consequently. Flowchart of multiple FCLs allocation algorithm includes load flow, short-circuit calculations and the combination of GA and SA in the proposed method is shown in Fig. 4.

#### 4 Case Studies and Results

In order to evaluate the proposed algorithm, FCLs with any type, size, and voltage level are considered at all possible locations of the test systems. According to presented data about FCL costs in [6] and the economic review carried out in [1, 28, 29] for different types of FCL, the costs of FCLs based on their types and voltage level are summarized in Table 2. Three case studies with different topologies and voltage levels are used in order to test and evaluate the proposed method and compare with other studies.



Fig. 4 Flowchart of the proposed multiple FCLs allocation algorithm (HGASA).

	Fixed c	ost (FC)	Incremental cost (IC)		
Voltage [kV]	[milli	on \$]	[millior	n \$/p.u.]	
	RFCL	XFCL	RFCL	XFCL	
330 - 420	0.80	0.85	0.70	0.60	
220 - 330	0.80	0.85	0.70	0.60	
130 - 220	0.70	0.75	0.50	0.40	
80 - 130	0.60	0.65	0.35	0.25	
40 - 80	0.50	0.55	0.30	0.20	
20 - 40	0.40	0.45	0.15	0.10	
10 - 20	0.30	0.40	0.10	0.08	
< 10	0.20	0.30	0.10	0.08	

#### 4.1 IEEE 30-Bus Test System

In the first step, in order to evaluate the proposed method, it is assumed that the maximum tolerable fault current by the CBs on all 33kV buses of the IEEE 30-bus test system (Fig. 5), without the DGs penetration to be 10kA. So, in order to reduce the fault currents to less than 10kA, the FCLs are located in the network. The critical buses and per-unit deviation of fault current magnitude ( $\Delta I_j^{\text{Margin}}$ ) in all of them are shown in Table 3, considering the maximum 10kA for allowable fault current.

In order to multiple FCLs allocation, the ADFC index and weighting coefficient for different types of FCLs (XFCL and RFCL) in the first stage are calculated and shown in Fig. 6. These coefficients indicate the proper lines for FCL installation to reduce the short circuit level of all critical buses. As previously mentioned, a probability selection has been assigned to all the lines. These probabilities are calculated in the process of selecting the best location for  $\Delta Z_{FCL}$  at each stage according to (12). These indices and coefficients will be updated in the next stages.

It can be seen that during the first stage, the lines of 16, 14, and 15 have the highest sensitivity index among all the lines, respectively. Considering the fixed and incremental costs, the results of multiple FCLs allocation by the proposed HGASA method are indicated in Table 4.



Table 3 l	Deviatior	n of faul	t current	in critic	al buses	•
Critical bus	10	12	15	17	21	22
$\Delta I_{j}^{\mathrm{margin}}$ [p.u.]	0.59	1.16	0.19	0.10	0.16	0.15



Fig. 6 Sensitivity analysis for various FCL impedances in all 33kV lines; a) Sensitivity index ADFC and b) Weighting coefficients of FCL installing at the first stage.

Table 4 Results of inductive and resistive FCLs allocation considering the fixed and incremental costs in the 30-bus test system.

Line 14	Line 16	N	$\Sigma_{\mathbf{Z}}$ [m m ]	Cost [million \$]	
$R_{\rm FCL}$ [p.u.]	$R_{\rm FCL}$ [p.u.]	IVFCLs	$\Delta \mathbf{Z}_{FCL}$ [p.u.]	Cost [minion \$]	
0.42	0.81	2	1.23	0.965	

**Table 5** Results of inductive and resistive FCLs allocation considering the incremental costs only in the 30-bus test system.

Line 14	Line 15	Line 16	Maar	$\Sigma Z_{\text{part}}$ [p 11]	Cost [million \$]	
$X_{\rm FCL}$ [p.u.]	$X_{\rm FCL}$ [p.u.]	$R_{\rm FCL}$ [p.u.]	IVFCL	ZZFCL [p.u.]		
0.31	0.15	0.41	3	0.87	0.1167	



Fig. 7 Inductive FCL allocation; a) ADFC index for inductive FCLs and b) Fault current magnitudes in 33kV buses before and after inductive FCLs allocation.

As shown, locating two resistive FCLs in lines 14 and 16 is the optimal technical and economic solution to satisfying the technical constraints, which consequently, imposes lower costs to the planner (0.965 million dollars). Therefore, for reducing of short circuit level in critical buses, only two RFCLs are required by applying the proposed method.

Generally, increasing the fixed cost in the proposed method leads to a reduction in the number of FCLs, whereas considering the incremental cost reduces total impedance for located FCLs. As shown in Table 5, without considering fixed cost, the total impedance of FCLs would significantly reduce. That being said, this leads to minimizing the total impedance of FCLs. In fact, when the incremental cost of FCLs is increased, the program's output would be more sensitive to minimizing the total impedance of FCLs. As seen, in these conditions, the total impedance required for two XFCLs and one RFCL is 0.87 per-unit. This imposes the approximate cost of 0.117 million dollars to the network planner for limiting the short circuit levels to 10kA.

It is worth noting that some references have also reduced the critical fault currents to less than 10kA, by locating and installing the XFCLs only in this case study [5, 6]. In order to evaluate the proposed method, the results are compared with these references. In order to multiple XFCLs allocation, as illustrated in Fig. 7(a) the ADFC indices are calculated for XFCLs in the first stage. Also, weighting coefficients proportional to the average ADFC index are shown in Table 6. As can be seen, in the first stage, line 16 has the highest probability of selection; since it has the highest weighting coefficient among all the lines.

Finally, the results of multiple XFCLs allocation obtained from the proposed method are shown in Table 7. In this table the results are compared with the presented method in [5] and [6]. Also, the short circuit level in 33kV buses after and before the XFCL installation is illustrated in Fig. 7(b). The proposed HGASA method locates three XFCLs at minimum cost to limit the fault currents to 10kA. The proposed method has located fewer XFCL with less cost as a technical and economic solution. This shows the accuracy of the iterative HGASA method, comparing to the other methods. The proposed method provides a more precise solution relatively, which is due to the gradual (step by step) installation of XFCL impedance ( $\Delta X_{FCL}$ ) to the network during the iterative proposed method. Furthermore, considering the fixed and variable costs of XFCL causes the fewer costs are imposed on the network planner.

In order to investigate the impact of FCL type on allocation problem, the effect of installing the FCL in line 16 on the ADFC index and fault current reduction of the most critical bus, i.e. bus 12, is illustrated in Fig. 8. According to Fig. 8(a), installing the XFCL with up to 0.2645p.u. has more influence in increasing the ADFC index, comparing to the RFCL, whilst for impedances higher than this value, the RFCL decreases the fault currents of all critical buses and increases the ADFC index more efficiently, comparing to the XFCL. As shown in Fig. 8(b), installing and increasing the size of XFCL in line 16 reduces the short circuit current in bus 12 significantly. As shown in Fig. 8(b), installing and increasing the size of xFCL in line 16 reduces the short circuit current in bus 12 significantly. As shown in Fig. 8(b), installing and increasing the size of XFCL in line 16 reduces the short circuit current in bus 12 significantly. However, this procedure follows a non-linear curve and declines gradually, so that increasing the XFCL has a negligible effect on reduction of short circuit current finally.

On the other hand, increasing the RFCL in line 16 has an inconsiderable effect on reduction of short circuit current in bus 12 initially. But in the following, with increasing the RFCL impedance, the rate of reduction increases. As shown, for specific impedance (0.2756p.u.) in crossing point, the effect of FCL type in fault current reduction in bus 12 is similar. Generally, increasing the impedance size based on the FCL type has a non-uniform and different effect on reducing the short circuit currents of critical buses and improving ADFC index. In fact, increasing FCL's size and its influence on reducing short circuit levels in any position follows a non-linear relation that depends on the FCL type and system parameters.

le 6 Weig	hting coef	ficients of	inductive	FCLs inst	allation in the	first stage.	
From	bus		To bus		$\omega^{l}_{X-SFCL}$	P	X-SFCL
12			13		0.1132	0.	2478
9			10		0.0683	0.	1495
4			12		0.0429	0.	0940
10			17		0.0290	0.	0636
12			15		0.0236	0.	0517
Table 7 R	Results of i	nductive I	FCLs alloc	ation in th	e 30-bus test s	ystem.	
	Lines v	vith X-FC	L [p.u.]		λ7	$\nabla V$ [ ]	Cost function
12	14	15	16	26	IVX-FCLs	$\Delta X_{\rm FCL}$ [p.u.]	[million \$]
0.8	1	0.6	0.7	0.8	5	3.9	2.568
-	0.33	0.29	0.43	-	3	1.05	1.386
-	0.36	0.24	0.39	-	3	0.99	1.378
0.5 0.6 edance in Line	> XFCL ZFCL 0.7 0.8 16 [p.u.]	8 0.9		22 Fault current in Bus 12 [kA] 19 10 10 10 10 10 10 10 10 10 10 10 10 10	0.1 0.2 0.3 0.2756	L ZFCL 0.4 0.5 0.6 0.7 FCL in Line 16 [p.u.]	0.8 0.9 1
	le 6 Weig From 12 9 4 10 12 Table 7 F 12 0.8 - - - - - - - - - - - - -	$\frac{10}{12} = 6 \text{ Weighting coef} From bus}{12} = 9$ 4 10 12 $\frac{14}{10} = 7 \text{ Results of i} = 12$ 14 0.8 1 - 0.33 - 0.36 $\frac{1}{2} = 0.36$	le 6 Weighting coefficients of         From bus         12       9         4       10         12       10         Table 7 Results of inductive I         Lines with X-FC         12       14         15       0.8         0.8       1       0.6         -       0.33       0.29         -       0.36       0.24	le 6 Weighting coefficients of inductive         From bus       To bus         12       13         9       10         4       12         10       17         12       15         Table 7 Results of inductive FCLs alloc         Lines with X-FCL [p.u.]         12       14         12       14         13       0.6         0.8       1       0.6         0.33       0.29       0.43         -       0.36       0.24       0.39	le 6 Weighting coefficients of inductive FCLs inst         From bus       To bus         12       13         9       10         4       12         10       17         12       15         Table 7 Results of inductive FCLs allocation in the         Lines with X-FCL [p.u.]         12       14         12       14         15       16         26       0.8         1       0.6       0.7         0.33       0.29       0.43         -       0.36       0.24       0.39         -       0.36       0.24       0.39         -       0.36       0.24       0.39         -       0.36       0.9       1         10       1       1       1         10       0.7       0.8       -         -       0.36       0.24       0.39       -	de 6 Weighting coefficients of inductive FCLs installation in the From busFrom busTo bus $\omega'_{X-SFCL}$ 12130.11329100.06834120.042910170.029012150.0236Table 7 Results of inductive FCLs allocation in the 30-bus test sLines with X-FCL [p.u.]NX-FCLs121415160.810.60.70.810.60.7-0.360.240.393	le 6 Weighting coefficients of inductive FCLs installation in the first stage.         From bus       To bus $\omega^{I}_{X:SFCL}$ P         12       13       0.1132       0.         9       10       0.0683       0.         4       12       0.0429       0.         10       17       0.0290       0.         12       15       0.0236       0.         Table 7 Results of inductive FCLs allocation in the 30-bus test system.         Lines with X-FCL [p.u.]       Nx-FCLs $\Sigma X_{FCL}$ [p.u.]         0.8       1       0.6       0.7       0.8       5       3.9         -       0.36       0.24       0.39       -       3       0.99

Fig. 8 Sensitivity analysis of increasing FCL impedance in line 16; a) ADFC index improvement in line 16 and b) Changes of short circuit current magnitude in bus 12.

According to the network parameters such as high  $X_1/R_1$  ratio in 33kV subsystem of the IEEE 30-bus test system, installing the XFCL in low-sized, has a considerable effect on reducing the magnitude of fault current, while in high-sized FCL installation, more fault current limitation and high ADFC index be achieved with RFCLs. The different behaviors of inductive and resistive FCLs are due to their different influence on magnitude and phase of fault current. Generally, adding FCL to the network not only reduces the fault current magnitude, but also changes the phase angle of fault current based on the FCL parameters such as type, size, and location.

As shown in Fig. 9(a), *j*-th critical bus can be connected to the network through some lines and should be installed an FCL on one of them to decrease the short circuit level. Also, as illustrated in Fig. 9(b), critical bus may be fed with one or more DGs that FCL is required in DG feeder line to mitigate the fault current contribution of DG. However, DG parameters such as size, location, and type of DG, influence the share of DG in total fault current. As shown in Fig. 9, assuming that the FCL is installed on the *m*-th line, it can be expressed:

$$I_{f,net} = \sum_{l=1}^{n} I_{f,l}$$
(14)

$$I_{f,j} = I_{f,net} + I_{f,m}$$

$$\tag{15}$$

$$I_{f,j} = I_{f,net} + I_{f,FCL}$$
or
$$I_{f,j} = I_{f,net} + I_{f,DG\&FCL}$$
(16)

The phasor diagram of changing the fault current magnitude and phase angle due to installing FCL in the transmission line and DG feeder line is shown in Fig. 9(c). In the phasor diagram, the horizontal axis, which represents the voltage angle of bus *j*, is assumed as the reference axis. Installed FCL in the *m*-th line will change the phase angle difference between fault current flow from *m*-th line  $(I_{f,m})$  and resultant fault currents flowing from other lines to bus j ( $I_{f,net}$ ). Therefore,  $I_{f,net}$ has a phase difference ( $\alpha$ ) with the FCL-equipped line's fault current, as shown in Fig. 9(c). The current  $I_{f,m}$ according to FCL location equal to  $I_{f,FCL}$  or  $I_{f,DG\&FCL}$ . Angle  $\alpha$  depends on the type and size of FCL. For short circuit level mitigation of faulty bus *j*, the resultant of all fault currents flowing to bus j should be reduced. The phase angle of the fault current flows through the line L to the critical bus j, related to the reactance to resistance ratio  $(X_L/R_L)$  of line viewed from the critical bus j. However, other factors, including the voltage angle and impedance of fault, influence the phase angle of fault current. Assuming the voltage phase angles of the buses are approximately equal, in a highly inductive network, i.e. high  $X_L/R_L$  ratio, the fault currents are



Fig. 9 FCL locations and change of fault currents due to XFCL and RFCL installation; a) FCL in the transmission line, b) FCL DG feeder line, c) Phasor diagram of fault currents changes due to XFCL and RFCL, and d) The changing of fault current phasor in bus 12 due to XFCL and RFCL installation in line 16.

closer to the vertical axis. It is assumed that without FCL installation, the currents  $I_{f,net}$  and  $I_{f,m}$  have the same phase angle. The changes in currents  $I_{f,m}$  and  $I_{f,j}$  due to FCL installation and its impedance increasing are shown in the phasor diagram.

As shown, increasing the XFCL impedance in lowsized, has a considerable effect on reducing the magnitude of fault current in the critical bus. However, it has little impact on the phase angle of the fault current. Whereas, the high ratio of  $X_L/R_L$  causes the lowsized RFCL, have no significant effect on reducing the fault current magnitude. Although it has a great impact on increasing the phase angle difference between currents  $I_{f,FCL}$  and  $I_{f,net}$ . In this regard the phasor diagram of fault current changes in bus 12 due to XFCL and RFCL in line 16 is shown in Fig. 9(d) that confirms this analysis. As shown, with the high-sized RFCLs, more limitation for fault current is achieved, comparing to the XFCLs. In inductive network RFCLs have a more effective role in increasing the phase angle  $\alpha$ . In general, according to the short circuit calculations, adding the FCL with impedance ZFCL to the line that is connected to the bus *j* makes a change in phase angle of the fault current, which can be formulated as follows:

$$\tan \theta = \frac{X_{h,m} + X_{FCL}}{R_{h,m} + R_{FCL}}$$
(17)

where,  $X_{th,m}$  and  $R_{th,m}$  are equivalent reactance and resistance seen by the FCL-equipped line, respectively, and  $\theta$  is the phase angle of the fault current. Among FCLs with lower impedances, XFCLs have a more effective role in reducing fault current magnitude. Nevertheless, among FCLs with higher impedances, RFCLs are more effective in changing angle  $\theta$ , increasing angle  $\alpha$ , and reducing the short circuit level in the critical bus. Also, regarding (17) and phasor diagram, it is evident that for small impedances, the inductive FCL causes the phase angle of DG fault current to reach the near of 90 degrees. While resistive FCL with small impedance, do not make change the phase angle of DG fault current. Therefore, the low sized RFCL has a negligible limitation compared to the XFCL. But in large impedances, the RFCL creates more phase difference between the DG and network fault currents and provide a more fault current limitation in comparison to the XFCL.

#### 4.2 IEEE 57-Bus Test System

In order to implement and evaluate the proposed method for locating the multiple FCLs in the network with multi-level voltages and penetrated by DGs, the IEEE 57-bus test system is used. As shown in Fig. 10(a), all buses of the test system are classified into four voltage levels that are 132, 69, 33, and 13.8kV. The short circuit level in each bus according to the voltage level is shown in Fig. 10(b). It is assumed that there is possible, installing the FCLs in any location with any voltage level in the network. It is assumed that the critical buses are at the voltage levels of 69, 33, and 13.8kV, and the target level of short circuit currents are shown in Table 8. In order to reduce the short circuit levels to target levels at critical buses, the whole network as an interconnected system with four subsystems and voltage levels is considered and the results of locating FCLs using the proposed method are shown in Table 9.

Moreover, locating the FCLs is accomplished for each voltage level and independent of the other voltage levels and the results of independent FCL allocation for voltage levels of 69, 33, and 13.8kV are shown in Table 10. According to the results, it is obvious that locating the FCLs in an interconnected network with four voltage levels mitigates the short circuit levels to the target levels with the fewer FCLs and the lowest cost. As indicated, the sum of the total cost for fault current reduction by FCLs installation in the whole network entirely is about the 5.98 million dollars for 9 allocated FCLs, while this amount is about 6.58 million dollars with 12 FCLs installation independently in each subsystem. Therefore, FCLs allocation in an interconnected network with all voltage levels prevents the overlapping of some FCLs in reducing the short circuit levels. This also prevents unnecessary investments for FCL installation in the network.

		Ű							
Vo	Voltage level [kV] Critical			Targ	get short circuit le	vel [kA]			
	69		38,48,51		6				
	33	19	9,20,25,26		2				
	13.8		56,57		6				
	132			-					
Table 9 FCLs allocation in the whole 57-bus test system entirely with four voltage levels.									
	FCL type and loc	ation (Type: From-To	o)	- Nrei	$\Sigma 7_{-} = [n + 1]$	Cost function			
132 kV FCLs	69kV FCLs	33kV FCLs	13.8kV FCLs	INFCL	$\Delta \mathbf{Z}_{FCL}$ [p.u.]	[million \$]			
(X:15-45),	$(\mathbf{V}, 22, 28)$	(R:18-19),							
(R:14-46),	$(\Lambda.22-30),$ (V.27,28)	(X:24-26),	(R:11-41)	9	7.56	5.989			
(R:10-51)	(A.37-38)	(R:27-28)							

 Table 8 Critical buses and target short circuit levels in the 57-bus test system



Fig. 10 IEEE 57-bus test system [30], a) Classified subsystems based on the voltage level and b) The short circuit level of buses at each subsystem.

Several cases can be mentioned and described in this regard, which are shown in Fig. 11. For example as indicated in Fig. 11(a), in order to reduce the short circuit levels in critical buses at the voltage level of 33kV (buses of 19, 20, and 25), either one FCL can be installed at the voltage level of 69kV in multi-level voltages allocation or two FCLs can be installed at the voltage level of 33kV in single-level voltage allocation. So, there are two technical solutions for FCLs installation to mitigate the short circuit level of critical buses at the voltage level of 33kV. But always, in multiple FCLs allocation using the proposed algorithm, according to the fixed and incremental costs of FCL, the low-cost scenario is selected as the optimal solution.

Generally, if a major portion of the fault current in one or more critical buses is injected via a power plant or DG located in another voltage level, in multi-level voltages allocation it may be satisfied the technical constraints by installing the FCLs in other voltage levels with minimum number, size and investment cost. Therefore, to reduce the critical short circuit levels, the FCLs allocation in multi-level voltages is less costly, comparing to the allocation in single-level voltage separately. Therefore the result of entire allocation is an optimal technical and economic solution.

As mentioned previously, the critical buses may be fed with one or more DGs located in other subsystems. Actually, the all penetrated DGs together make increase the short circuit levels in critical buses; so that, each DG based on its rating and location, shares the fault current and causes the high short circuit level in critical buses. Hence, sometimes installation of FCL in a subsystem is required for mitigating fault currents contribution of several DGs in other subsystem. Because it may impose the fewer FCLs and the lower costs to network planner for reducing short circuit levels in critical buses at all the subsystems.

The penetration of synchronous-based DGs in various voltage levels of the IEEE 57-bus test system is assumed according to the categorization of DG classes in Table 11. It is assumed the maximum increase percentage allowable short circuit level to be 15% in all the buses. The short circuit levels in 17 buses with various voltage levels increase to more than 15%, due to DGs penetration. Therefore, using the FCLs allocation the exceeded short circuit levels are limited to allowable level. The parameters of located FCLs in the modified 57-bus test system are shown in Table 12.

	Tuble 101 CES unocution in cuch voltage level of the 57 b		stem maepena	entry.
Voltage level [kV]	FCL type and location (Type: From-To)	NFCL	$\Sigma Z_{FCL}$ [p.u.]	Cost function [million \$]
69	(R:46-47), (R:49-50), (X:44-50), (X:38-48)	4	1.56	2.542
33	(R:18-19), (R:20-21), (R:24-25), (R:24-26), (X:27-28)	5	5.13	2.671
13.8	(R:56-57), (R:41-56), (X:11-41)	3	5.01	1.370
Total		12	11.70	6.583

Table 10 FCLs allocation in each voltage level of the 57-bus test system independently



**Fig. 11** The changes of FCLs location in single or multi-level voltages allocation for reducing the fault currents of critical buses; a) Critical buses at 33kV: 19, 20, 25, b) Critical buses at 69kV: 38, 48, 51, and c) Critical buses 13.8kV: 56, 57.

Table 11 Penetration of DG	s in the IEEE 57-bus test system	m (modified 57-bus test system)
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DG number	Installing bus	Voltage [kV]	MVA	Transient reactance [p.u.]	Power factor	
DG 1	21					
DG 2	38	69	10	0.1	0.9 lag	
DG 3	45				-	
DG 4	20	22	5	0.1	0.0.1.2	
DG 5	26	33	3	0.1	0.9 lag	
DG 6	41	13.8	2	0.1	0.9 lag	

Table 12 Results of FCLs allocation in all lines of the modified 57-bus test system.							
FCL-equipped lines (FCL type, FCL size, From-To)				Σ7 [n 11 ]	Cost function		
69kV FCLs	33kV FCLs	13.8kV FCLs	INFCL	ZZFCL [p.u.]	[million \$]		
(R,1.07,22-38), (R,1.05,38-44)	(X,0.5,19-20), (X,1.04,24-26)	(X,1.08,41-42), (R,1.55,56-57)	6	6.29	3.630		

	Table 13 Results of	f FCLs allocation	in DG feeder lines	of modified 57-bus test sy	stem.
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FCL-equipped DGs (FCL type, FCL size, DG number)			Maar	Σ7[m +ı ]	Cost function
69kV DGs	33kV DGs	13.8kV DGs	INFCL	ZZFCL [p.u.]	[million \$]
(R,1.21,1), (R,0.87,2), (R,0.4,3)	(X,2.45,4), (X,2.26,5)	(R,1.53,6), (R,1.54,7)	7	10.26	4.521

For comparing results, the FCLs allocation is performed just for DG connection points as candidate locations. The required FCLs for short circuit level reduction are shown in Table 13. As indicated in the results, sum of the investment cost for fault current reduction by FCL installations in all lines is about the 3.63 million dollars with 6 installed FCLs, while that is required about 4.52 million dollars for 7 FCLs installation in DG feeder lines. Therefore, in FCL allocation the candidate locations should not be limited to the DG connection points.

The procedures of multiple FCLs allocation in the best

scenario for the two above cases (Tables 12 and 13) are illustrated in Fig. 12. As previously mentioned, according to the type and size of FCL, an optimal location for FCL is selected in each stage of the proposed method. Adding the FCL impedance ( $\Delta Z_{FCL}$ ) continues in the next stages until all the technical constraints are satisfied and producing a scenario is finished. This iterative procedure is repeated to produce other scenarios. Finally, a scenario with the least cost is selected as an optimal solution or best scenario for multiple FCLs allocation in the network that is shown for the two above cases.



Fig. 12 Changes of positions and impedances of assigned FCLs during the best scenario or path in the IEEE 57-bus test system; a) Optimal FCLs allocation in all locations and b) Optimal FCLs allocation in DGs connection points.

A notable point in determining the best scenario or path is that an optimal path to reach the optimal solution in FCL allocation is not unique. Nevertheless, the final optimum solution related to the number, location, type, and size of FCLs is unique. In the other words, there may be one or more paths to reach this optimal solution, whilst the allocation parameters of the FCLs (number, type, size, voltage level, location) are constant and optimal.

#### 4.3 IEEE 300-Bus Test System

In order to implement and evaluate the proposed method on a larger case, the IEEE 300-bus test system including 13 voltage levels, 411 lines, and 69 generators is used. The classifying this grid into 9 subsystems is shown in Fig. 13. The penetration of the synchronous-based DGs in subsystems is assumed as listed in Table 14.

The short circuit levels will change due to the penetration of DGs. The short circuit levels in all buses of the modified network are checked and compared with the state of pre-installed DGs. It is assumed the maximum increase percentage allowable short circuit level to be 10% in all the buses. It is seen that upgrading the breaking capacity of CBs is inevitable due to increasing the short circuit levels to more than 10% in some buses. In these conditions, the short circuit level

of critical buses can be reduced by applying the multiple FCLs allocation on the modified network. Therefore, by using the proposed method, the short circuit levels in these buses are limited to the allowable level. The critical buses and the changes in the fault currents due to DGs penetration and FCLs installation are indicated in Fig. 14. As illustrated, after the multiple FCLs installation the exceeded short circuit levels, are mitigated to levels with a maximum increase percentage of 10%. Also, the result of multiple FCLs allocation is shown in Table 15. As can be seen, there are required four FCLs located in some lines and seven FCLs located in DGs connection points to the network. Also, the sum of the total cost for fault current reduction by FCLs installation in the network entirely is about 7.544 million dollars for 11 allocated FCLs.

#### 4.4 A Real Transmission System in Iran

In order to verify the proposed method on a real network, Khorasan's transmission network is used. This network has multiple voltage levels, from 63kV to 400kV. This study focuses on the subsystem of 400kV which whole has 17 buses and 19 transmission lines. The single-line diagram of the portion of the system at 400kV is illustrated in Fig. 15.

During the generation expansion planning it is planed the installation of two 500MW wind farms in this network. The feasibility studies are accomplished for these wind farms that will be connected to buses 10 and 14. With the penetration of these wind farms, fault currents are increased at some buses. Fault currents on all load buses were calculated, and buses 3, 6 and 11, have the highest increase in short circuit level. The proposed method is applied to reduce the short circuit level to the previous levels in these buses.



Fig. 13 Classified IEEE 300-bus test system [30].

Table 14 Penetration of DGs in IEEE 300-bus test system.						
DG number	Subsystem	Installing bus	Voltage [kV]	MVA	Transient reactace [p.u.]	Power factor
DG 1	2	89				
DG 2	2	103	115	18	0.1	0.9 lag
DG 3	7	197				-
DG 4	7	189				
DG 5	7	205	66	12	0.1	0.0.102
DG 6	8	246	00	15	0.1	0.9 lag
DG 7	7	248				
DG 8	9	230				
DG 9	9	236	20	7	0.1	0.9 lag
DG 10	2	7039				
DG 11	3	7055				
DG 12	2	7049	13.8	5	0.1	0.9 lag
DG 13	5	7130				
DG 14	2	9006	6.6	2	0.2	0.0.100
DG 15	2	9023	0.0	2	0.2	0.9 lag



FCL number	Subsystem	FCL location (DG connection point or line:From-To)	Z <sub>FCL</sub> [p.u.]	Cost function [million \$]
1	2	Line: 9001-9006	j0.71	
2	2	Line: 9002-9021	0.49+j0.35	
3	2	DG 1 connection point	1.12	
4	2	DG 2 connection point	j0.52	
5	7	DG 4 connection point	0.59	
6	7	DG 5 connection point	j1.54	7.544
7	8	DG 6 connection point	0.62	
8	2	DG 14 connection point	0.54+j0.75	
9	2	DG 15 connection point	1.41	
10	8-9	Line: 198-211	1.64	
11	7-8	Line: 247-248	0.56	

Table 15 Results of FCL allocation in the modified 300-bus test system



Fig. 15 Single-line diagram of Khorasan's transmission network.



Fig. 16 Fault currents and reductions after installing DGs and FCLs on Khorasan's transmission network.

The optimal FCLs locations, found by the proposed method, are lines 2, 3, and 16. The lines are equipped by FCL and shown in Fig. 15. The fault current reductions on all 400 kV buses are given in Fig. 16. The final impedance of the FCLs and the total cost to FCL installation, are given in Table 16.

#### 5 Conclusion

This paper presents a novel iterative based method to determine the optimal type, number, location, and impedance of FCLs in the network that have multiple voltage levels considering DGs penetration in all voltage levels. In the proposed method, the multiple FCLs allocation problem is solved with a combination of genetic algorithm and sensitivity analysis. The reduction of the exceeded short circuit levels with minimum investment cost according to the FCL costs is formulated as the objective function. Furthermore, a new sensitivity index, named ADFC, is introduced for quantifying impacts of FCL location on mitigation of short circuit level. The proposed ADFC can serve as an effective measure to determine the best location for FCLs, especially in large networks with a lot of subsystems. The proposed method is implemented and tested on the standard 30-bus, 57-bus, and 300-bus test systems. The results confirm the effectiveness of the proposed HGASA method.

#### References

- [1] B. V. Vaishnavi, S. Angelin, D. P. Trivenishree, N. Nabi, and G. J. Sowmya, "Superconducting fault current limiter & its application," *International Journal of Scientific & Engineering Research*, Vol. 7, No. 5, pp. 126–134, 2016.
- [2] R. Asghar, "Fault current limiters types, operations and its limitations," *International Journal of Scientific & Engineering Research*, Vol. 9, No. 2, pp. 1020–1027, 2018.
- [3] A. Khazali and M. Kalantar, "Optimal power flow considering fault current level constraints and fault current limiters," *International Journal of Electrical Power & Energy Systems*, Vol. 59, pp. 204–213, 2014.
- [4] U. A. Khan, J. K. Seong, S. H. Lee, S. H. Lim, and B. W. Lee, "Optimal placement and sizing of fault current limiter in a real network: A case study," *International Journal of Engineering Transactions* C: Aspects, Vol. 28, No. 3, pp. 402–409, 2015.
- [5] J. H. Teng and C. N. Lu, "Optimum fault current limiter placement with search space reduction technique," *IET Generation, Transmission and Distribution*, Vol. 4, No. 4, pp. 485–494, 2009.
- [6] P. Yu, B. Venkatesh, A. Yazdani, and B. N. Singh, "Optimal location and sizing of fault current limiters in mesh networks using iterative mixed integer nonlinear programming," *IEEE Transactions on Power Systems*, Vol. 31, No. 6, pp. 4776–4783, 2016.
- [7] H. T. Yang, W. J. Tang, P. Lubicki, C. Wang, and S. Wang, "Placement of fault current limiters in power system through a two-stage optimization approach," *IEEE Transactions on Power Delivery*, Vol. 33, No. 1, pp. 131–140, 2018.

- [8] H. C. Jo and S. K. Lee, "Optimal placement of superconducting fault current limiters (SFCLs) for protection of an electric power system with distributed generations (DGs)," *IEEE Transactions* on Applied Superconductivity, Vol. 23, No. 3, pp. 5600304–5600304, 2013.
- [9] A. Elmitwally, E. Gouda, and S. Eladawy, "Optimal allocation of fault current limiters for sustaining overcurrent relays coordination in a power system with distributed generation," *Alexandria Engineering Journal*, Vol. 54, No. 4, pp. 1077–1089, 2015.
- [10]H.C. Joo, S.K. Joo, and K. Lee, "Superconducting fault current limiter placement for power system protection using the minimax regret criterion," *IEEE Transactions on Applied Superconductivity*, Vol. 25, No. 3, pp. 1–5, 2015.
- [11]S.Y. Kim, W.W. Kim, and J. O. Kim, "Determining the location of superconducting fault current limiter considering distribution reliability," *IET Generation, Transmission and Distribution*, Vol. 6, No. 3, pp. 240–246, 2012.
- [12]H. Bahramian Habil, E. Azad-Farsani, and H. Askarian abyaneh, "A novel method for optimum fault current limiter placement using particle swarm optimization algorithm," *International Transaction* on *Electrical Energy Systems*, Vol. 25, No. 10, pp. 2124–2132, 2015.
- [13]S. Y. Kim, I. S. Bae, and J. O. Kim, "An optimal location for superconducting fault limiter considering distribution reliability," in *Power and Energy Society General Meeting*, pp. 1–5, 2010.
- [14]S. Behzadirafi and H. Salehfar, "Using superconducting fault current limiters to enhance the reliability of power transmission systems," in *Power* and Energy Society General Meeting, pp. 1–8, 2010.
- [15]S. Behzadirafi, M. Fotuhi-Firuzabad, and T. S. Sidhu, "Reliability enhancement in switching substations using fault current limiters," in 9<sup>th</sup> International Conference on Probabilistic Methods Applied to Power Systems, KTH, Stockholm, Sweden, 2006.
- [16] M. Sjöström and D. Politano, "Technical and economical impacts on a power system by introducing an HTS FCL," *IEEE Transactions on Applied Superconductivity*, Vol. 11, No. 1, pp. 2042–2045, 2001.
- [17] J. Lee and S. K. Joo, "Economic assessment method for superconducting fault current limiter (SFCL) in fault current-constrained power system operation," *IEEE Transactions on Applied Superconductivity*, Vol. 23, No. 3, pp. 5601104– 5601104, 2013.

- [18]S. A. Shahriari, A. Variani, and M. Haghifam, "Cost reduction of distribution network protection in presence of distributed generation using optimized fault current limiter allocation," *International Journal of Electrical Power & Energy Systems*, Vol. 43, pp. 1453–1459, 2012.
- [19]B. C. Sung, D. K. Park, J. W. Park, and T. K. Ko, "Study on optimal location of a resistive SFCL applied to an electric power grid," *IEEE Transactions on Applied Superconductivity*, Vol. 19, No. 3, pp. 2048–2052, Jun. 2009.
- [20]G. Didier, J. Leveque, and A. Rezzoug, "A novel approach to determine the optimal location of SFCL in electric power grid to improve power system stability," *IEEE Transactions on Power Systems*, Vol. 28, No. 2, pp. 978–984, May 2013.
- [21]S. Y. Kim and J. O. Kim, "Reliability evaluation of distribution network with DG considering the reliability of protective devices affected by SFCL," *IEEE Transactions on Applied Superconductivity*, Vol. 21, No. 5, pp. 3561–3569, 2011.
- [22]L. Huchel, H. H. Zeineldin, and E. F. E. Saadany, "Protection coordination index enhancement considering multiple DG locations using FCL," *IEEE Transactions on Power Delivery*, Vol. 32, No. 1, pp. 344–350, 2017.
- [23] K. Hongesmbut, Y. Mitani, and K. Tsuji, "Optimal location assignment and design of superconducting fault current limiters applied to loop power systems," *IEEE Transactions on Applied Superconductivity*, Vol. 13, No. 2, pp. 1828–1831, Jun. 2003.
- [24] A. Agheli, H. A. Abyaneh, R. M. Chabanloo, and H. H. Dezaki, "Reducing the impact of DG in distribution networks protection using fault current limiters," in 4<sup>th</sup> International Power Engineering and Optimization Conference (PEOCO), pp. 298– 303, 2010.
- [25]S. Alaraifi, M. S. El Moursi, and H. H. Zeineldin, "Optimal allocation of HTS-FCL for power system security and stability enhancement," *IEEE Transactions on Power Systems*, Vol. 28, No. 4, pp. 4701–4711, 2013.

- [26] A. Mahmoudian and M. Niasati, "A novel approach for optimal allocation of fault current limiter in distribution system via combination of particle swarm optimization algorithm and genetic algorithm (PSOGA)," in 21<sup>st</sup> Electrical Power Distribution Conference, 2016.
- [27] The Guideline for Connection of Distributed Generators to Utility, Ver. 1, Tavanir, Iran, Jan. 2014.
- [28]G. Ganev, K. Hinov, and N. Karadzhov, "Fault current limiters – Principles and application," *International Symposium on Electrical Apparatus* and Technologies (SIELA), Bulgaria, Vol. 1, 2012
- [29]I. Normal and S. Eckroad, "Superconducting Fault Current Limiters," *Electric Power Research Institute* (*EPRI*), 2009.
- [30]IEEE Test Systems, accessed Jun. 2019 [Online]. Available: <u>http://www.ee.washington.edu/research/p</u>stca/



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