Implementation of Low-Cost Architecture for Control an Active Front End Rectifier

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Abstract: In AC-DC power conversion, active front end rectifiers offer several advantages over diode rectifiers such as bidirectional power flow capability, sinusoidal input currents and controllable power factor. A digital finite control set model predictive controller based on fixed-point computations of an active front end rectifier with unity displacement of input voltage and current to improve dynamic response has been presented in this paper. Here by using a predictive cost function and fixed-point computations, the optimal switching state to be applied in the next sampling is selected. The low-cost architecture is implemented on a FPGA platform. Designed architecture is constructed based on fixed-point arithmetic with minimal functional units. The control algorithm, which is used in this architecture, is Finite-Set Model Predictive Control (FS-MPC). Compared with other controllers, this controller provides a much better dynamic performance. Finally, in order to evaluate the accuracy of the fixed-point computations several cases for various loading conditions and word lengths are verified.

1 Introduction

ACTIVE-FRONT-END Rectifiers (AFE) are currently a well-suited alternative to diode rectifiers, because they produce sinusoidal input currents with unity displacement power factor, low harmonic input current and bidirectional power flow [1], [2]. AFE rectifier can be used in renewable energies and active power filter where interconnection stages are essential [3]. Different control scheme applied to power electronic converters have been classified as; Voltage Oriented Control (VOC) and Direct Power Control (DPC) which is investigated in [4]. Recently, finite-control-set model-predictive-control has been successfully addressed to control AFEs [5]. It has been successfully applied to several power electronics

devices as such as DC-DC converters (buck and boost), DC-AC converters (Two-level VSI, Neutral Point Clamped, Cascaded H-Bridge Inverter and Flying-Capacitor Inverter), AC-DC converters (Single- phase Boost Converter, Asymmetric Half Bridge converter, Active-Front-End Rectifier and Current Source Rectifier) and AC-AC converters (Modular Multilevel Converter, Direct Matrix Converter and Indirect Matrix Converter) [6]. Model Predictive Control (MPC) offers many advantages; in particular, it can be used in a variety of process, being simple to apply in multivariable systems. Furthermore, the inclusion of nonlinearities and constraints in the control law is straightforward [6]. Moreover, this scheme does not require internal current control loops and modulators, which greatly reduces its complexity. This digital control technique has successfully been applied to a wide range of power converters, drives and energy system applications [7], [8]. In Finite Control Set Model Predictive (FCS-MPC) there are limited number of switching states of the power converter for solving the optimization problem and a cost function is used as a criterion to select the optimal future actions [9], [10]. This control technique uses a model of the system to calculate predictions of the future behavior of the

system for a given set of possible actuations for a predefined time horizon. The sequence of actuations that minimizes a cost function, which synthesizes the control objectives, is selected, and the first element of the sequence is applied. This optimization is repeated every sampling time considering the new measured data [11]. In this work, a FCS-MPC technique has been used to control an AFE rectifier with unity power factor. FCS-MPC uses a discrete-time model of the system and selects the optimal firing actuation to converter for the next sampling period based on minimum cost function [12].

In the present study, the basic purpose is to evaluate a low-cost architecture of a digital controller for an AC-DC rectifier using FCS-MPC concept. As a proof of concept, the controller is implemented on a FPGA platform (Xilinx vertex II), based on predictive control and fixed point arithmetic. In previous works, controllers are implemented using based block-diagram high level synthesis tools, such as XILINX VIVADO or ALTERA QUARTUS. These synthesis tools provide an easy design platform using functional description of the algorithm, but design details are hidden from designer, which makes it suitable for lab prototyping of the design, but it is not applicable for industrial designs in which designer needs an optimized implementation suitable for embedded or integrated circuit hardware realization. For instance, accuracy and implementation cost (bit-width vs. required hardware) is normally ignored in automated design synthesis. Further, without deep knowledge of hardware design and synthesis, proper trade-offs between different design parameters such as, implementation cost, speed, reliability, precision and power consumption are not possible. In this work, unlike previous works, we present an explicit design architecture and details, which give the transparency to future designers to acquire this design approach and apply modifications for further improvements and/or industrial applications.

With this approach, the controller design is optimum in terms of required resources (only two adder and two multiplier), which makes it an efficient candidate for an integrated circuit implementation of this controller. With this approach variety of switching control algorithms can be transformed to firmware hardware with practical industrial application. There are several challenges in transforming a software algorithm to a firmware design including: required resources, limitation of mathematical operations in hardware, precision, data management and control.

In this work computation accuracy is evaluated for different word-lengths. There is a trade-off between word-length and hardware cost. This scheme predicts behavior of future input currents for each switching state of the converter. The cost function evaluates predicted value for input currents with their references and minimizes the error between them at the end of each sampling time and then the optimum switching states

apply to power switches.

The paper is organized as follows. In Section 2, the Operation of the AFE rectifier is analyzed. In Section 3, the model predictive control of active front end rectifier is introduced. In Section 4, hardware implementation is presented. In Section 5, implementation results are presented and the conclusions are presented in Section 6.

2 Operation of the AFE Rectifier

The AFE rectifier topology is shown in Fig. 1 which corresponds to a fully controlled three phase bridge with semiconductor switches(IGBTs) connected to the three-phase voltage supply (V_u, V_v, V_w) using the input filter inductances (L) and resistances (r). The model of the ac side of the rectifier is:

$$V_u = ri_u + L\frac{di_u}{dt} + V_{u0} + V_{0N} \tag{1}$$

$$V_v = ri_v + L\frac{di_v}{dt} + V_{v0} + V_{0N} \tag{2}$$

$$V_w = ri_w + L\frac{di_w}{dt} + V_{w0} + V_{0N} \tag{3}$$

V_{0N} is the common mode voltage between the floating neutral of the source and the negative bus of the rectifier, considering balanced input voltages and no neutral current, can be calculated as [13]:

$$V_{0N} = \frac{V_{u0} + V_{v0} + V_{w0}}{3} \tag{4}$$

Considering each rectifier voltage given by

$$V_{u0} = S_u V_{dc} \quad , \quad V_{v0} = S_v V_{dc} \quad , \quad V_{w0} = S_w V_{dc} \tag{5}$$

where S_u, S_v, S_w are the switching states (1 if the corresponding upper switch is ON or 0 if it is OFF) and V_{dc} is the dc voltage. According to the above equations the ac side can be modeled as:

$$L\frac{di_u}{dt} = -ri_u + V_u - \frac{1}{3}(2S_u - S_v - S_w)V_{dc} \tag{6}$$

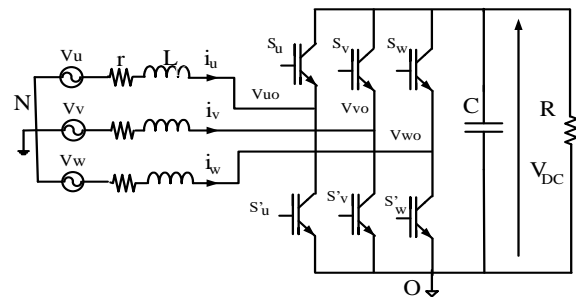$$L\frac{di_v}{dt} = -ri_v + V_v - \frac{1}{3}(-S_u + 2S_v - S_w)V_{dc} \tag{7}$$

Fig. 1 AFE rectifier topology.

$$L \frac{di_w}{dt} = -ri_w + V_w - \frac{1}{3}\left(-S_u - S_v + 2S_w\right)V_{dc} \qquad (8)$$

The dc side of the converter is modeled as

$$c \frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R} + i_u S_u + i_v S_v + i_w S_w \qquad (9)$$

where R is the load resistance and C is the dc-link capacitance.

Re-writing the model using vector variables, the model of the AC side becomes

$$L \frac{di_s}{dt} = -ri_s + v_s - MS_s V_{dc} \qquad (10)$$

where $\quad V_s = \begin{bmatrix} V_u \\ V_v \\ V_w \end{bmatrix}, i_s = \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix}, \quad S_s = \begin{bmatrix} S_u \\ S_v \\ S_w \end{bmatrix} \quad$ and

$$M = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}.$$

The DC side can be expressed as

$$C \frac{dV_{dc}}{dt} = -\frac{V_{dc}}{R} i_s^T S_s \qquad (11)$$

3 Model Predictive Control of Active Front End Rectifier

Model Predictive Control (MPC) has now approximately three decades of sustained development and offers many advantages; MPC is a control scheme based on the search of the optimal input to achieve a desired output. As in power electronics the inputs belong to a finite set, this control strategy is well suited for power converters [14]. The MPC techniques applied to Power Electronics have been classified into two main categories [7], [8]: Continuous Control Set MPC and Finite Control Set MPC (FCS-MPC). In the first group, a modulator generates the switching states starting from the continuous output of the predictive controller. On the other hand, the FCS-MPC approach takes advantage of the limited number of switching states of the power converter for solving the optimization problem. A discrete model is used to predict the behavior of the system for every admissible actuation sequence up to the prediction horizon. The switching action that minimizes a predefined cost function is finally selected to be applied in the next sampling instant. The main advantage of FCS-MPC lies in the direct application of the control action to the converter, without requiring a modulation stage [11]. A simplified control block diagram for control of an AFE rectifier is shown in Fig. 2. In this block diagram the input currents ($i_s(k)$) and input voltages ($v_s(k)$) measured and apply to digital

controller. Output voltage (V_{dc}) measured and compared with its reference (V_{dc}^*), then apply to PI controller. PI controller is used to set reference currents (I_{ref}) from the error signal between the measured and reference DC voltage. The predictive controller uses a current reference which obtained by the dc-link PI controller, the output of the dc-voltage controller is multiplied by the input voltage in order to obtain the in phase sinusoidal references.

In digital controller the future current ($i_p[k+1]$) will predict then compared with its reference ($i^*[k+1]$) by cost function. The cost function minimizes the error between the predicted currents and their references at the end of each sampling time. Finally, the switching state that minimize the cost function apply to IGBTs.

To find a suitable discrete model of the converter a first order forward difference approximation of the derivative can be used [13]. In the AFE rectifier the current derivatives are calculated as

$$\frac{di_s}{dt} = \frac{i_{sp}(k+1) - i_s(k)}{T_s}, \quad s = u, v, w \qquad (12)$$

where T_s is sampling time. According to these equations, the discrete model of the AFE rectifier is given by

$$i_{sp}(k+1) = i_s(k)K_L + \frac{T_s}{L}\left(V_s(k) - MS_s V_{dc}(k)\right) \qquad (13)$$

where $K_L = 1 - rT_s/L$. The currents error of each input can be defined as

$$e_s = i_s^*(k+1) - i_{sp}(k+1) \qquad (14)$$

where i_s^* is current reference. The cost function is calculated by

$$g = e_s^T e_s \qquad (15)$$

4 Hardware Implementation

FPGAs contain an array of programmable logic blocks, and a hierarchy of reconfigurable interconnects
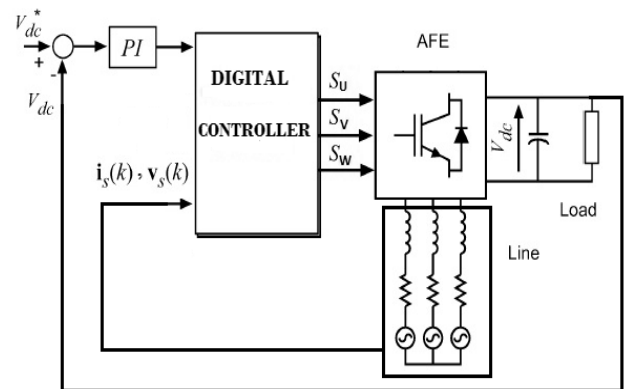

Fig. 2 Proposed control scheme for the rectifier.

that allow the blocks to be wired together, like many logic gates that can be inter-wired in different configurations. Some of the major disadvantages of the conventional microprocessor or DSP controls could overcome by using FPGA, because it can be designed to perform any application and is not specific to a particular function. The FPGA can be more efficient than the conventional controller due to fast prototyping, software design and simple hardware design. Also, the written code is almost independent from the architecture of the device and the hardware is reconfigured easily. Other advantages over other traditional devices are different and probably shorter design cycles, low-power consumption, and higher density for implementing digital control system [15].

The FPGA is suitable for systems which require relatively simple computation and fast processing time; complex control algorithms with complicated computations could be easier implemented by software in the FPGA, as they may embed a true microprocessor. The results of this co-design is increasing the flexibility of the designed system and reducing the development time [16]. The speed, size, and the number of I/O pins of a modern FPGA far exceed that of a microprocessor or DSP. These features allow to improve the implementation of predictive control algorithm by means of calculates the next step currents and error functions for all the inputs simultaneously [13].

The biggest issue in the most of previous approaches, however, is their hardware design approach. Since hardware implementation of the control algorithm is a multidisciplinary field, it is a challenge for power electronic designers to consider and solve both control algorithm issues and hardware design efficiency at the same time. Our approach presents a new direction in this regard. We are introducing a design method based on a predefined soft-architecture in which hardware datapath is synthesized. This approach provides a solution for power electronic engineers by which they can design efficient control hardware with minimum cost. This is different from a microcontroller-based approach which is limited to the hardware resources available on the microcontroller chip. Also, it is different from other FPGA-based approaches and automatic synthesis tools, which either offer simplified drag and synthesis methods by hiding design complexity or offer a large amount of hardware and FPGA parameters and professional design details.

In this section, we present and analyze the implementation details of the fixed-point based architecture. Our purpose is to control the current in fixed-point based architecture for different word-lengths. For simulation results, component designs were coded in VHDL. Our target device is Xilinx vertex II, which contains 4.3 Mb on-chip memory and Xilinx ISE development tools were used to simulate and synthesize our architecture. The controller has implemented on FPGA and control signals have achieved. The flow

chart of computation is shown in Fig. 3. In this flow chart since we have three switches (S_u, S_v, S_w) thus 8 (23) switching states are possible. The algorithm selects the state that minimizes the cost function.

The block diagram of the hardware in this project is shown in Fig. 4. In this block diagram input currents (i_u, i_v, i_w), input voltages (v_u, v_v, v_w) and DC-link voltage (v_{dc}) are inputs and optimum switching states (s_u, s_v, s_w) are outputs.

In this block diagram the 3 bits counter provides 8 switching states. In the formulation section, we have a scheduling (arithmetic structure) diagram for computing cost function, which is represented in the Fig. 5. In this scheduling diagram, we have eleven steps to calculate
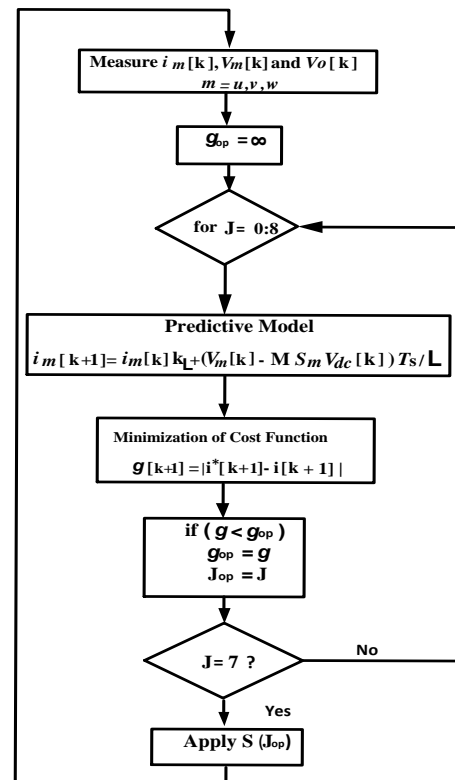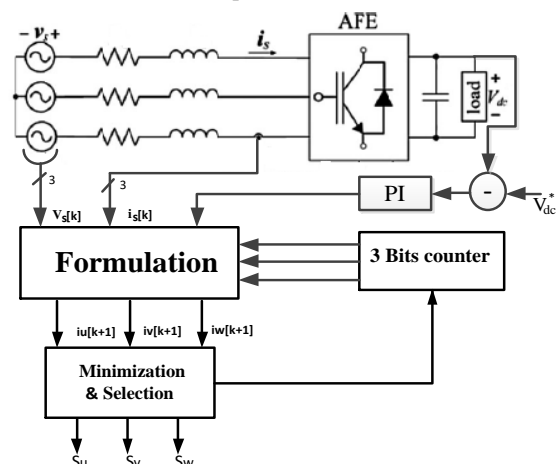

Fig. 3 Flow chart of computation.

Fig. 4 Block diagram of the predictive-control-based hardware for the AFE

cost function. The minimization section by using cost function, compare predicted currents with their references and finally selects the state that minimizes the cost function, then this state is applied to the switches.

The hard-ware implementation of controller is represented at fig.6. This architecture contains two booth multiplier, two ripple carry adder, 11 multiplexers (mux), 3 registers, etc. Datapath and required arithmetic units are determined based on scheduling diagram and their mapping to the proposed hardware. Sequencer, which is essentially a finite state machine (FSM), provides control signals for the functional units to operate based on the control algorithm. The delay

produced by the hardware, gate drivers and switching devices is inevitable. A simple solution to compensate this delay is to take into account the calculation time and apply the selected switching state after the next sampling instant. Here, the measured currents and the applied switching state at time t_k are used to estimate the value of the load currents at time $t(k+1)$. Then, this current is used as a starting point for the predictions for all switching states.

These predictions are calculated by using the load model shifted one step forward in time [17].

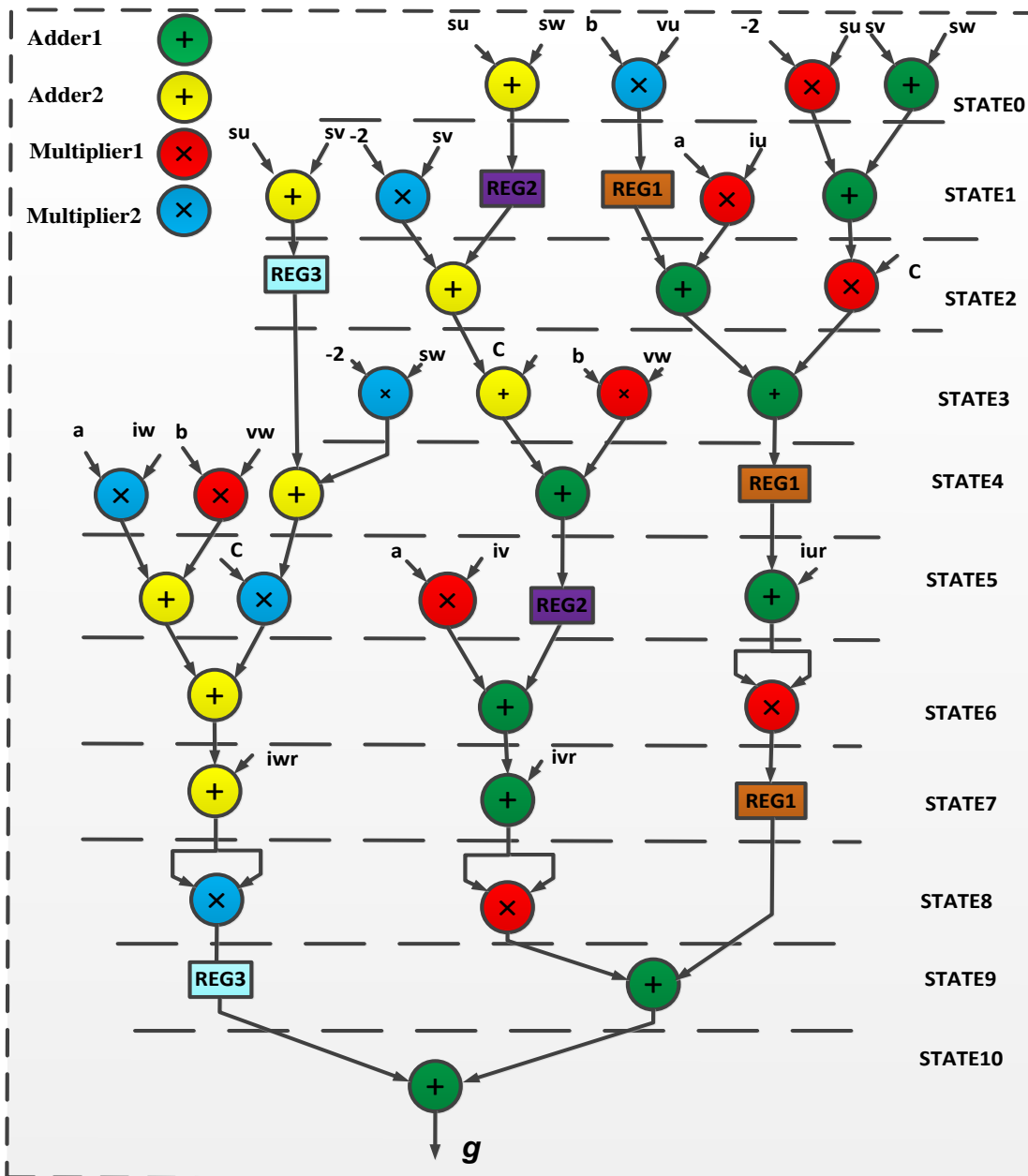Table 1 shows resource usage in fixed-point based architecture for various word-lengths.

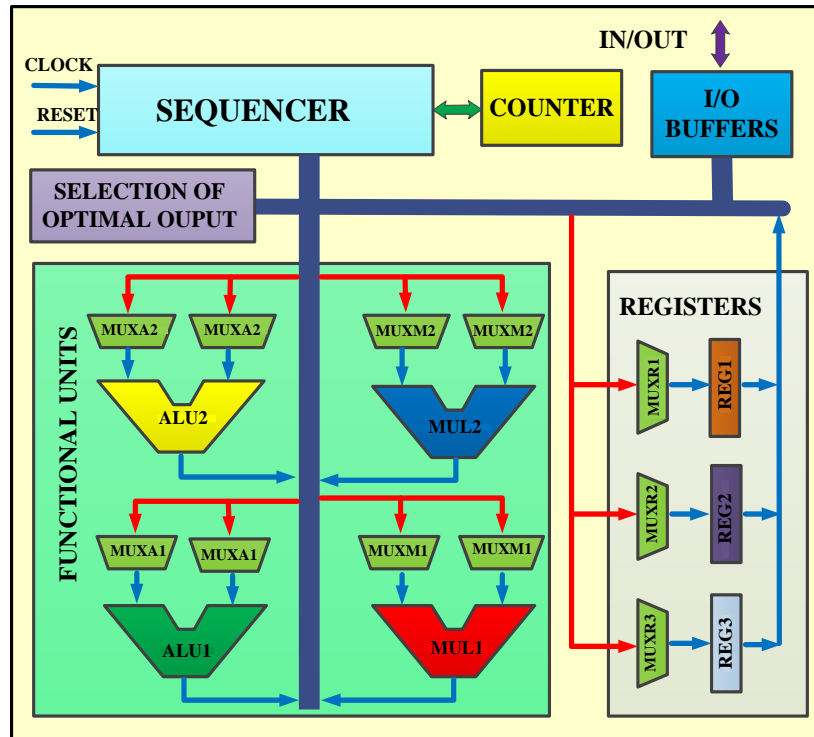**Fig. 5** Arithmetic structure (Scheduling) for computing cost function.

Fig. 6 proposed low-cost architecture.

Table 1 Required hardware resources.

Word- length		32-bits	24-bits	15-bits
Area (Slices)	Multiplier	65	49	34
	Adder	33	22	18

5 Implementation Results

This section, evaluates computation accuracy of the implemented fixed-point based architecture for the control system. Digital circuits are implemented on a XILINX Vertex-II Pro development board. The converter parameters are represented in Table 2.

DC-link reference is taken as 55V which compared with output DC-link voltage. The error calculated from the reference and output DC voltage is used as an input to PI controller. The reference current is calculated with this PI controller. This reference current is compared with predicted input current for all possible switching states for the active front end rectifier. Hence cost functions are found for 8 valid switching states of the converter; the switching state corresponds to minimum cost function is selected for the next sampling time firing actuation.

Figs. 7-9 display the output voltage under negative load step changes for various word lengths (WL). Every word length consists of integer and fraction parts and one bit is considered as a sign bit. The word length, integer length and fraction length are selected based on the nature of numbers and their corresponding calculations. For word lengths greater than 32 bits, round-off errors have no effect on the outputs accuracy, but the system cost will be increased and calculation

speed will be decreased. For word lengths smaller than 15 bits the outputs are severely erroneous and would not be acceptable. To find an optimal word length, one should consider a tradeoff between the output accuracy and implementation cost of the system. The results for positive load step change are similar to negative step. Here voltage overshoot/undershoot, transition time (T_{Tran}), total harmonic distortion(THD) and power factor of input currents are considered as accuracy cost measures. To evaluate performance of the controller negative load current steps are considered. In these states load resistance at t=0.15s changes from 30Ω to 20Ω, 15Ω and 10Ω.

Table 2 Value of the converter parameters.

parameter	Value
V_{smax}	30v
f_s	50Hz
C	1500μf
L	15mH
r	0.4Ω
$V_{dc}{}^*$	55v
T_s	40μs

5.1 Word length (WL) is 32 bits

In this case integer length is 12 bits and fraction length is 19 bits. At t=0.15s load resistance changes from 30Ω to 20Ω, 15Ω and 10Ω. For load changing from 30Ω to 20Ω, input current and voltage and output voltage are shown in Fig 7(a) Here THD of input

currents are equal, and their values are 3.22%. This figure reveals the unity power factor because the angle between input voltage and current is zero degree. It can be observed from Fig. 7(a) that undershoot of output voltage is 3.5v and recovery time is 0.05s.

Results for 30Ω to 15Ω are depicted in Fig. (b). It can be observed that undershoot of output voltage is 7v and recovery time is 0.1s. In this case THD of input current is 3.39% and power factor is equal to 1.

In Fig. 7(c) results for load changing from 30Ω to 10Ω are represented. The undershoot of the output voltage is 12v and recovery time is 0.12s. Here THD of the input currents are equal, and their values are 3.5%. The angle between input voltage and current after load changing is 82.2° (power factor=0.13).

5.2 Word length (WL) is 24 bits

In this part for all cases integer length is 10 bits and fraction length is 13 bits. Results for this state are depicted in Fig. 8. It can be observed from Fig. 8(a) that
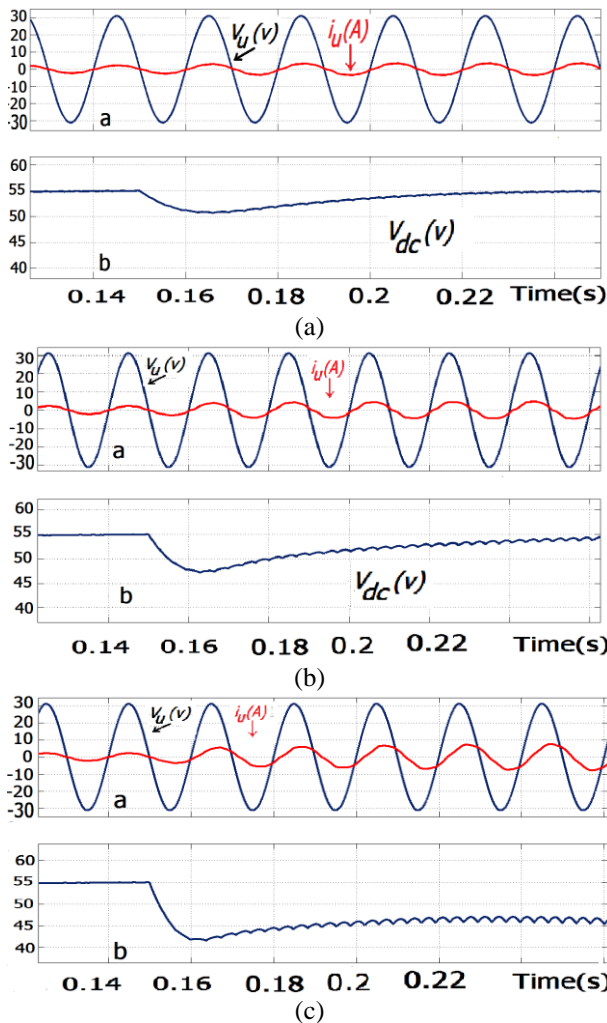

Fig. 7 Results for WL=32 a) Load changing from 30Ω to 20Ω, b) Load changing from 30Ω to 15Ω and c) Load changing from 30Ω to 10Ω.

for load changing from 30Ω to 20Ω undershoot of output voltage is 4v and recovery time is 0.07s. In this case THD is 4.45% and we observer unity power factor. Input current and voltage and output voltage for load changing from 30Ω to 15Ω are shown in Fig. 8(b). Here THD of the input currents are equal, and their values are 4.55%. This figure reveals the unity power factor. It can be observed that undershoot of the output voltage is 8v and recovery time is 0.12s.

Results for load changing from 30Ω to 10Ω are depicted in Fig. 8(c). In this figure undershoot of output voltage is 13v and recovery time is 0.15s. THD of input current is 4.67% and after load changing the angle between input voltage and current is 84.2° (power factor=0.1).

5.3 Word length (WL) is 15 bits

In Fig. 9 results for this case is represented. Here integer length is 5 bits and fraction length is 9 bits. Similar to another sections at *t*=0.15s load resistance changes from 30Ω to 20Ω, 15Ω and 10Ω. For load
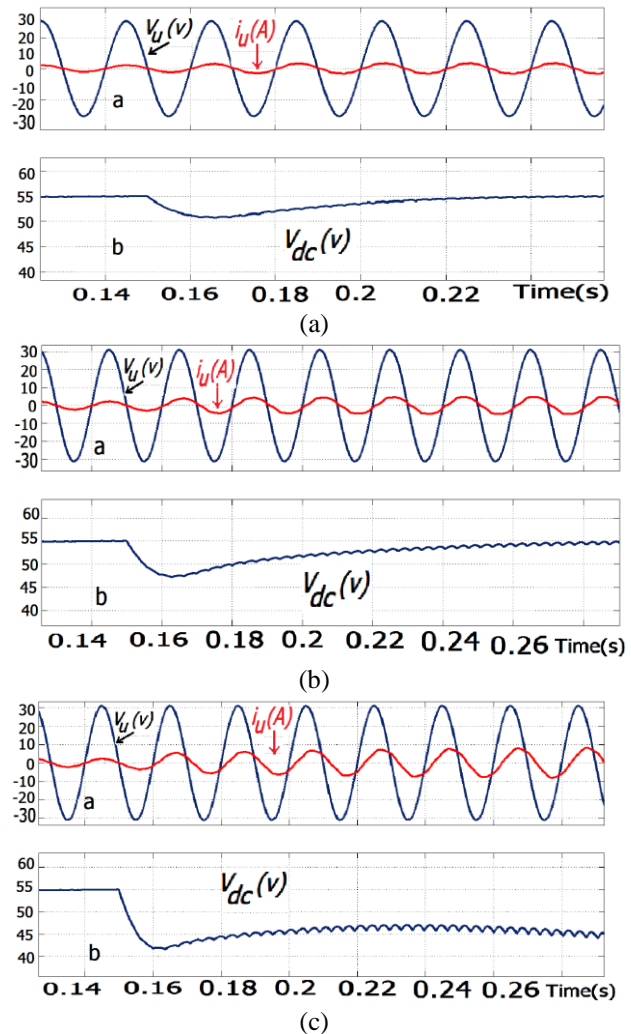

Fig. 8 Results for WL=24 a) Load changing from 30Ω to 20Ω, b) Load changing from 30Ω to 15Ω and c) Load changing from 30Ω to 10Ω.

changing from 30Ω to 20Ω output results are depicted in Fig. 9(a). In this figure undershoot of output voltage is 5v and recovery time is 0.15s. Here THD of input currents are equal, and their values are 7.15%. The angle between input voltage and current is zero.

In Fig. 9(b) results for load changing from 30Ω to 15Ω are represented. Here THD of input currents are equal, and their values are 7.2%. This figure reveals the unity power factor. The undershoot of output voltage is 8v and recovery time is 0.17s.

Results for load changing from 30Ω to 10Ω in Fig. 9(c) are depicted. It can be observed from this figure, that undershoot of output voltage is 13v and recovery time is 0.19s and steady state of output voltage is smaller than 55v. Here THD of input currents are equal, and their values are 7.5%. The angle between input voltage and current after load changing is 85.4º (power factor=0.08).

The results for all cases are represented in Table 3. According to result values for all cases, in smaller WL are the THD, undershoot and recovery time are bigger, so a tradeoff exists between these parameters.

In [13] there is an FPGA design, which is based block-diagram high level synthesis tools (XILINX SPARTAN 3E). In this work word-length is fixed and is 29 bits. In our project we consider various word-length. There is a trade-off between word-length, used resources and output precision, considering gives design flexibility. In other implementations, the controller does not have this flexibility. In previous works by using automated synthesis tools, the software considers many functional units such as adder and multiplier; as a result, the implementation cost increases. But in this work we design a controller with minimum functional units (only two adders and two multipliers). The area on chip of these functional units is variable and dependent on word length.

6 Conclusions

In this article, a low-cost architecture for a digital controller to improve dynamic response of an AC/DC three phase rectifier is presented. For designing this controller we have used predictive control algorithm.

This scheme predicts behavior of future input currents for each switching state of the converter. The cost function appraises predicted value for input currents with their references at the end of each sampling time
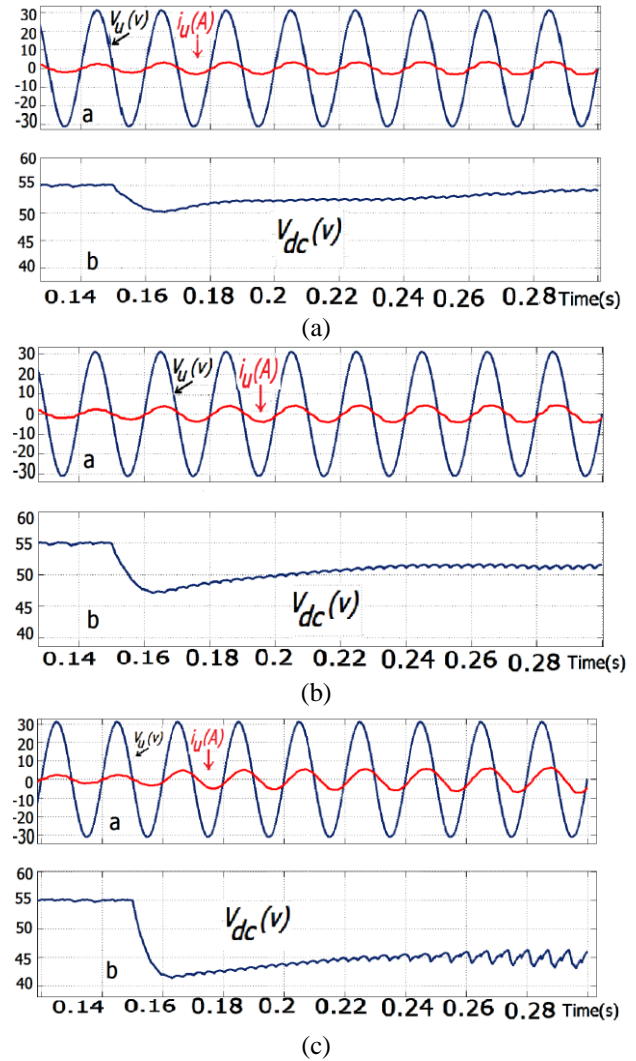

Fig. 9 Results for WL=15 a) Load changing from 30Ω to 20Ω, b) Load changing from 30Ω to 15Ω and c) Load changing from 30Ω to 10Ω.

Table 3 Summary of the results for all conditions.

	load changing from 30Ω to 20Ω				load changing from 30Ω to 15Ω				load changing from 30Ω to 10Ω			
	THD%	Power factor	Recovery time(s)	Undershoot(v)	THD%	Power factor	Recovery time(s)	Undershoot(v)	THD%	Power factor	Recovery time(s)	Undershoot(v)
WL=32	3.22	1	0.05	3.5	3.39	1	0.1	7	3.39	0.13	0.12	12
WL=24	4.45	1	0.07	4	4.55	1	0.12	8	4.67	0.1	0.15	13
WL=15	7.15	1	0.15	5	7.2	1	0.17	8	7.5	0.08	0.19	13

and minimizes the error between them and then the optimum switching states apply to power switches. Another concept that has used for controller design is fixed-point computation. The designed hardware is examined in three word lengths to evaluate the computation precision. The main purpose of this design is to minimize the transient time, overshoot/undershoot current and THD of input currents. In this work by using minimal functional unit (low cost architecture) we design a controller that its results show more accuracy in the computation and improvement in the dynamic response of the proposed converter. There is a tradeoff between architecture cost and accuracy of output parameters.

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