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High-Speed and Low-Power Flash ADCs Encoder

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Abstract: This paper presents a high-speed, low-power and low area encoder for implementation of flash ADCs. Key technique for design of this encoder is performed by convert the conventional 1-of-N thermometer code to 2-of-M codes (M = ¾ N). The proposed encoder is composed from two-stage; in the first stage, thermometer code are converted to 2-of-M codes by used 2-input AND and 4-input compound AND-OR gates. In the second stage by two ROM encoders, 2-of-M codes determine n-1 MSB bits and one LSB bit. The advantages of the proposed encoder rather than other similar works are high speed, low power consumption, low active area, and low latency with same bubble error removing capability. To demonstrate the mention specifications, 5-bit flash ADCs with conventional and proposed encoders in their encoder blocks, are simulated at 2-GS/s and 3.5-GS/s sampling rates in 0.18-μm CMOS process. Simulation results show that the ENOB of flash ADCs with conventional and proposed encoders are equal. In this case, the proposed encoder outputs are determined almost 30-ps faster rather than the conventional encoder at 2-GS/s. Also, the power consumptions of the conventional and proposed encoders were 17.94-mW and 11.74-mW at 3.5-GS/s sampling rate from a 1.8-V supply, respectively. Corresponding, latencies of the conventional and proposed encoders were 3 and 2 clock cycles. In this case, number of TSPC D-FFs and logic gates of the proposed encoder is decreased almost 39% compared to the conventional encoder.

Keywords: Flash ADC, Encoder, Thermometer Code, Bubble Error.

1 Introduction

Generally, 4 to 6 bits flash ADCs are used as the first choice for applications at conversion rates of 1-GHz or beyond with the lowest latency rather than other ADCs [1]. Flash ADCs are consists of various blocks, which each one plays special role to convert the analog input signal to digital binary bits. Since, one of the main blocks is encoder, which is placed in the end of the flash ADC and converts the output thermometer codes of comparison chains to the binary bits. Various structures have been designed to implement the encoder block of flash ADCs [1-24]. In this case, ROM-based encoder, because of its low-power, low-area, regularity structure (only need for local connections to convert the thermometer code to 1-of-N code) is extensively used to implement the encoder block of 5-bit and higher ones flash ADCs [5-25]. So, in this paper the ROM-based encoder is called as conventional encoder.

Encoder in [1] has been implemented with different series logic gates such as AND, NAND, and XOR. Encoder in [2] has been achieved as a series combination of full adder circuits. Also, encoder in [3] has been implemented with series NOR gates. Although encoders in [1-3] remove the bubble error and would be created maximum 3-LSB error in binary output bits of ADC. As all of these encoders include high delay because of using series logic gates; therefore at high-speed applications they should be used flip-flips or latches in between of these gates. It leads to increase complexity, power consumption, active area, and latency. In addition, to implement entire gates of these encoders require to complementary inputs (T and $\overline{\text{T}}$). Also, using encoder [1] requires that signals from different areas of chip be logically combined. Therefore, in implementations with 5 to 8-bit resolution, the wiring capacitance of these signals becomes substantial.

As known the conventional encoder is consists of two-

stages as shown in Fig. 1(a). In the first stage of conventional encoder, thermometer codes have been converted to 1-of-N code by an array of 2-input or 3-input AND gates (3-inputs AND gates use to remove the bubble error); and in its second stage, a ROM encoder has been used to determine the binary output bits. In Fig. 1(b), circuit structure of the 3-bit conventional encoder is illustrated. The conventional encoder provides better performance compared to other encoders in terms of delay, power consumption, and latency. But, in the conventional encoder, the output nodes capacitor of the ROM encoder is large, because of 2^{n-1} paralleled NMOS transistor with each other. Hence the determination of the output binary bits will be delayed. However, in high-speed applications, ROM encoder must divide into multi sub-blocks with TSPC-DFFs in between them; that cause to higher power consumption, and latency of conventional encoder [8-10].

In this paper, a high-speed, low-power and low area encoder designed in two-stages for n-bits flash ADCs by improving the conventional encoder based on an idea about converting the conventional 1-of-N thermometer codes to 2-of-M code. In the first stage of proposed encoder, the thermometer code are turned to 2-of-M codes using 2-input AND and 4-input compound AND-OR gates; and in its second stage, 2-of-M codes would be converted to n-1 MSB bits and one LSB bit using two ROM encoders. These ROM encoders are composed of Pseudo-NOR gates that each of these gates are implemented by 2^{n-2} NMOS and 1 PMOS transistors.

This paper is organized as follow. In the second section, design of the proposed encoder and its performance are presented in detail. In the third section, the simulation results of proposed encoder are introduced and compared to conventional encoder. Finally, fourth section concludes the paper.

2   Proposed Encoder

The encoder is an essential block in the flash ADC and the design of this block is very effective on the ADC performance. It should be able to properly handle the Comparison Chains (C.C) and remove bubble errors in the thermometer code.

Fig. 2(a) shows the general structure of an n-bit flash ADC. As it is observed in this figure, the analog input signal is sampled by T/H circuit and it is applied to the pre-amplifiers block in order to be strengthened. Then, the amplified signal is delivered to the comparison chains stage. As it is mentioned, the comparison chains outputs are the thermometer codes and these codes must be converted to the digital binary bits by the encoder block that is designed in two stages as shown in Fig. 2(b). In the first stage of proposed encoder, 2^{n-1} 2-input AND and 2^{n-2} 4-input compound AND-OR gates are used to turn the thermometer codes to 2-of-M codes,

and in the second stage, two parallel ROM-based encoders are used to convert the 2-of-M codes to the digital binary bits.

According to Fig. 2(b), one of these 2-of-M codes is between G_{01} to G_X (1-of-X code) and another is between g_{01} to g_Y (1-of-Y code) codes (M = X + Y). To determine the G_i codes (1-of-X code), 2^{n-1} 2-input AND gates which shown with symbol "A" in Fig. 2(b) and their transistor structure is shown in Fig. 2(c), are used. The inputs of these gates are two consecutive even thermometer codes, respectively (e.g.: $T_{02} - \overline{T}_{04}$, $T_{04} - \overline{T}_{06}$, ⋯). In accordance with applied thermometer codes, one of the outputs of these gates is logic zero and another would be logic one. These outputs are applied to the ROM encoder (second stage) which is consists of the n-1 Pseudo-NOR gates. Finally, the ROM encoder determines n-1 MSB bits of the ADC, B_1 to B_{n-1}. Also, 2^{n-2} 4-input compound AND-OR gates shown with symbol "B" in Fig. 2(b), are used to determine the g_i codes (1-of-Y code) that their transistor structure is shown in Fig. 2(c). In this case, the inputs of compound AND-OR gates are the odd thermometer codes and their next even codes (e.g.: [$T_{01} - \overline{T}_{02}$, $T_{03} - \overline{T}_{04}$]; [$T_{05} - \overline{T}_{06}$, $T_{07} - \overline{T}_{08}$]; ⋯). In accordance with applied thermometer code, one of the outputs of compound AND-OR gates is logic one and another would be zero. Finally, to determine the LSB bit, B_0, the outputs of these gates are applied to the ROM encoder (second stage) which is consists of a Pseudo-NOR gate. For better understanding, determination method of binary output bits for the 3-Bit proposed encoder is illustrated in the Fig. 3. According to Fig. 3, the Pseudo-NOR gates of the proposed encoder second stage are implemented with half NMOS transistors of the Pseudo-NOR gates of the conventional encoder second stage in Fig. 1(b).

2.1 Speed and Latency of the Proposed Encoder

In order to increase the speed of flash ADC, all of its blocks must have high speed to avoid making difficulties for the final speed of ADC. The proposed encoder speed is determined through the loading effect of first stage on the comparison chains and delays of the first and second stages. As it is observed in Fig. 2, T_i and Tb_i outputs of the even comparison chains are connected to one and two NMOS transistors in the first stage of proposed encoder, each with size of 2 (W/L), respectively. Also, T_i output of the odd comparison chains are connected to one NMOS transistor in the first stage of proposed encoder with size of 2 (W/L). Also, according to Fig. 1, T_i and Tb_i outputs of the comparison chains are connected to one and one NMOS transistor in the first stage of conventional encoder with 2-input AND gates in its first stage, each with size of 2 (W/L), respectively; and with 3-input AND gates in its first stage, are connected to one and two NMOS
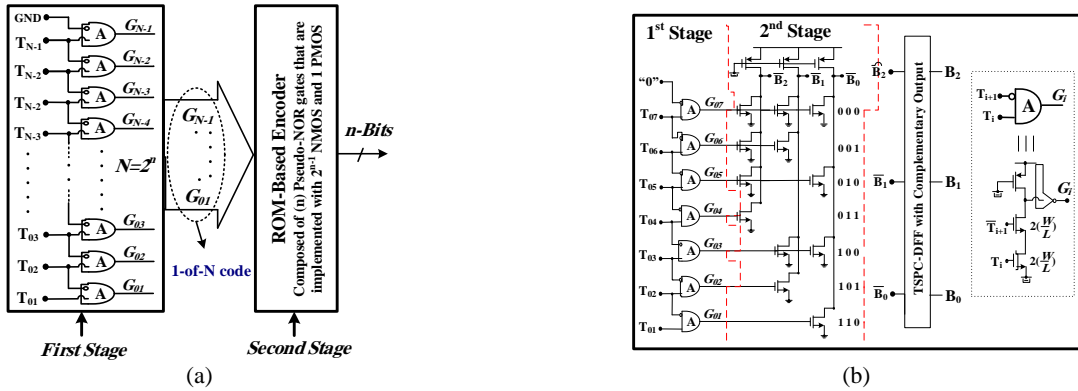
Fig. 1 a) The n-bit conventional encoder structure and b) circuit structure of the 3-bit conventional encoder.
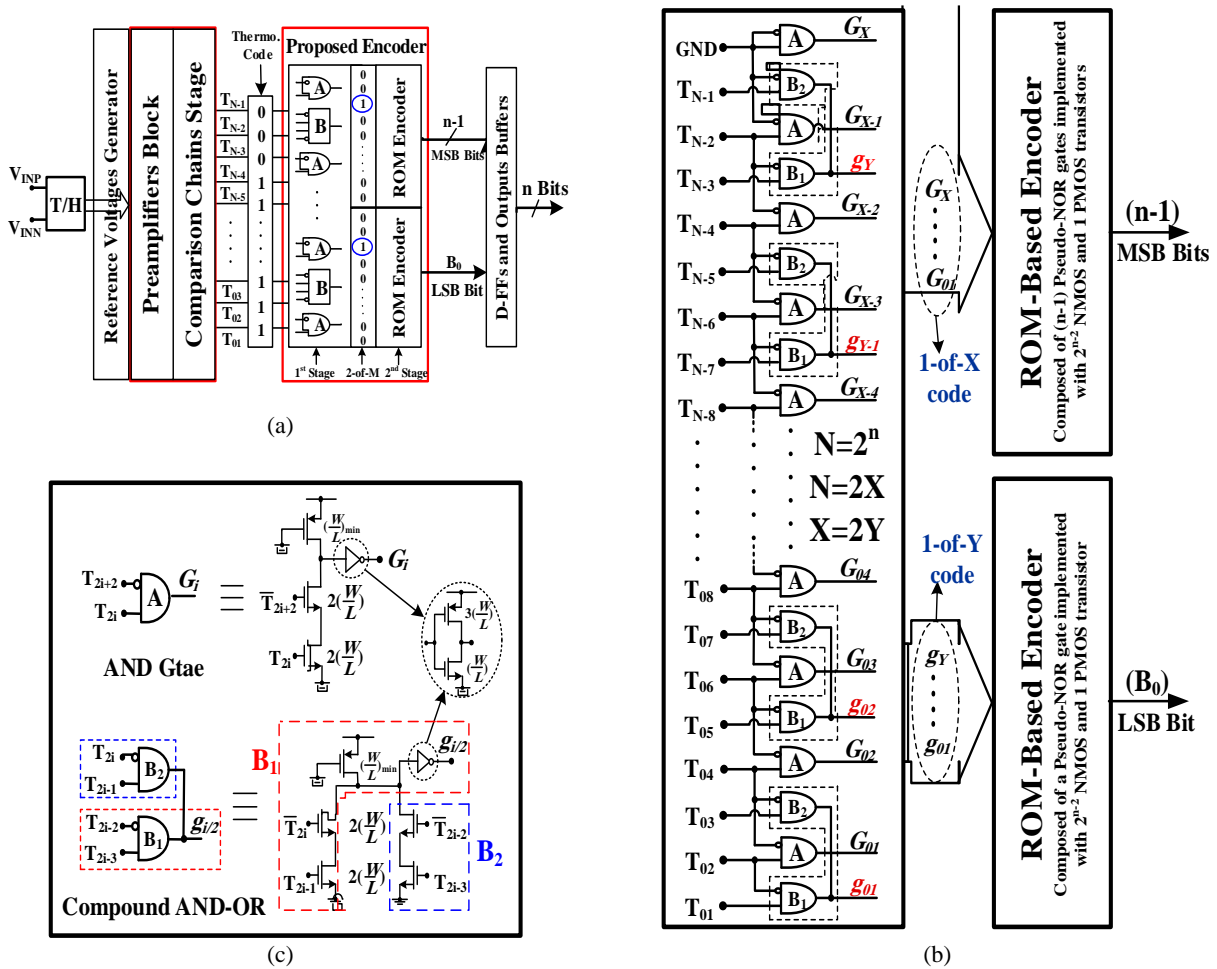

Fig. 2 a) The general structure of n-bit flash ADC with schematic of the proposed encoder in its encoder block, b) The n-bit proposed encoder and c) Transistor level implementation of AND gates and compound AND-OR gates with their dimensions.

transistors, each with size of 3 (W/L), respectively. Then the maximum loading effect of AND gates and compound AND-OR gates on the comparison chains outputs for the proposed encoder is 6 (W/L) and for the conventional encoder with 2-input or 3-input AND gates are 4 (W/L) or 9 (W/L), respectively. Then, the ratio of loading effects of the proposed and conventional encoders is 6/4 (for 2-input AND gates) or 6/9 (for 3-input AND gates), and these ratios will be same at different sampling rates. Therefore, the loading effects of the proposed and conventional encoders on the ADC comparison chains outputs are approximately same. So, it can be realized that the proposed encoder almost would not change determination speed of T_i and Tb_i outputs (thermometer codes) compared to the conventional encoder.

In the conventional encoder, the outputs of first stage (1-of-N code) are applied to a ROM-based encoder

which consist of n Pseudo-NOR gates. So that each of the Pseudo-NOR gates of conventional encoder have been implemented with 2^{n-1} NMOS and 1 PMOS transistors (totally $n \times 2^{n-1}$ transistor). But, in the proposed encoder, outputs of the first stage (2-of-M codes) are applied to two ROM-based encoder which are consist of n Pseudo-NOR gates. Since, each of the Pseudo-NOR gates are implemented with 2^{n-2} NMOS and 1 PMOS transistors (totally $n \times 2^{n-2}$ transistor). Therefore, reducing the number of NMOS transistors in Pseudo-NOR gates decrease their input/output nodes parasitic capacitors. Consequently it can be written:

$$t_{d\text{-}2nd,n+1\text{-Bit}}(P) = t_{d\text{-}2nd,n\text{-Bit}}(C) \tag{1}$$

where $t_{d\text{-}2nd,n+1\text{-Bit}}(P)$ and $t_{d\text{-}2nd,n\text{-Bit}}(C)$ are the second stage delays of n+1-bit proposed encoder and n-bit conventional encoder, respectively. Then, the second stage speed of proposed encoder will increase rather than the conventional encoder (e.g. for 3-Bit conventional and proposed encoders in Figs. 1(b) and 3. In this case, the second stage of proposed encoder can

implement with half sub-blocks that are used in the second stage of conventional encoder in high-speed applications. For better understanding of this issue and compare the performance of the proposed and conventional encoders in high-speed applications, design structures of these encoders for a 5-bit flash ADC are illustrate in Fig. 4. In Fig. 4, to increase the speed of both encoders, their first stages are implemented in NAND/NOR structure. In this case, the maximum speeds of proposed and conventional encoders could be determined based on delay of the slowest stage. Therefore, due to used similar structure and gates, the maximum speeds of proposed and conventional encoders are approximately equal. Also, the maximum speed for n-bit proposed and conventional encoders are independent of encoder resolution. Note, in Fig. 4(a), because delay of pseudo-NOR gates in the ROM-based encoder of conventional encoder (second stage) is more then to its first stage; therefore, to have maximum speed, second stage of conventional encoder is partitioned to two pipeline stages with TSPC-DFFs in
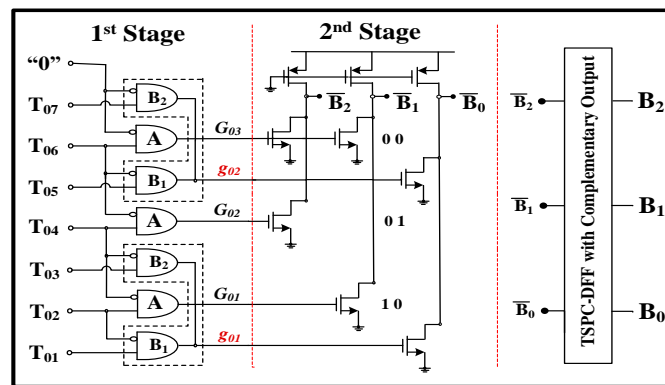

Fig. 3 Circuit structure of the 3-Bit proposed encoder.

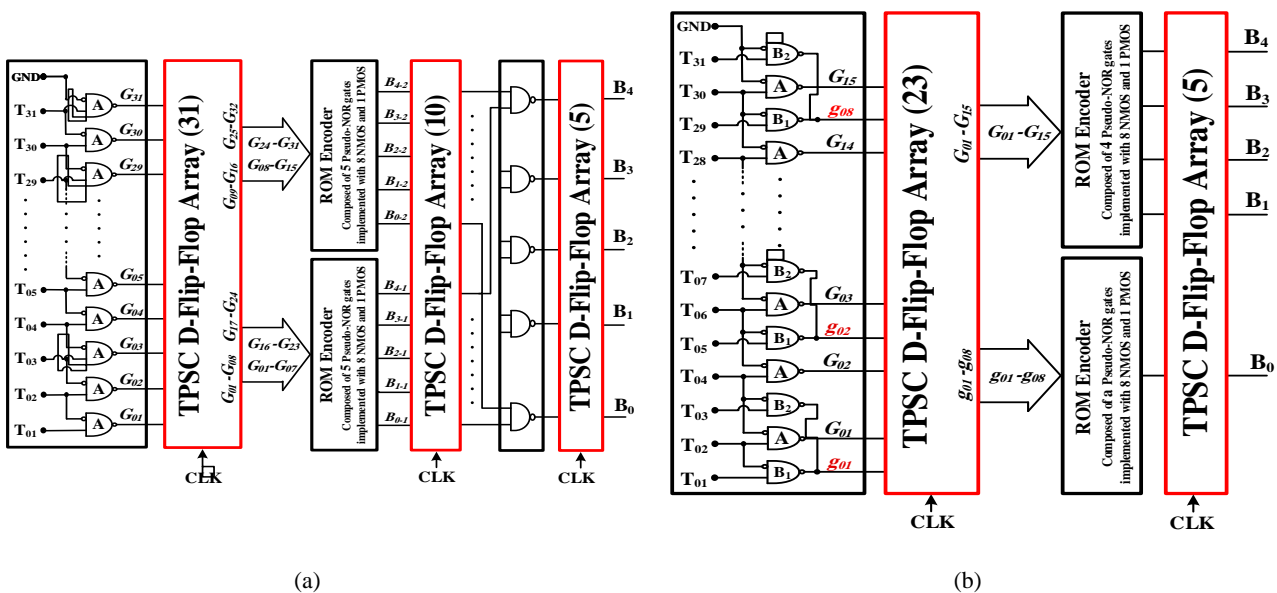(a)   (b)

Fig. 4 Structure of the proposed and conventional encoders in high-speed applications. a) The conventional encoder and b) The proposed encoder.

between of them to decrease the delay of its second stage and increase of its operational speed that cause to increase of the latency, power and area of conventional encoder compared to the proposed encoder [8-10].

According to Fig. 4, the maximum latency of the 5-bit proposed encoder is equal to two clock cycles and for 6 to 8-bit high-speed proposed encoders would be equal to three clock cycles. Where the latency for the 5 to 7-bit high-speed conventional encoder is equal to three clock cycles and for 8-bit is four clock cycles.

2.2 Power Consumption and Occupied Area of the Proposed Encoder

The power consumption and occupied area of the proposed encoder especially in high-speed applications are decreased compared to the conventional encoder due to reducing the dynamic power consumption, power dissipation of clock signal, number of D-FFs and logic gates. According to Fig. 4, the clock consumption, number of TSPC-DFFs and logic gates of 5-bit proposed encoder is decreased approximately 39% rather than the conventional encoder and also for 6-bit and 7-bit high-speed proposed encoders, these parameters decrease approximately 30% and 32% compared to the conventional encoder, respectively.

The numbers of logic gates and TSPC-DFFs for implementation of n-bit high-speed proposed and conventional encoders are summarized in Table 1.

2.3 Bubble Error Removing in the Proposed Encoder

For very fast input signals, small timing differences between the response time of the comparators with unfavorable offset voltages in the comparators can cause a situation where a zero is found between the "1"s. This is called a "bubble error" in the thermometer codes. This error causes incorrect determination on ADC binary output bits. The bubble error could not be removed in the comparison chains of ADC. Therefore, this error must remove in the encoder block.

The bubble error will be removed in the first stage of proposed encoder. To simplify the matter how to remove the bubble error in the proposed encoder, the thermometer codes of a 4-bit ADC are considered in three possible situations as shown in Fig. 5. In the first situation, assume there is no bubble error in the thermometer code; two determinant codes (2-of-M codes) of the binary output bits in Fig. 5(a) are G_{05} and g_{03}. In this case, binary output bits of the ROM encoders

will be "1011", where it is expected. In the second situation, assume there is a bubble error in the odd thermometer code (e.g.: T_{11}). In this case, two determinant codes (2-of-M codes) of the binary output bits in Fig. 5(b) are G_{06} and g_{04}. The binary output bits of the ROM encoders would be "1100", where it is expected. It means that the bubble error is removed. In the third situation, assume there is a bubble error in the even thermometer code (e.g.: T_{12}). In this case, two determinant codes (2-of-M codes) of the binary output bits in Fig. 5(c) are G_{05} and g_{03}. Naturally, the expected binary output bits of ROM encoders are "1101", where the binary output bits will be "1011". Then, it can be realized that only a ROM line in the ROM-based encoder is always selected in each three situations and the maximum error will be 2-LSB in the binary output bits if bubble error happens in the even thermometer code.

3 Simulation Results

To compare and show better performance of the proposed encoder rather than the conventional encoder, the thermometer code of a 5-bit flash ADC at 2-GS/s sampling rate with nyquist rate input frequency, as illustrated in Fig. 6, are applied to these encoders. The encoders are simulated in 0.18μm CMOS technology with $V_{DD} = 1.8$-V. In this case, latencies of encoders are quantified in term of clock cycle and the simulations are explained with same transistor dimensions. In Fig. 6, three SR-latches are pipelined for the meta-stability error removing.

In order to compare the loading effect of proposed and conventional encoders on the ADCs comparison chains outputs, these outputs are simulated and their results are shown in the Fig. 7(a) (in Fig. 7 "C" refers to conventional and "P" refers to proposed). In this figure, it is obviously observed that the delays in determination of the comparison chains outputs are approximately same. Therefore, the proposed encoder almost will not change determination speed of the T_i and T_{bi} outputs (thermometer code) compared to the conventional encoder. Also, two encoders are evaluated in term of the delay on outputs determination of the first and second stages of encoders that simulation results are shown in the Figs. 7(b) and 7(c), respectively. Fig. 7(b) shows that the delays of the first stages of proposed and conventional encoders are same and equal to t_{d-up}. Also, according to Fig. 7(c), the second stage of

Table 1 Comparison of the number of logic gates and TSPC-DFFs for implementation of n-bit high-speed proposed and conventional encoders.

	First Stage		Second Stage	Total Stages
Encoder	2-input NAND	8-input Pseudo-NOR	2, 4 or 8-input Pseudo-NOR	TSPC-DFFs
Conventional	N	N.K	α.n	$N+(N.K+\alpha.n)$
Proposed	M	N.(K/2)	β.n	$M+(N.[K/2]+\beta.n)$

Note: The $\beta = 0$ for 5-bit and $\beta = 1$ for 6 to 8-bit proposed encoder. Also, $\alpha = 1$ for 5 to 7-bit conventional encoder and $M = (3/4).N$ and $K = n/16$.
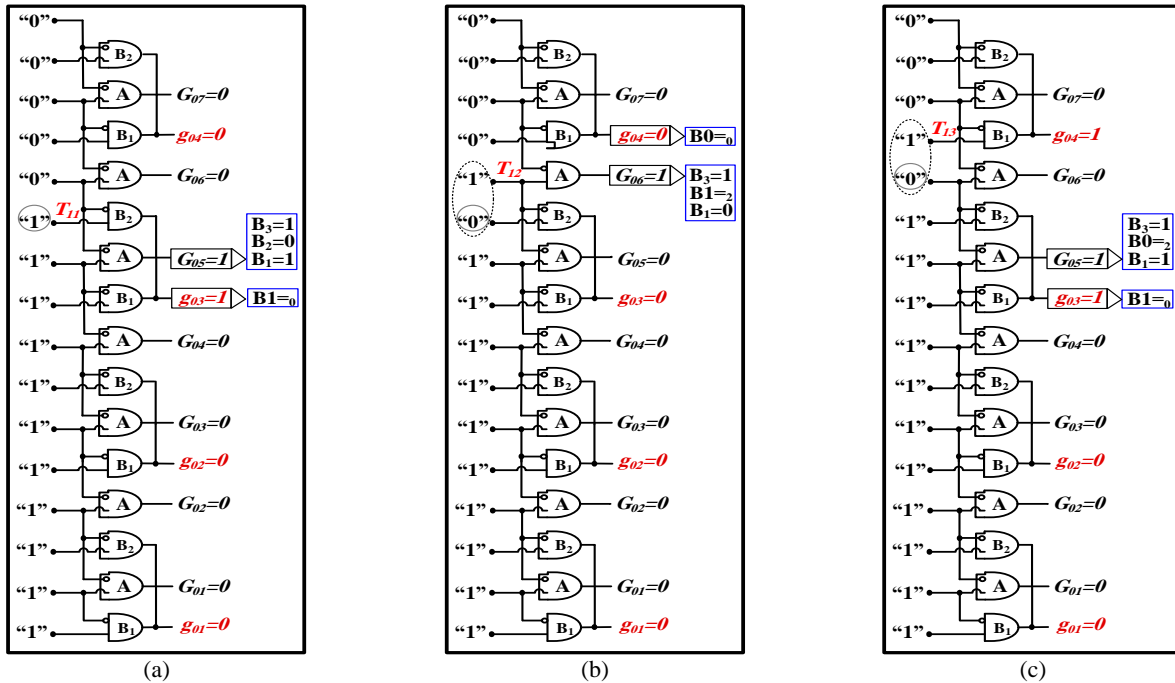
Fig. 5 First stage of the 4-bit proposed encoder. a) An example for no bubble error in thermometer code, b) Bubble error in odd thermometer code (e.g.: in T_{11}) and c) Bubble error in even thermometer code (e.g.: in T_{12}).
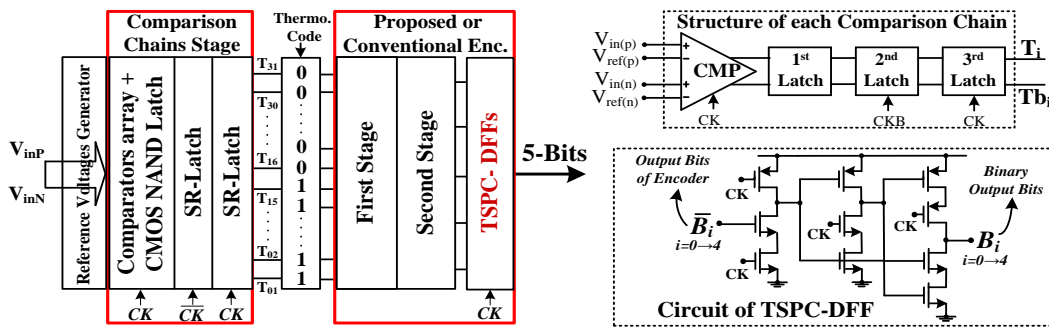

Fig. 6 The structure of designed 5-bit flash ADCs with the proposed and conventional encoders in their encoder block at 2-GS/s.

proposed encoder are determined 30-ps (12%) faster compared to the conventional encoder; because the Pseudo-NOR gates in the ROM encoders of proposed encoder are implemented with half NMOS transistors (8 NMOS Tr.) compare to Pseudo-NOR gates in the ROM encoder of conventional encoder (16 NMOS Tr.). Therefore, it confirms higher speed of the second stage of proposed encoder rather than the conventional encoder and with increasing the encoder resolution; the speeds of second stages will be more different.

The FFT analysis of two 5-bit flash ADCs at 2-GS/s sampling rate are shown in Fig. 8. It shows that the ENOB of two 5-bit flash ADCs with proposed and conventional encoders are same. In this case, power dissipations of proposed and conventional encoders were 2.37-mW and 2.58-mW, respectively. Also, the ADCs power dissipations without their encoder power are same and equal to 22.28-mW.

The amounts of SNDR and SFDR versus input frequency of two 5-bit flash ADCs at 2-GS/s are shown

in Fig. 9. This figure shows that the SNDR and SFDR of two flash ADCs are same in entire input frequencies. Therefore, the proposed encoder does not change SNDR and SFDR of flash ADC rather than the conventional encoder.

Also, for high-speed applications, two 5-bit flash ADCs at 3.5-GS/s sampling rate are designed and simulated that results are summarized in Table 2. In this case, flash ADCs are implemented with proposed and conventional encoders, according to Fig. 4, in their encoder block with same transistor dimensions (other blocks of ADCs considered similar together) that results are summarized in Table 2. Table 2 shows the better performance of the proposed encoder rather than the conventional encoder in terms of the power consumption, occupied area and latency when ENOB of two flash ADCs are same. In this case, the ADCs power dissipations without their encoder power are same and equal to 73.16-mW.

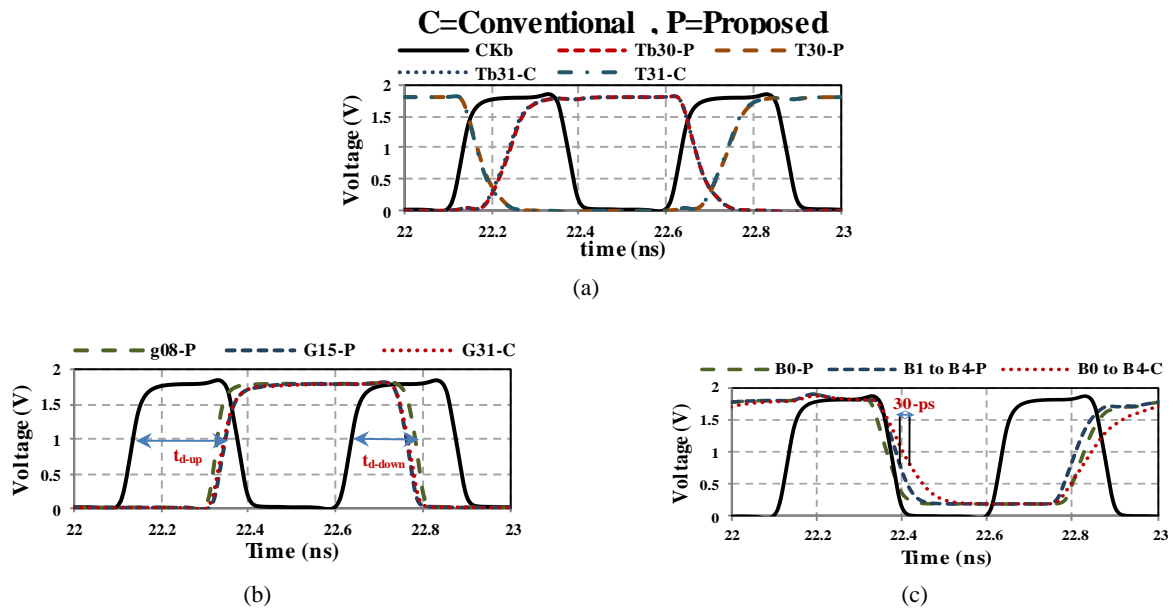The proposed encoder performance is compared with

(a)

(b)

(c)

Fig. 7 Comparison of simulation results (stages delay) of the proposed and conventional encoders. a) Delays in output determination of ADCs comparison chains, b) The delays in output determination of first stages and c) The delays in output determination of second stages.
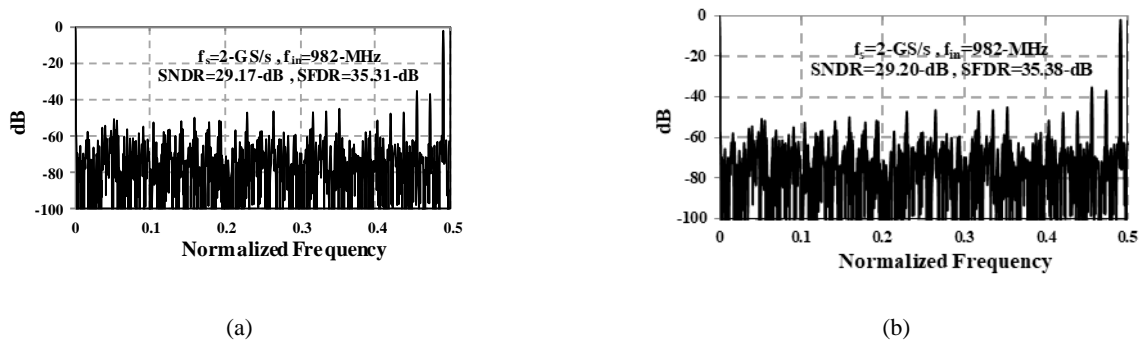

(a)

(b)

Fig. 8 The FFT analysis at 2-GS/s with fin=982-MHz. a) The flash ADC with conventional Encoder and b) The flash ADC with proposed Encoder.
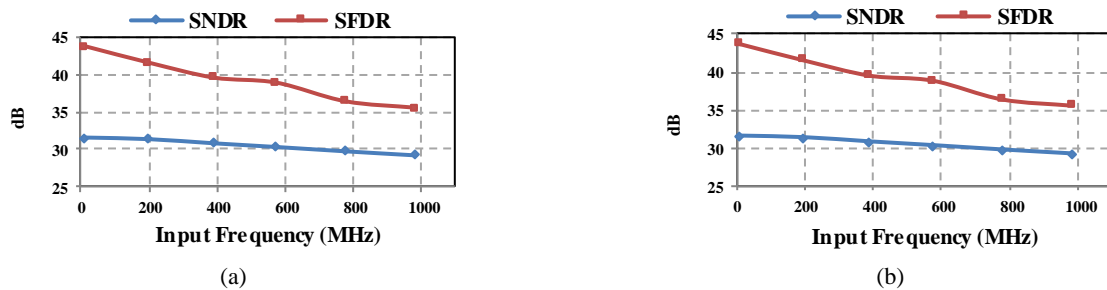

(a)

(b)

Fig. 9 SNDR and SFDR at 2-GS/s. a) The flash ADC with conventional encoder and b) The flash ADC with proposed encoder.

other works in Table 3. This table confirms the better power consumption and latency of proposed encoder compared to other works at same sampling rates.

4 Conclusion

In this paper, a high-speed, low-power and low-area encoder is designed for flash ADCs. Key technique for design of this encoder is performed by convert the conventional 1-of-N thermometer code to 2-of-M codes (M = ¾ N). The proposed encoder includes high speed rather than the conventional encoder. Higher speed of the proposed encoder is resulted reducing the output nodes parasitic capacitor and number of NMOS transistors in Pseudo-NOR gates of ROM-based encoders.

Also, in high-speed applications, the power

Table 2 Simulation results of the proposed and conventional encoders.

Parameters	Conventional *	Proposed
Sampling Rate	3.5-GS/s	3.5-GS/s
Input Frequency	1.05-GHz	1.05-GHz
Power consumption	6.07-mW	4.28-mW
Clock Power Dissipation	11.87-mW	7.46-mW
Latency	3-CLK cycles	2-CLK cycles
Occupied Area (Number of Gates)	(46) TSPC-DFFs	(28) TSPC-DFFs
	(36) 2-input NAND	(31) 2-input NAND
	(10) 8-input Pseudo-NOR	(5) 8-input Pseudo-NOR
Power of Comparison Chains	27.25-mW	27.33-mW
Total Power of ADC	91.02-mW	84.90-mW
ENOB of ADCs	3.76-Bit	3.78-Bit

* The conventional encoder is used to implement the encoder block of Flash ADCs in [5-25].

Table 3 Comparison of proposed encoder performance with other works.

	Tech.	Sampling Rate	Resolution	ADC ENOB	Encoder Power (P_{EN})	Encoder Latency	P_{EN}/P_{ADC}	ADC FOM
[1]	180-nm	4-GS/s	4-Bit	2.75-Bit	8-mW	2-CLK	18.6%	2.14@3-GS/s f_{in}=Nyquist
[4]	180-nm	1.6-GS/s	4-Bit	3.7-Bit	2.28-mW	1.5-CLK	15%	0.69@1.6-GS/s f_{in}=Nyquist
[5]	90-nm	3.5-GS/s	5-Bit	3.63-Bit	17-mW	3-CLK	12.9%	3.05@3.5-GS/s f_{in}=1-GHz
[9]	90-nm	3.5-GS/s	6-Bit	4.89-Bit	21.56-mW	4-CLK	22%	1.09@3.5-GS/s f_{in}=Nyquist
[Proposed]	180-nm	2-GS/s	5-Bit	4.56-Bit	2.37-mW	1-CLK	9.2%	0.56@2-GS/s f_{in}=Nyquist
[Proposed]	180-nm	3.5-GS/s	5-Bit	3.78-Bit	11.74-mW	2-CLK	13.8%	1.77@3.5-GS/s f_{in}=1.05-GHz

Note: PADC is total power consumption of flash ADC.

dissipation and occupied area of the proposed encoder are decreased compared to the conventional encoder that these specifications are resulted reducing the clock consumption, number of D-FFs and logic gates of the proposed encoder. The bubble error removing capabilities of the proposed and conventional encoders are same. In this case, the maximum error of proposed encoder is 2-LSB that is acceptable then to the other encoders.

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