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Compact Lossy Inductance Simulators With Electronic Control

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Abstract: In this paper two R-L network simulator configurations employing a single VDDIBA, one resistance and one grounded capacitance are presented. The first configuration is a grounded series resistor-inductor (R-L) network simulator and the second configuration is intended for grounded parallel resister-inductor (R-L) circuit simulation. Both the proposed circuits enjoy several beneficial features such as: 1) compact structure employing only one VDDIBA and two passive elements, 2) electronic tuning of inductive part of realized series/parallel R-L impedances, 3) independent control of inductive and resistive parts of realized parallel R-L impedance, 4) no requirement of any component matching, and 5) un-deviated performance in non-ideal environment. By choosing appropriate values of active/passive elements, a series R-L circuit for simulating resistance of 7.742 kΩ and inductance of value 7.742 mH has been developed. Similarly a parallel R-L simulation circuit to simulate a resistance of value 1 kΩ and inductance of value 77.4 µH is implemented. To study the influence of parasitics on developed lossy inductances, the behavior of these configurations has been studied keeping terminal parasitics of VDDIBAs under consideration. To check the performance and usefulness of the proposed configurations some second-order filtering circuits have been designed. To confirm the theoretical analysis, PSPICE Simulation results have been included.

Keywords: Active RL Networks, Compact Circuit, Electronic Control, VDDIBA.

1 Introduction

AN inductor is a very useful passive element which finds very frequent applications in circuits and electrical engineering. The working of conventional spiral inductors is not matched with the ideal behavior. The conventional spiral inductors also suffer from large weight and size, generation of undesired harmonics, electromagnetic radiations and strong parasitic effects. Therefore, in the last two decades, interest has been comprehensively directed towards the realization of synthetic inductors employing different active elements for simulating the behavior of passive conventional inductors. Several grounded inductance realizations employing different active components have been described in open literature [1-8]. In addition to the simulation of lossless inductors, the simulation of lossy inductors is also found very useful. The grounded lossy inductance simulators have a wide range of applications covering series/parallel resonance circuits, filters and sinusoidal oscillators. Several grounded R-L (series/parallel) network simulation circuits employing numerous active elements such as OP-AMPs, current conveyors, current feedback amplifiers, Four terminal floating nullers, operational trans-resistance amplifiers, differential voltage current conveyor, current-feedback operational-amplifiers, dual X-current conveyors and voltage differential current conveyors have been introduced in literature[9-30]. On careful investigation of previously reported series/parallel R-L simulation circuits, it is observed that all these reported circuits have one or more of below given disadvantageous features:

(i) Employment of excessive number of active building blocks(ABBs) (more than one);

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(ii) Employment of excessive number of passive components (more than two);
(iii) Employment of floating capacitance(s);
(iv) Lack of electronic control of realized equivalent resistances and inductances;
(v) Non-availability of independent tuning of realized equivalent resistances and inductances and;
(vi) Requirement(s) for matched active/passive components.

Therefore, the main aim of this article is to present new grounded lossy inductor simulators (series R-L, parallel R-L) with following useful features:

(1) Employment of single active Element (VDDIBA);
(2) Use of Two Passive Elements;
(3) Use of single Grounded Capacitance;
(4) Availability of Electronic Tuning of Realized Equivalent Inductance;
(5) Availability of Non-Interactive Tuning Of Realized Inductance;
(6) No Requirement of matched passive or active elements;
(7) Excellent working under non-ideal constraints with no deviation;
(8) Low Parasitic Effects.

The comparison of proposed grounded series R-L network simulator shown in Fig. 2 with previously proposed series R-L simulators has been given in Table 1. Similarly proposed grounded parallel R-L simulator (shown in Fig. 3) has been compared with previously reported parallel R-L simulators in Table 2.

2 Voltage Differencing Differential Input Buffered Amplifier (VDDIBA)

VDDIBA is a popular circuit idea proposed in [33]. It is a very useful ABB with electronic controllability feature. The symbolic block representation of VDDIBA is given in Fig. 1. VDDIBA has five input/output ports namely *V*-, *V*+, *W*, *V*, and *Z*. The voltage difference of terminals *V*+ and *V*- is transferred to *Z* terminal in the form of current. The voltage difference between the *V* and *Z* terminals is transferred at terminal *W* through a differential buffer of unity gain. The voltage-current relationships between different ports of VDDIBA have been given by Eqs. (1)-(3) in static (steady-state situation). The implementation of VDDIBA circuit concept using operational transconductance amplifiers (OTAs) and current feedback operational amplifier (CFOA) is demonstrated in Fig. 2. The CMOS realization of OTAs used in Fig. 2 has been shown in Fig. 3.

$$I_Z = \beta_Z g_m \left(V_{V+} - V_{V-}\right) \tag{1}$$

$$V_W = V_Z - V_V \tag{2}$$

$$I_{V+} = I_{V-} = I_V = 0 \tag{3}$$

The use of VDDIBA in various analog signal processing circuits has been discussed in [34-37]. Grounded lossless inductor simulator employing positive type VDDIBA has been discussed in [34] which employ two

Table 1 Comparison of proposed series R-L simulator with previously reported series R-L simulation circuits.

Ref.	Fig. No.	No. of Active Element	No. of Resistors	No. of Capacitors	Electronic Control of L_{eq} and R_{eq}	Non-Interactive Control of L_{eq}	Need for Element Matching
[10]	Fig. 2(a)	1	1(F)+1(G)	1(F)	No	No	No
[11]	Fig. 1	1	1(F)+1(G)	1(F)	No	No	No
	Fig. 2	2	1(F)+1(G)	1(F)	No	Yes	No
	Fig. 2	2	2(F)+1(G)	1(G)	No	Yes	No
	Fig. 2	2	1(F)+1(G)	1(F)	No	Yes	No
[13]	Figs. 1(a)-(b)	2	2(F)+2(G)	1(G)	No	Yes	Yes
[14]	Fig. 1	1	3(F)+1(G)	1(G)	No	Yes	No
[15]	Fig. 1(a)	1	4(F)+1(G)	1(G)	No	Yes	No
	Fig. 1(c)	1	3(F)+1(G)	1(F)	No	Yes	No
[16]	Fig. 1	1	2(F)+2(G)	1(F)	No	Yes	Yes
[17]	Fig. 1	1	1(F)+1(G)	2(G)	No	Yes	Yes
[18]	Fig. 2(b)	1	1(F)+1(G)	1(F)	No	No	No
[20]	Fig. 2(a)	1	1(F)+1(G)	1(G)	No	No	No
	Fig. 2(b)	1	2(F)+1(G)	1(F)	No	No	No
[23]	Figs. 2-5	1	1(F)+1(G)	1(F)	No	Yes	No
[25]	Fig. 2(b)	1	1(F)+1(G)	1(F)	No	No	No
[26]	Fig. 2(b)	1	2(F)	1(F)	No	Yes	No
	Fig. 2(f)	1	2(F)+1(G)	1(F)	No	No	No
[27]	Fig. 2(c)	1	1(G)	1(G)	No	Yes	No
[28]	Fig. 3	1	2(F)	2(F)	No	Yes	No
[29]	Fig. 13	1	1(G)+1(F)	1(F)	No	Yes	No
[30]	Fig. 3	2	4(F)+1(G)	3(F)	No	No	Yes
Proposed	Fig. 2(a)	1	1(F)	1(G)	Yes	Yes	No

G* Grounded, F* Floating

Table 2 Comparison of proposed parallel R-L simulator with previously reported parallel R-L simulation circuit.

Ref.	Fig. No.	No. of Active Element	No. of Resistors	No. of capacitors	Electronic Control of L_{eq} and R_{eq}	Non-Interactive Control of L_{eq}	Need for Element Matching
[9]	Fig. 1(a)	1	2(F)	1(F)	No	No	No
[12]	Fig. 2(a)	1	1(F)	1(G)	No	Yes	No
[15]	Fig. 1(b)	1	3(F)+1(G)	1(F)	No	Yes	No
[16]	Fig. 1	1	2(F)+2(G)	1(F)	No	Yes	Yes
[18]	Fig. 2(a)	1	1(F)+1(G)	1(F)	No	Yes	No
[19]	Figs. 2(a)-(b)	2	4(F)	1(F)	No	Yes	No
[20]	Figs. 3(a)-(b)	1	1(F)+1(G)	1(G)	No	No	No
[21]	Figs. 3(a)-(b)	1	1(F)+1(G)	1(F)	No	No	No
[22]	Fig. 2	1	1(F)+1(G)	1(G)	No	No	No
[24]	Fig.1	1	2(F)+2(G)	1(F)	No	No	No
[25]	Fig. 2(c)	1	1(F)+1(G)	1(F)	No	Yes	No
[26]	Fig .2(c)	1	2(F)+1(G)	1(F)	No	No	Yes
	Fig. 2(d)	1	3(G)	1(F)	No	No	No
	Fig. 2(e)	1	2(F)+1(G)	1(F)	No	Yes	No
[29]	Fig. 4(a)	1	2(G)	1(F)	No	Yes	No
[30]	Fig. 4	2	1(F)+3(G)	3(F)+2(G)	No	Yes	Yes
[31]	Fig. 2(a)	1	2(F)	1(G)	No	No	No
[32]	Fig. 1	1	2(F)	1(F)	No	No	No
	Fig. 2	1	2(F)	1(G)	No	No	No
	Fig. 3	1	3(F)	1(F)	No	No	No
Proposed	Fig. 2(b)	1	1(F)	1(G)	Yes	Yes	No

G* Grounded, F* Floating

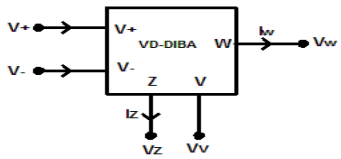

Fig. 1 VD-DIBA Symbol.

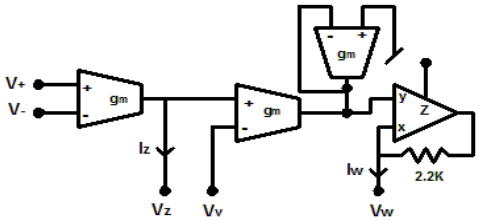

Fig. 2 VD-DIBA Circuit implementation using OTAs and CFOA.

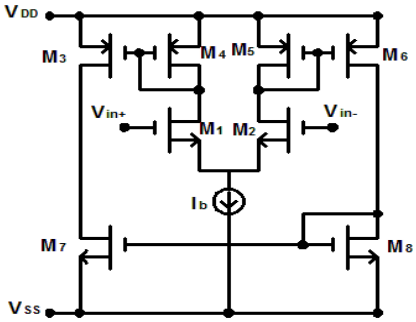

Fig. 3 CMOS realization of OTAs shown in Fig. 2.

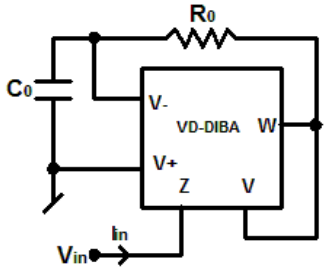

Fig. 4 Presented grounded series R-L simulation circuit.

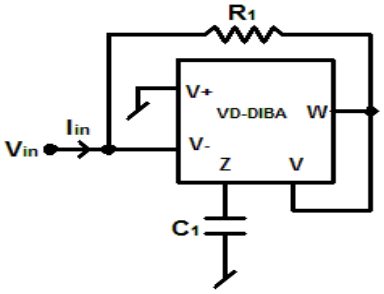

Fig. 5 Presented grounded parallel R-L simulation circuit.

positive types VDDIBAs one grounded capacitance and one floating resistance. Therefore implementation of RLC filters, series/parallel RLC resonance circuits and other useful applications in which grounded series/parallel RL networks are required employing circuit proposed in [34] will require large number of VDDIBAs and resistances as compared to implementation by VDDIBA based lossy inductors proposed in this paper.

3 Proposed Configurations

The proposed grounded series R-L and grounded parallel R-L impedance simulation circuits are given in Figs. 4 and 5, respectively. By simple mathematical analysis the expressions of input impedances of configurations shown in Figs. 4 and 5 have been evaluated and given in Table 3.

It can be seen from Table 3, that configurations are shown in Fig. 4 and Fig. 5 are realizing grounded series

Table 3 Input Impedances of proposed series/parallel RL simulators.

Fig. No.	Input Impedance	Type of Impedance Realized	Equivalent Inductance (L_{eq})	Equivalent Resistance (R_{eq})
Fig. 4	$\frac{2R_0sC_0}{g_m}+\frac{2}{g_m}$	$+L_{eq}$ series with $+R_{eq}$	$\frac{2R_0C_0}{g_m}$	$\frac{2}{g_m}$
Fig. 5	$\frac{1}{\frac{g_m}{2sC_1R_1}+\frac{1}{R_1}}$	$+L_{eq}$ parallel with $+R_{eq}$	$\frac{2C_1R_1}{g_m}$	R_1

Table 4 Input Impedances of proposed series/parallel RL simulators under non-ideal conditions.

Fig. No.	Input Impedance (Z_{in})	Type	Equivalent Inductance (L_{eq})	Equivalent Resistance (R_{eq})
Fig. 4	$\frac{R_0sC_0}{g_m}\left(\frac{1+\beta^-}{\beta^+}\right)+\frac{1}{g_m}\left(\frac{1+\beta^-}{\beta^+}\right)$	$+L_{eq}$ series with $+R_{eq}$	$\frac{R_0C_0\left(1+\beta^-\right)}{g_m\beta^+}$	$\frac{1}{g_m}\left(\frac{1+\beta^-}{\beta^+}\right)$
Fig. 5	$\frac{1}{\frac{g_m}{sC_1R_1}\left(\frac{\beta^+}{1+\beta^-}\right)+\frac{1}{R_1}}$	$+L_{eq}$ parallel with $+R_{eq}$	$\frac{R_1C_1\left(1+\beta^-\right)}{g_m\beta^+}$	R_1

R-L and parallel R-L networks. Both the configuration employs single VDDIBA along with single resistance and single capacitance. The placement of grounded capacitor in both circuit configurations makes them suitable for monolithic integration. The series R-L network simulator enjoys the electronic control of both inductive as well as the resistive parts by g_m along with the independent control of the inductive part by resistance R_0. Similarly, the parallel R-L simulator has the facility of independent electronic tunability of inductive part by g_m. To Study the behavior of proposed circuits under different non-ideal circumstances, analysis under non-ideal transfer ratios and analysis under parasitics have been carried out.

4 Non-Ideal Analysis

The voltage-current relationships among between terminals of VDDIBA under non-ideal voltage/transconductance transfer ratios conditions can be defined as;

$$I_Z = \beta_Z g_m \left(V_{V+} - V_{V-}\right) \tag{4}$$

$$V_W = \beta^+ V_Z - \beta^- V_V \tag{5}$$

$$I_{V+} = I_{V-} = I_V = 0 \tag{6}$$

where β^+ and β^- are the voltage transfer errors and β_z is transconductance error with a value slightly less than unity. On studying presented VDDIBA based series/parallel R-L simulation circuits under non-ideal conditions, the realized input impedances and their types can be found as given in Table 4.

On comparing the expressions of Table 3 with Table 4, it can be illustrated that the working of proposed simulators with non-ideal constraints remains the same as the ideal behavior. The values of R_{eq} and L_{eq} deviate from ideal values but as the values of β^+ and β^- are very near to unity, the deviations in values of R_{eq} and L_{eq} are very minute. Hence, even taking non-ideal constraints under consideration, the performance of developed simulators has a closed match with ideal performance.

5 Effects of VDDIBA Terminal Parasitics

In this section, the behavior of proposed series/parallel grounded R-L impedance simulators is evaluated under the presence of parasitic impedances of VDDIBA terminals. At high frequencies, the port parasitics of VDDIBAs become effective and influence the working of VD-DIBA based applications. In CMOS VDDIBA [34] at high frequencies, a finite grounded parasitic resistance R_Z along with finite grounded parasitic capacitances C_Z appears at Z ports.

The presented grounded series R-L circuit simulator shown in Fig. 4 is re-evaluated considering the port parasitics of VD-DIBA. The expression of the input impedance is found;

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{2R_Z\left(1+sC_0R_0\right)}{g_mR_Z + 2\left(1+sR_ZC_Z\right)\left(1+sC_0R_0\right)} \tag{7}$$

The equivalent circuit configuration developed from (7) has been illustrated in Fig. 6, where

$$L_{eq} = \frac{2R_0C_0}{g_m} \tag{8}$$

$$R_{eq} = \frac{2}{g_m} \tag{9}$$

Similarly the input impedance of presented parallel R-L simulation circuit given in Fig. 5 under the influence of VD-DIBA port parasitics can be found as;

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{R_0\left(1+sR_ZC_0+sR_ZC_Z\right)}{1+g_mR_ZR_0+sR_Z\left(C_0+C_Z\right)} \tag{10}$$

The circuit realized from (10) is given in Fig.7, where

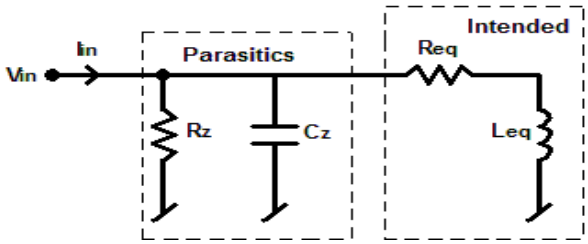

Fig. 6 Proposed Grounded series RL with VDDIBA port parasitic.

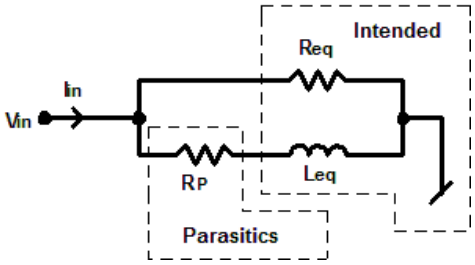

Fig. 7 Equivalent circuit of proposed Grounded Parallel R-L considering parasitics.

$$R_{eq} = R_0 \tag{11}$$

$$R_{eq} = \frac{2\left(C_1 + C_z\right)R_1}{g_m} \tag{12}$$

$$R_P = \frac{2R_1}{R_z g_m} \tag{13}$$

So, from Figs. 6 and 7 we can conclude that the influence of VD-DIBA port parasitics on proposed series/parallel R-L simulators is not very adverse.

6 Effect of Frequency Dependent Transconductance

The transconductance gain of a VDDIBA is frequency dependent. So, bandwidth limitation of VDDIBA transconductance gain may affect the behavior of proposed circuit at high frequencies. The frequency sensitive transconductance of VDDIBA can be defined by single pole frequency representation as;

$$g_m = \frac{g_{m0}}{1 + s\tau} \tag{14}$$

Here $\tau = 1/\omega_0$, where ω_0 is pole frequency and g_{m0} is zero frequency transconductance gain.
The input impedance of proposed series R-L circuit simulator considering frequency dependent transconductance is evaluated as;

$$Z_{in} = \frac{2sR_0C_0\left(1+s\tau\right) + 2\left(1+s\tau\right)}{g_{m0}} \tag{15}$$

The impedance Z_{in} realized by (16) is a grounded network of series resistance R_{eq}, inductance L_{eq} and frequency dependent negative conductance (FDNC) M_{eq}, where

$$L_{eq} = \frac{2\left(R_0C_0 + \tau\right)}{g_{m0}} \tag{16}$$

$$R_{eq} = \frac{2}{g_{m0}} \tag{17}$$

$$M_{eq} = \frac{2\tau}{g_{m0}} \tag{18}$$

So, considering the frequency dependent transconductance, the proposed series R-L configuration behaves like a series R_{eq}–L_{eq}–M_{eq} circuit where M_{eq} is the lossy term.

Similarly, the input impedance of proposed parallel R-L circuit simulator considering frequency dependent transconductance is evaluated as;

$$Z_{in} = \frac{2sR_0C_0\left(1+s\tau\right)}{2sR_0C_0\left(1+s\tau\right) + g_{m0}} \tag{19}$$

The impedance Z_{in} realized by (20) is a passive element network consisting two grounded parallel branches. The first branch consists of a series inductance L_{eq} along with a frequency dependent negative conductance (FDNC) M_{eq}. On the other hand the second branch has a resistance R_{eq},where

$$L_{eq} = \frac{2R_0C_0}{g_{m0}} \tag{20}$$

$$M_{eq} = \frac{2R_0C_0\tau}{g_{m0}} \tag{21}$$

$$R_{eq} = R_0 \tag{22}$$

So from (21)-(23) it is clear that, considering frequency dependent transconductance, the proposed parallel R-L circuit behaves like a parallel (R_{eq})-(L_{eq} series M_{eq}) circuit where M_{eq} is the lossy term.

7 Application Examples

The performances of the presented parallel/series R-L simulation circuits are demonstrated by some typical circuit applications. By using proposed series R-L simulation circuit a second order current mode low-pass filtering (LPF) circuit is developed which is shown in Fig. 8.

For demonstrating the working of proposed parallel R-L simulation configuration given in Fig. 5, a voltage-mode high-pass filter (HPF) is constructed and demonstrated in Fig. 9.

8 Simulation Results

To validate the mathematical analysis, Simulations were performed under PSPICE environment employing

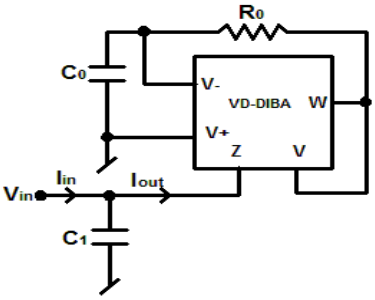

Fig. 8 Current mode LPF developed employing proposed series R-L simulator.

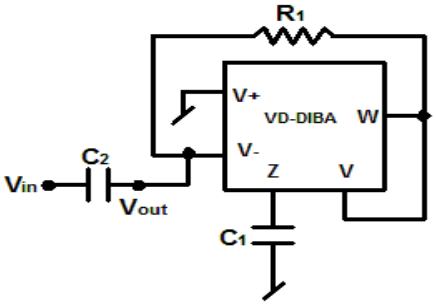

Fig. 9 Voltage mode HPF developed employing proposed parallel R-L simulator.

Table 5 Specification of VDDIBA.

Specification	Value
Input voltage linear range	-120 to 120 [mV]
3 dB bandwidth	121 [MHz]
Power consumption	62.5 [mW]
Transconductance gain	258.091 [µA/V]

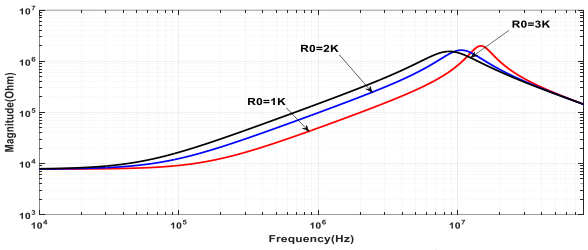

Fig. 10 Frequency responses of impedance of proposed series R-L simulator.

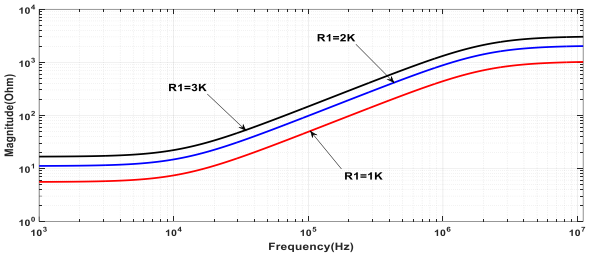

Fig. 11 Frequency responses of impedance of presented parallel R-L simulation circuit.

CMOS VDDIBA which includes CMOS OTA and CFOA SPICE micro-model of AD844. The DC supply voltages were chosen as ±0.9 VDC with all the biasing current of VDDIBA equals to 32 µA. The main specifications of this VDDIBA are given in Table 5.

Series R-L simulator of Fig. 2 is simulated with R_0 = 1, 2 and 3kΩ and C_0 = 1nF. The magnitude responses of the input impedance of configuration described in Fig. 4 have been illustrated in Fig. 10. From input impedance expression of Fig. 4 given in Table 3, it is observed that at low frequencies the inductive part of realized impedance L_{eq} is very small in comparison to the lossy term R_{eq}. Therefore, the magnitude responses are almost constant for low frequencies and representing the R_{eq}. As the frequency increases, the value of L_{eq} start increasing in comparison to constant lossy part R_{eq} and the circuit start behaving like a series lossy inductor. At very high frequencies, the value of L_{eq} becomes very high in comparison to R_{eq} and the configuration acts as a pure lossless inductor. This effect can be illustrated by plots shown in Fig. 8 The initial "horizontal part" of frequency response is due to the dominance of lossy term R_{eq}. Similarly the PSPICE simulated responses of impedance of parallel R-L network described in Fig. 5 have been illustrated in Fig. 10, for component values R_0 = 1, 2 and 3 kΩ, and C_0 = 0.01 nF.

From input impedance expression of Fig. 4 given in Table 3, it can be seen that for the high value of C_0, the value of L_{eq} is high in comparison to lossy part R_{eq} and behavior of this series lossy inductor become inclined more towards a lossless inductor. For further high values of C_0, the value of R_{eq} will be very small in comparison to L_{eq} and the configuration will work as a pure lossless inductor. This effect can be illustrated by response plots shown in Fig. 12. The initial "horizontal part" of frequency response is due to the existence of the lossy term R_{eq}. As the value of C_0 increases, the value of L_{eq} becomes high and flat part of response become comparatively narrower than inclined part. Which clearly indicate that on increasing C_0 the behavior of the proposed circuit starts inclining towards the behavior of a lossless inductor. Similarly the magnitude plots of impedance of parallel R-L network given in Fig. 5 on varying capacitance C_1 have been given in Fig. 13.

To demonstrate the electronic controllability of developed series R-L simulator shown in Fig. 4, simulations were performed with different bias current values. With component values R_0 = 1 kΩ and C_0 = 1 nF, bias currents were selected as I_b = 32, 48, and 64 µA. The simulation plots are shown in Fig. 14 which clearly illustrates that on increasing the bias currents, g_m is increasing and the input impedance is decreasing.

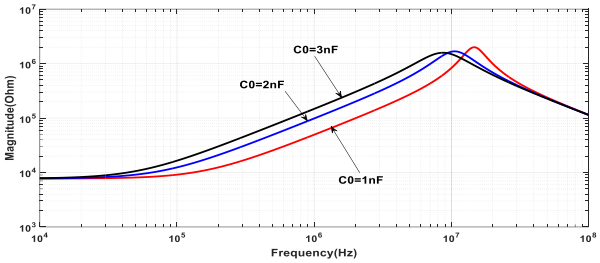

Fig. 12 Frequency responses of impedance of series R-L simulator with different values of C_0.

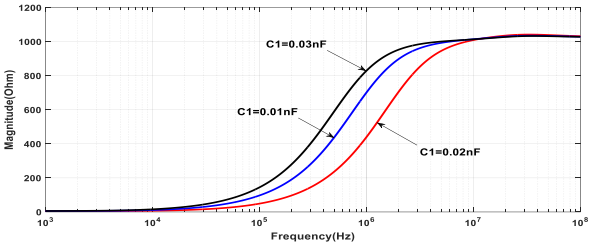

Fig. 13 Frequency responses of impedance of parallel R-L simulator with diverse values of C_1.

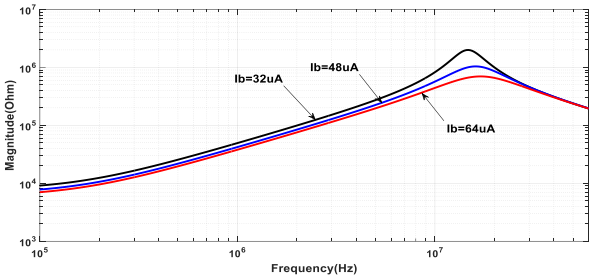

Fig. 14 Frequency responses of impedance of series R-L simulator for different values of biasing currents.

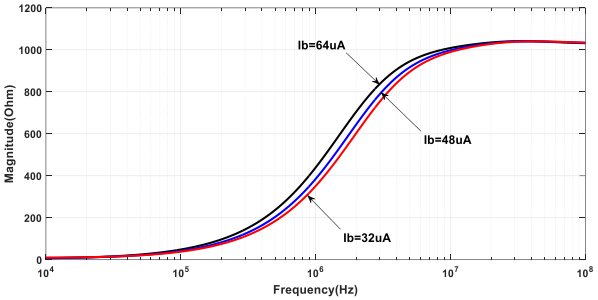

Fig. 15 Frequency responses of parallel R-L simulation circuit for different values of biasing currents.

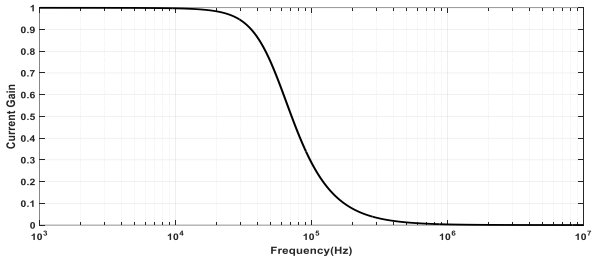

Fig. 16 The frequency response from current-mode low-pass filtering circuit given in Fig. 8.

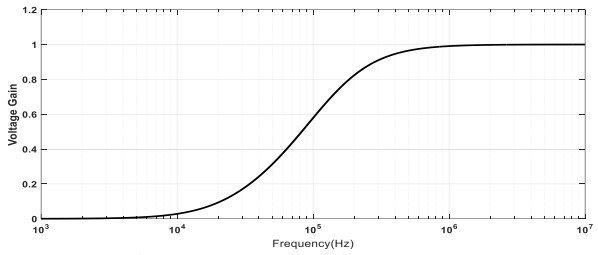

Fig. 17 The frequency response of voltage-mode high-pass filtering circuit given in Fig. 9.

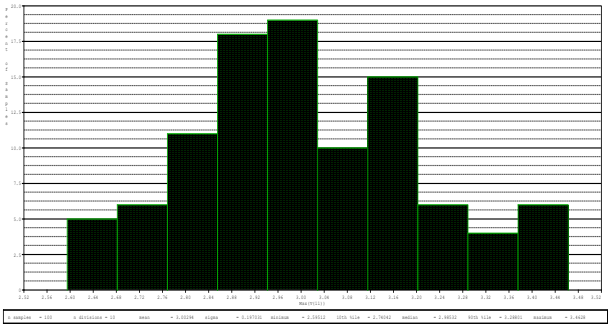

Fig. 18 Monte-Carlo simulation results of circuit shown in Fig. 8.

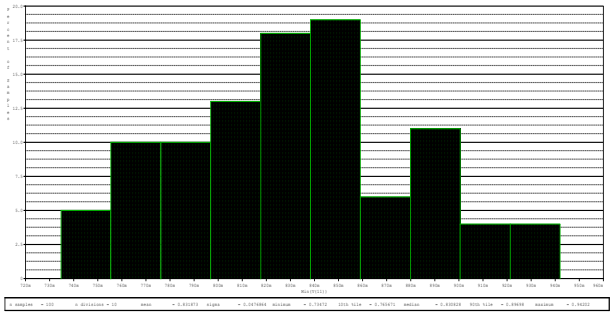

Fig. 19 Monte-Carlo simulation results of circuit shown in Fig. 9.

Electronic tunability of parallel R-L simulator shown in Fig. 5 has been demonstrated in plots shown in Fig. 15 with component values R_1 = 1 kΩ and C_1 = 0.01 nF. The current mode LPF design example shown in Fig. 8 is simulated with passive component values selected as C_0 = 0.01 nF, and C_1 = 0.02 nF. The simulated filter response is shown in Fig. 16. For simulation of HPF shown in Fig. 9, following component values are chosen: C_1 = 0.02 nF, and C_2 = 0.01 nF. The frequency response of this HPF is given in Fig. 17. To verify the robustness, the Monte-Carlo simulations of developed filtering circuits shown in Figs. 8 and 9 have been performed on taking 100 samples and 5% variation in passive element values. The Monte-Carlo simulations results are demonstrated in Figs. 18 and 19 respectively.

9 Conclusion

This paper proposes a new grounded series/parallel

R-L Network simulators using VDDIBA. In literature, several grounded series/parallel R-L network simulation circuits employing various active elements have been reported. These reported circuits suffer from one or more of following disadvantages; Use of more than one active element [11, 19, 30], employment of more than one resistance [10-11, 13-32], requirement of floating capacitance [9-11, 15-16, 18-21, 23-26, 28-30, 32], un-availability of electronic tuning facility of both inductive as well as resistive part [9-32], lake of independent control of realized inductance[11, 18, 20, 25, 26, 30] and need of matched elements [9, 20-24, 26, 31, 32]. The series R-L and parallel R-L simulation circuits presented in this paper are very compact with minimum requirement of passive and active components (one VDDIBA, single capacitance and single resistance) and enjoy several advantageous characteristics like use of grounded capacitor, facility of electronic tuning, non-interactive tuning of equivalent inductance and no need of any element value matching. Under non-ideal conditions, the behavior of presented circuits was found un-deviated from their ideal behavior. The influence of port parasitics of VDDIBA and effect of frequency dependent transconductance was also studied. To check the workability of presented circuits, some application examples are given. PSPICE simulations with 0.18 µm TSMC CMOS model were included to confirm the theoretical results

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