

A New Topology for Dynamic Voltage Restorer Using High Frequency Link

B. Tousi*, M. Farhadi-Kangarlu^{*(C.A.)} and M. Farzinnia*

Abstract: In this paper a new topology for Dynamic Voltage Restorer (DVR) with high frequency link is proposed. This topology is able to compensate different types of voltage disturbances such as voltage sag, voltage swell and voltage harmonics. According to the obtained equations, this topology operates as a controllable current source to charge the series capacitor. Due to using High Frequency Transformer (HFT), the volume and the weight of the proposed DVR is decreased in comparison with conventional DVRs. This topology contains two ac/ac converters which are using in the input and output of the device. The absence of DC link capacitors and storage elements is the other advantage of using the proposed structure. In order to verify the claimed features, the proposed topology has been simulated by PSCAD/EMTDC software and examined under several disturbance conditions. In addition, an experimental prototype has been designed and tested. The results of the simulation and experimental cases are presented.

Keywords: Dynamic Voltage Restorer, High-Frequency Link, Power Quality.

List of Symbols

v_l	Load voltage.
v_g	Grid voltage.
v_c	DVR output voltage.
X_{link}	Link reactance.
i_l	Load current.
i_{inj}	DVR output current (injected current).
\overline{P}_{link}	Active power flow through the link.
\overline{P}_{inj}	DVR output power.
V_i	Voltage phasor of the link input.
V_o	Voltage phasor of the link output.
δ	Leading angle of V_i with respect to V_o .
η_0	Efficiency of the HFT and the output converter.
n	Turns ratio of the HFT.

T_s	Switching period.
$v_{g,max}$	Instantaneous maximum value of the three-phase grid voltage.
$v_{g,min}$	Instantaneous minimum value of the three-phase grid voltage.

1 Introduction

NOWADAYS with proliferation of electronic applications, the Power Quality (PQ) has become an important issue in electrical engineering studies [1]. Voltage disturbances are the most frequent events which threaten the PQ in industrial distribution systems [1, 2]. Voltage sag, swell and flicker are some of common disturbances, which may be caused by over loads, short-circuit faults or start-up of the heavy loads. These disturbances can cause substantial economic and data losses due to malfunction of sensitive loads used in industries, hospitals and offices [1–3].

Dynamic Voltage Restorer (DVR) is a series connected custom power device which protects the sensitive loads against the voltage disturbances [3, 4]. DVR operates as a series controllable voltage source and generates the compensation voltage with the required amplitude, phase and frequency to compensate the disturbances [3–5].

Several literatures presented different topologies and

Iranian Journal of Electrical and Electronic Engineering, 2019.

Paper first received 25 July 2018 and accepted 07 March 2019.

* The authors are with the Department of Electrical Power Engineering, Faculty of Electrical and Computer Engineering, Urmia University, Urmia, Iran.

E-mails: b.tousi@urmia.ac.ir, m.farhadi@urmia.ac.ir and mr.farzinnia@gmail.com.

Corresponding Author: M. Farhadi-Kangarlu.

control methods for DVR since now. In general, the presented topologies are categorized into two groups. The first group includes the topologies which supplied by the Energy Storage (ES) elements such as batteries, flywheel, large capacitors, etc. [6–8]. Due to the limited energy storage, the first group of topologies is incapable to compensate severe voltage disturbances for long time intervals [3–5]. Also the used storage elements result in increasing the volume, weight and price of the DVR. Since the reliability of ES is very low, the reliability the DVR is decreased by using the ES. In the other words, the elimination of ES from the topology increases the reliability of the DVR. In order to improve the disadvantages of the first group, the second type of DVR has been presented. In the second group, DVR is directly connected to the grid and the required energy is directly provided from the grid. Therefore, there is no need for ES in the second category. The presented topology in [9] uses direct three-phase to three-phase converter to compensate the balanced and unbalanced disturbances. The proposed topology in [10], energizes the compensator of each phase from the two other phases. In order to protect the sensitive loads against the rapid voltage disturbances, the three-phase hybrid-transformer is used in [11]. Reference [12] presents another voltage compensator based on matrix converter without ES elements. This category of DVRs is able to compensate the voltage for long-time intervals but, the compensation capability is directly dependent on the amplitude of grid voltage. For this reason, the second group is unable to compensate severe voltage sags. However, the lack of ES in the second type of DVR causes the decreasing of the weight but the weight of the injection transformer is noteworthy amount. For this reason, several types of DVR with high frequency transformer are presented. In [13], a new DVR topology with a high frequency link transformer is presented. Another topologies using High Frequency Link (HFL) and buck converter are presented in [14–16]. The presented topology of DVR in [17] compensates the voltage sag using a high frequency link with an ES element.

Clearly, the presented DVRs studies in the literature are not limited to those mentioned above. Other studies have been also done on the DVRs considering both topologies [18] and control methods [19–20]. A comprehensive review of the DVR systems is presented in [21].

In this paper a new topology for three-phase DVR is proposed. This topology is able to compensate different types of voltage disturbances. The proposed topology is directly connected to the grid. Moreover, a HFL is used to control the amount of the transferred power and compensation. The HFL is responsible to control the power flow in addition of voltage isolation. The volume and the weight of the structure are reduced due to use of HFT. In the next section, the electrical topology of the proposed DVR along with the fundamentals of the

operation is discussed. Then, the proposed method to control the switching and detecting the voltage disturbances is expressed. The simulation and experimental results verify the proper performance of the proposed topology under different disturbance conditions.

2 High Frequency Transformer-Based AC-AC DVR

The issue which has not been investigated widely in the DVR topologies is the injection transformers. In DVRs, the transformers are usually employed to isolate the compensation voltage from the grid voltage in addition of increasing the amplitude of injected voltage. Using the transformer causes to increase the weight and volume of the DVR topology. In order to overcome this issue, applying the HFL in DVR can be an effective alternative. Fig. 1 shows the block diagram of the conventional ac/ac conversion using HFL in different systems. In this method, the input AC voltage is rectified and converted to High Frequency (HF) AC voltage. Afterward the converted voltage is transferred by HFT to the secondary side. The DC-link capacitors are employed to provide the smooth DC voltage for both of inverters placed in primary and secondary sides. Evidently, the required size of the transformer core is inversely proportional to the square of the frequency. Therefore, the mass of the structure is reduced in comparison with the converters using low-frequency transformers.

Fig. 2 shows the proposed topology for DVR with HFL. Although the proposed topology is a three-phase DVR, herein after only one phase (first phase) is studied to avoid repetition. As depicted in the figure, the proposed topology contains two ac/ac converters in each phase which are connected through the HFL. The input converter consists of three bidirectional switches which are marked with $S_{i,1}$, $S_{i,2}$ and $S_{i,3}$. This converter is used to convert the grid voltage into the input voltage of the HFL which is indicated by $v_i(t)$. Indeed, this converter produces the HF AC voltage using the input low-frequency AC voltages. As shown in the figure the generated HF voltage by the second converter is marked with $v_o(t)$. At the output side, a capacitor is inserted to carry the injected voltage for compensating the disturbance. Same as the input section, the output ac/ac converter is used as a link between high frequency part and low-frequency parts. The output converter is formed by two bidirectional switches which are indicated by $S_{o,1}$ and $S_{o,2}$. Also, when no voltage disturbance is detected, the DVR should be in bypass mode; in order to bypass the DVR, the bypass switch S_b is used which is a bidirectional power-electronic switch. As expressed in previous section, the proposed topology is not the first structure based on HFT but, the main feature of this topology in comparison of presented ones is the elimination of rectifiers and DC link capacitors. This

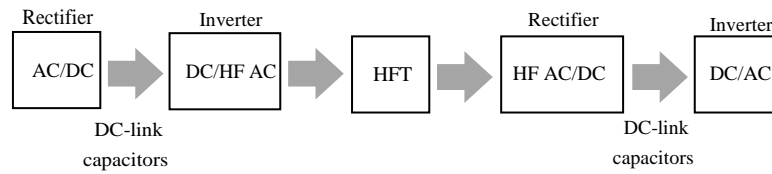


Fig. 1 Dem The operational structure of the HF link.

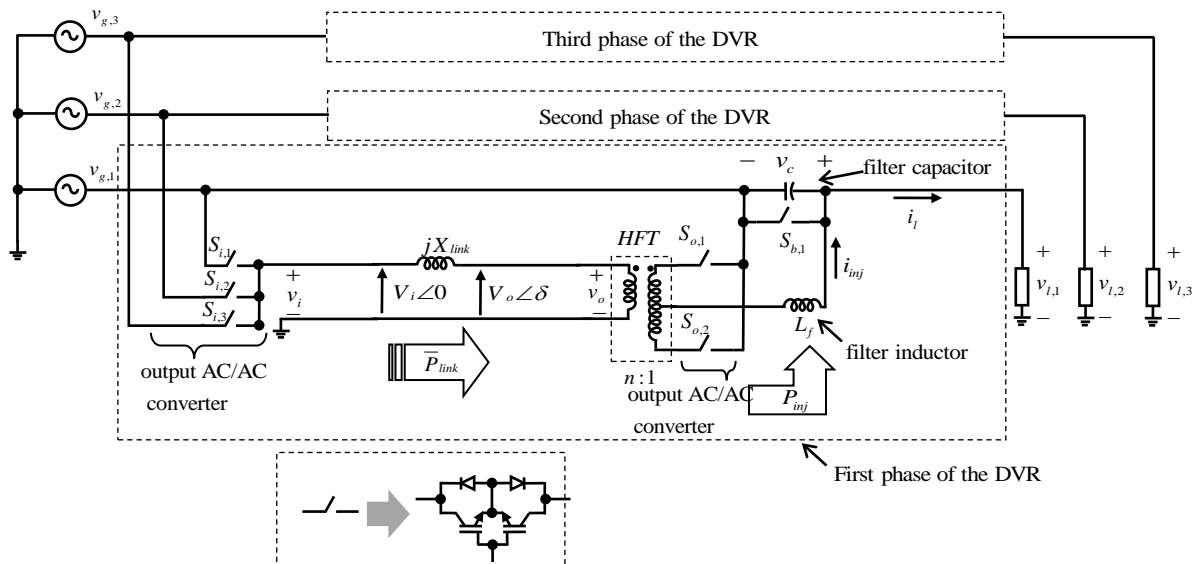


Fig. 2 The proposed HFT based ac-ac DVR topology.

will cause the reduction in weight, volume and evaluated cost.

The detailed control methods of the input and output ac/ac converters are discussed in the next subsection. The link reactance (X_{link}) is used to avoid short-circuit and limit the power flow to nominal amount for protecting the power switches. The HFT is used to isolate the injection voltage from the grid voltage in addition of increasing the compensation capability. Applying the HFT in the proposed topology causes reduction in volume and weight of the structure in comparison with the conventional topologies of DVR. Since, the HFT is used and the switching frequency is rather high, the topology would be more suitable for low-voltage (LV) cost-effective applications such as household applications.

The operation of the DVR is like a variable voltage source (v_c) which is placed in series with the grid line and the load voltage is sum of the grid and DVR voltage:

$$v_l(t) = v_g(t) + v_c(t) \tag{1}$$

When the grid voltage is under disturbance condition, DVR starts to generate the proper amount of voltage to protect the sensitive load. For instance, when the amount of voltage sag is equal to 20% ($v_g=0.8$ pu) the generated voltage by DVR should be equal to 0.2pu in phase with the grid voltage. On the other hand when the voltage is distended, the DVR is responsible to

compensate voltage by generating the voltage with the phase difference of 180 degrees from the phase voltage.

According to the proposed topology, the voltage of the output capacitor is affected by two parameters; the load current (i_l) and the injected current to the capacitor (i_{inj}).

$$v_c(t) = v_c(t^-) + \frac{1}{C} \int_{t^-}^t [i_{inj}(t) - i_l(t)] dt \tag{2}$$

The load current is an independent parameter varies with the amount of the connected load and its waveform can be non-sinusoidal for nonlinear types of the loads. Consequently, i_{inj} is the available parameter to control the compensation voltage in each condition. On the other hand, amount of injected current has influenced by the average of transferred power through the HFT and the required compensation voltage generates by controlling the power flow. By considering the high difference between the frequencies of the HF link and the grid, the variation of low-frequency voltages can be neglected during the given switching period while the link parameters are considered under steady condition. Therefore, the average amount of power flow through the link is calculated as follows:

$$\begin{aligned} \bar{P}_{link}(t) &= \text{Re} \left[\left(V_i(t) \angle 0 \right) \frac{V_i(t) \angle 0 - V_o(t) \angle \delta(t)}{jX_{link}} \right] \\ &= -\frac{V_i(t)V_o(t)}{X_{link}} \sin \delta(t), \quad -\frac{\pi}{2} \leq \delta(t) \leq \frac{\pi}{2} \end{aligned} \tag{3}$$

In the above equality, the amounts of the $V_i(t)$ and $V_o(t)$ are the amplitude of the input and output voltages of the HFL, respectively. It should be noted that the variation of the amplitudes and the phase angle in (3) is very smooth and can be neglected for several dozen consecutive period. The $\delta(t)$ phase angle is the accessible variable to control the amount of power flow. It means that, when $\delta(t)$ has a negative amount, the power is transferred to the output side and the voltage of capacitor starts to increase. Otherwise, when $\delta(t)$ is greater than zero the power is transferred from the capacitor to the grid and consequently the capacitor voltage will be decreased.

By considering η_o as the efficiency of the HFT and output converter, the injected power to output capacitor is obtained as follows:

$$P_{inj}(t) = \eta_o \bar{P}_{link}(t) = \frac{\eta_o V_o(t) V_i(t)}{X_{link}} \sin \delta(t) \quad (4)$$

The following equality can be considered between instantaneous amount of capacitor voltage and $V_o(t)$:

$$V_o(t) = n \left(1 - \frac{THD_o \%}{100} \right) v_c(t) \quad (5)$$

where, n denotes the turn ratio of HFT.

Same as (5), the following equality is expressed for the voltage of the input side:

$$V_i(t) = \frac{1}{2} \left(1 - \frac{THD_i \%}{100} \right) \left[|v_{g,max}(t)| + |v_{g,min}(t)| \right] \quad (6)$$

where, $v_{g,max}(t)$ and $v_{g,min}(t)$ are the instantaneous maximum and minimum amounts of grid voltages.

Considering Eqs. (4)-(6), the injected current to capacitor is obtained as follows:

$$i_{inj}(t) = \frac{P_{inj}(t)}{v_c(t)} = \frac{\eta_o n \sin \delta \left(1 - \frac{THD_i \%}{100} \right) \left(1 - \frac{THD_o \%}{100} \right) \left[|v_{g,max}(t)| + |v_{g,min}(t)| \right]}{2X_{link}} \quad (7)$$

According to the above equation, the injected current is a function of the grid voltages. Therefore, the proposed topology can be modelled as a variable current source in parallel with output capacitor. In this case the single capacitor can be used as the output filter instead of LC type. For this reason, the required output filter of the proposed topology is smaller in comparison with the used filter of the conventional DVRs.

3 Control Method

3.1 Switching Method

In this subsection, the control process of switches is

explained. The proposed method for both of input and output converter is based on Pulse Width Modulation (PWM). At first, the switching method of input converter is expressed. As mentioned in the previous section the input converter is responsible for converting the grid voltage into high frequency voltage. Fig. 3 shows the voltage waveforms of the input converter. According to the figure, the input voltage of the high frequency link (v_i) is the result of the proper switching between minimum and maximum amounts of input voltages. The switching period (T_s) is decomposed into two sections which are indicated by positive (t_p) and negative (t_n) intervals. In the positive interval the controller commands the converter to conduct the maximum input voltage to the link. In the same way, the converter conducts the minimum amount of input voltage to high frequency link. In order to eliminate the low-order components of input voltage the following equation should be satisfied.

$$t_p^j v_{g,max}^j + t_n^j v_{g,min}^j = 0 \quad (8)$$

where, $v_{g,max}^j$ and $v_{g,min}^j$ denotes the maximum and minimum amount of input voltage in j^{th} switching period. As mentioned the switching period is sum of the positive and negative time intervals. Therefore, the following equations are obtained:

$$t_p^j = \frac{v_{g,min}^j}{v_{g,max}^j - v_{g,min}^j} T_s \quad (9)$$

$$t_n^j = \frac{v_{g,max}^j}{v_{g,max}^j - v_{g,min}^j} T_s$$

Fig. 4 shows the voltage waveforms of the output converter. This converter is responsible to convert the output voltage of the high frequency link (v_o) into the low-frequency voltage of capacitor voltage. As shown in the figure, when the switching command is high the positive amount of v_c should be conducted to the link. Otherwise, the converter connects the negative voltage of capacitor to the link. In order to control the power flow through the link, the phase difference between the command signal of input and output.

3.2 Reference Signal Generation

Fig. 5 shows the block diagram of the proposed control method. As the first step, the grid voltage is passed through low-pass filter to cancel the high order harmonics of the grid voltage. The Phase Locked Loop (PLL) generates a sinusoidal waveform in phase with the grid voltage. Then, by using the obtained phase and the reference amplitude ($V_{g,ref}$) the reference signal of the grid voltage is obtained. In order to detect the disturbance, the absolute difference of the reference signal with the grid voltage is calculated and passed through PI controller. When the disturbance is occurred, the difference between the grid voltage and reference

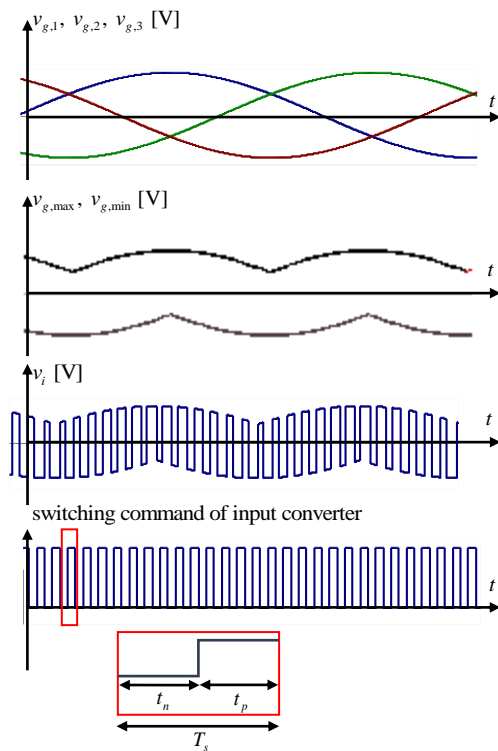


Fig. 3 The voltage waveforms of input converter.

signal is increased and the comparator will detect the disturbance. The difference of the reference signal and the grid voltage is equal the required compensation voltage or reference signal of compensation (v_c^{ref}). Afterward, the hysteresis method is used to control the phase difference between the high frequency link according to the subtraction of the measured and reference compensation voltages. Finally, the proper commands are sent to the gates based on the discussed method.

The main goal of this control part is generating the proper reference signals for the converters. In this method, the hysteresis band with the width β is defined around the reference signal of the compensation voltage. Fig. 6 shows the reference signal with the considered hysteresis bands. According to this method, when the measured voltage of capacitor ($v_{c,m}$) is smaller than the lower limit ($v_{c,ref}^L$) the amount of phase difference between the input and output voltages is set to the maximum amount ($\delta = 90$ degrees). Also, when the measured voltage is greater than the higher limit ($v_{c,ref}^H$) the phase difference is set the minimum amount ($\delta = -90$ degrees). Furthermore, when the measured voltage is located between the bands the phase difference is set to zero. Therefore, by controlling the power flow through the high frequency link, the capacitor voltage is changed in the hysteresis band.

4 Discussion on the Compensation Capacity

As expressed previously, the basic different of the

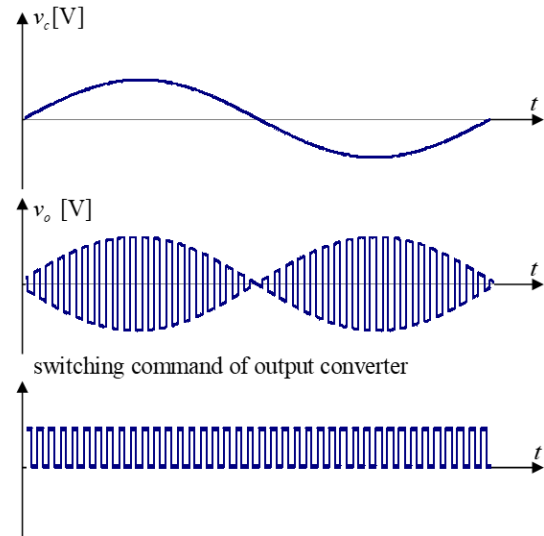


Fig. 4 The waveforms of output converter.

proposed topology with the conventional topologies is the compensation based on the current control. This means that the DVR compensate the disturbances by injecting the sufficient current to the series capacitor by measuring load voltage. Therefore, calculating the compensation capability will be different from the conventional voltage based DVRs. For this purpose, the grid voltage is considered under sag condition:

$$V_g = 1 - \frac{sag\%}{100} \text{ pu} \tag{10}$$

In the above equation, *sag%* refers to the percentage of voltage drop in the grid voltage. This means in the normal condition the *sag%* is equal to zero and when the *sag%* is equal to 100, it expresses the complete power outage in the system.

By considering the in-phase compensation method, the compensation voltage is obtained as follows:

$$V_c = V_{l,rated} - V_g = 1 - \left(1 - \frac{sag\%}{100}\right) = \frac{sag\%}{100} \text{ pu} \tag{11}$$

By considering the load current equal to 1 pu with zero phase difference from voltage, the required injected power will obtained as follows:

$$P_{inj} = V_c I_l \cos \varphi = \frac{Sag\%}{100} \text{ pu} \tag{12}$$

Considering Eqs. (7) and (13) the following result is concluded:

$$P_{inj} = \frac{\eta_o n \sin \delta \left(1 - \frac{THD_o\%}{100}\right) \left(1 - \frac{THD_o\%}{100}\right) V_c \min[|v_{g,max}(t)| + |v_{g,min}(t)|]}{2X_{link}} \tag{13}$$

$$\frac{Sag\%}{100} = \frac{\eta_o n \sin \delta \left(1 - \frac{THD_o\%}{100}\right) \left(1 - \frac{THD_o\%}{100}\right) \frac{Sag\%}{100} 1.5 \left(1 - \frac{sag\%}{100}\right)}{2X_{link}}$$

By simplifying the equation and considering the rectangular THD% equal to 55.1% the following result

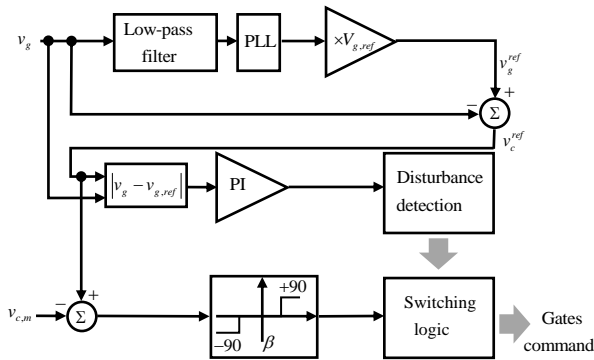


Fig. 5 The proposed control method.

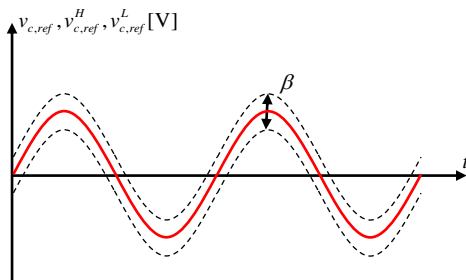


Fig. 6 The reference signal with the hysteresis band.

is concluded:

$$\text{Sag\%} = \left[1 - \frac{2X_{link}}{\eta_o \cdot n \cdot (0.3)} \right] \times 100 \quad (14)$$

The above equation, presents the maximum range of voltage sag that the proposed DVR is capable to compensate. According to the equation, the compensation capability is increased by decreasing the inductance of the HFL.

In the design consideration the amount of the X_{link} should satisfy the following inequality:

$$X_{link} < \frac{\eta_o \cdot n \times 0.3}{2} \quad (15)$$

In this study to achieve the proper compensation capability, the following equation is considered:

$$X_{link} = \frac{\eta_o \times 0.3}{4} \quad (16)$$

By considering the efficiency factor of output converter equal to 80%, the compensation capability of the proposed DVR is rewritten as follows:

$$\text{Sag\%} = \left[1 - \frac{1}{2 \cdot n} \right] \times 100 \quad (17)$$

For example, with a 1:1 transformer ($n = 1$) the voltage sags up to 0.5pu could be completely compensated according to the equation above. It worth to mention that, by decreasing the inductance of HFL the

compensation capability will increase at the same turn ratio of the transformer. This means, the proposed topology can achieve higher compensation capability in comparison with the conventional voltage-based DVRs with the constant transformer turn ratio.

5 Calculation of the Efficiency

In order to calculate the amounts of efficiency factors for the input and output converters, the losses have divide into the switching and conduction losses. The losses caused by the switching appear in start time of on and off states. As shown in Table 1, the waveforms of current and voltage of the switch have simplified as a ramp function. Therefore, the power losses of one switch during a cycle is obtained as follows:

$$P_{sw,loss} = f_s \left(\int_{t_{on}} v_{DS}(t) i_{DS}(t) dt + \int_{t_{off}} v_{DS}(t) i_{DS}(t) dt \right) = f_s \left(\frac{1}{6} V_{DS} I_{DS} t_{on} + \frac{1}{6} V_{DS} I_{DS} t_{off} \right) \quad (18)$$

In the above equation, V_{DS} and I_{DS} are the blocked voltage and conducted current through drain and source pins of the MOSFET. Since the used switches are in bidirectional configuration, the block voltage in the primary converter is divided between two MOSFETs.

$$\frac{V_g}{4} \leq V_{DS} \leq \frac{V_g}{2} \quad (19)$$

The block voltage in the output side is approximately equal to the compensation voltage.

$$0 \leq V_{DS} \leq V_c \quad (20)$$

In addition of the switching losses, the power losses due to the current conduction through the switches and

Table 1 Block voltage and conducted current of the MOSFET.

Switch State	
On	Off

diodes should be calculated. For this case, the electrical models of the MOSFET and diode during the current conduction are considered as follows:

$$\begin{aligned} v_{f,MOS} &= V_T + R_T I_{DS} \\ v_{f,D} &= V_D + R_D I_D \end{aligned} \quad (21)$$

During the on state of each switch, one of the MOSFETs with a diode is conducting the current. So, the power loss during the conduction is formulated as follows:

$$P_{loss,cond} = \left[(V_T + V_D) I_{DS} + (R_T + R_D) I_{DS}^2 \right] \times \left[1 - (t_{on} + t_{off}) f_s \right] \quad (22)$$

The conducted current by each MOSFETs in the input converter is obtained as follows:

$$\begin{aligned} I_{DS} &= \tilde{I}_{link} \\ &= \frac{0.5 \left(1 - \frac{THD_i\%}{100} \right) \left(|v_{g,max}(t)| + |v_{g,min}(t)| \right) - i \left(1 - \frac{THD_o\%}{100} \right) n v_c}{2 X_{link}} \\ &= \frac{\sqrt{\left[0.11 \left(|v_{g,max}(t)| + |v_{g,min}(t)| \right) \right]^2 + \left[(0.22) n v_c \right]^2}}{X_{link}} \end{aligned} \quad (23)$$

In the above equation, amount of the THD_i% and THD_o% considered equal to 55. Same as previous, the conducted current by the MOSFETs in the output converter is obtained as follows:

$$\begin{aligned} I_{DS} &= n \tilde{I}_{link} \\ &= n \frac{\sqrt{\left[0.11 \left(|v_{g,max}(t)| + |v_{g,min}(t)| \right) \right]^2 + \left[0.22 n v_c \right]^2}}{X_{link}} \end{aligned} \quad (24)$$

By using the Eqs. (19)-(23) and considering the losses of the transformer and inductor, the amounts of the efficiency in the 50% of sag disturbance is equal to 82.67% while the efficiency in 50% of swell disturbance is equal to 76.43%.

6 Simulation and Experimental Results

The simulation and experimental studies of the DVR structure and the control method proposed in the above sections, are presented in this section to assess the presented DVR system. In this examination, a transformer with three taps has been used to create the disturbance condition. The sag generator structure is shown in Fig. 7. The taps are connected through bidirectional power-electronic switches (common-emitter IGBTs) to the output (input of the DVR). As it is clear from Fig. 7, sag and swell conditions can be realized by turning ON the switch $S_{t,3}$ and $S_{t,1}$, respectively. Also, in normal condition (no sag is occurred) the switch $S_{t,2}$ is turned ON.

Table 2 indicates the details of the system parameters

used in the simulation and experiments. Fig. 8 shows the experimental prototype of the proposed topology. The 11N80 and 23N50L power MOSFETs are used in the input and output converters, respectively. In order to increase the amplitude of injected current, the turn ratio of the HFT (n) has been considered to be 1. Moreover, the injection capacitor and the inductor of the high frequency link have been set to be 20μF and 0.25ηH, respectively. As mentioned, the link inductor is used to protect the power switches by restricting the amplitude of the current. The LPC1768 processor has been employed to control the switching and generating the reference signals.

The simulation and experimental results for sag condition are presented in Fig. 9 and Fig. 10, respectively. The simulation of the proposed DVR has accomplished by PSCAD/EMTDC software. The grid voltage is shown in Fig. 10(a) and Fig. 9, is under the condition of 40% voltage sag during the 9 cycles. As shown in Fig. 10(b), the proposed DVR generated the

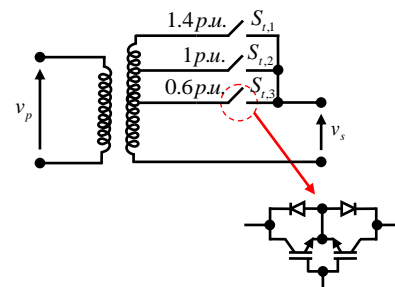


Fig. 7 Voltage sag/swell generator circuit for experimental studies

Table 2 System parameters.

Parameters	Values	
Grid	Amplitude [V]	210√2
	Frequency [Hz]	50
	Resistance [Ω]	50
Load	Inductance [mH]	60
	Frequency [Hz]	50
Filter	Capacitance [μF]	20
Switching frequency [kHz]		40

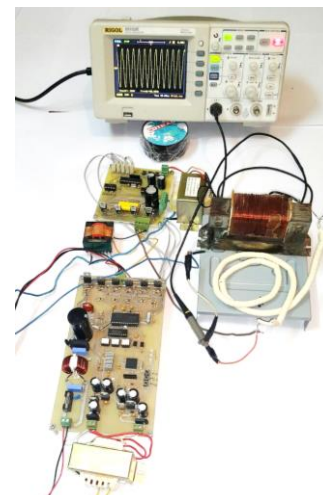


Fig. 8 The photo of experimental prototype.

required compensation voltage for compensating the voltage mitigation on the sensitive load side. The fully compensated load voltage is presented in Fig. 10(c). In addition, the voltage waveform of the secondary side of HFT is shown in Fig. 11. As obvious, the amplitude of the waveform is equal to the instantaneous amount of compensation voltage.

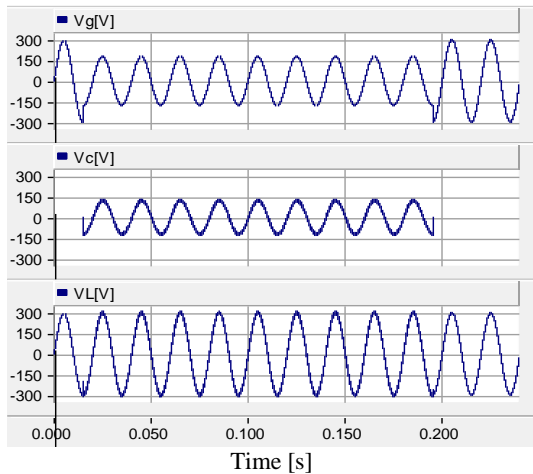


Fig. 9 The simulation results for 40% sag compensation.

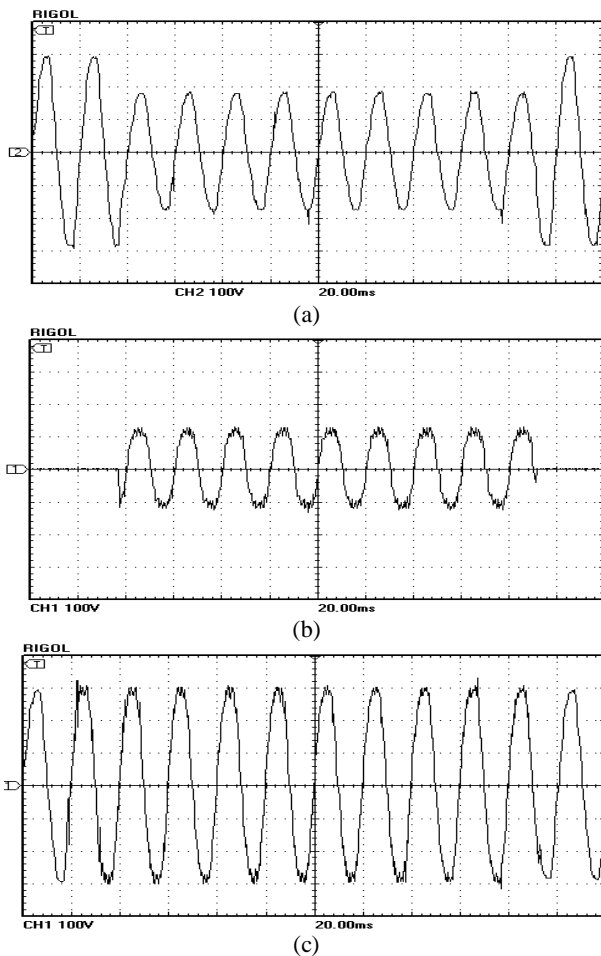


Fig. 10 Experimental results for sag compensation (vertical axis: 100V/div, horizontal axis: 20ms/div), a) grid voltage, b) injected voltage, and c) load voltage.

The simulation and experimental results for the voltage swell compensation are presented in Fig. 12 and Fig. 13. As shown in Fig. 13(a), 40% voltage swell is applied on the grid voltage for a considered time interval. In Fig. 13(b), the DVR output voltage is indicated. In the case of voltage swell, the output voltage of the DVR is opposite to the grid voltage to reduce it to the rated value. The compensated load voltage under swell disturbance is presented in Fig. 13(c). According to the simulation and experimental results, the proposed topology is properly capable to compensate the over voltages.

The simulation results for compensating the harmonic distortion are shown in Fig. 14. According to the figure, the grid voltage is in normal condition for 0.015s from the beginning then, the grid voltage encounters with a 40% sag and simultaneously fifth-order harmonic for 9 cycles. During the voltage disturbances, the proposed DVR detects the distortion and generates the proper voltage. As shown in the figure, the DVR generates the required compensation voltage so that the load voltage has a constant-magnitude sinusoidal waveform. Therefore, the proposed DVR is also able to compensate for different simultaneous events.

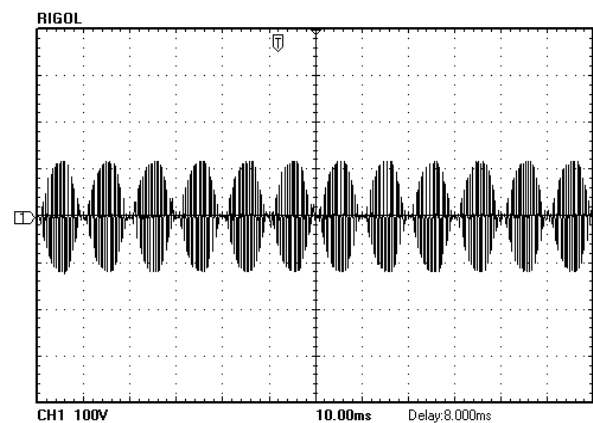


Fig. 11 The secondary voltage of HFT, v_o , (vertical axis: 100V/div, horizontal axis: 10ms/div).

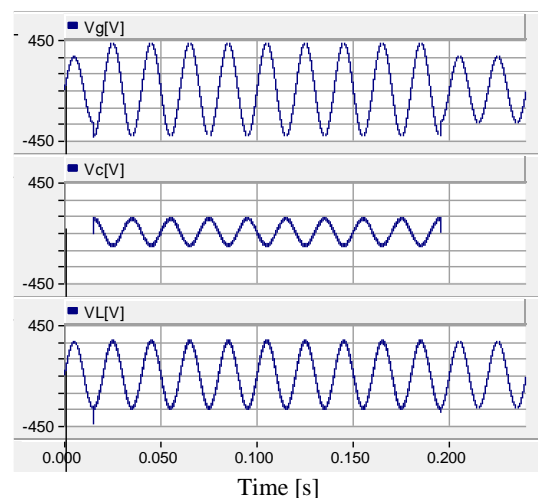


Fig. 12 The simulation results for 40% swell compensation.

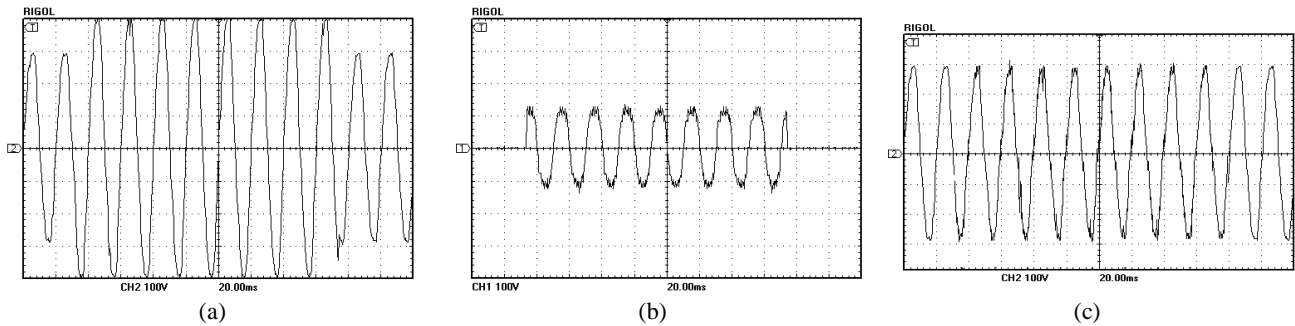


Fig. 13 Experimental results for swell compensation (vertical axis: 100V/div, horizontal axis: 20ms/div), a) grid voltage, b) injected voltage, and c) load voltage.

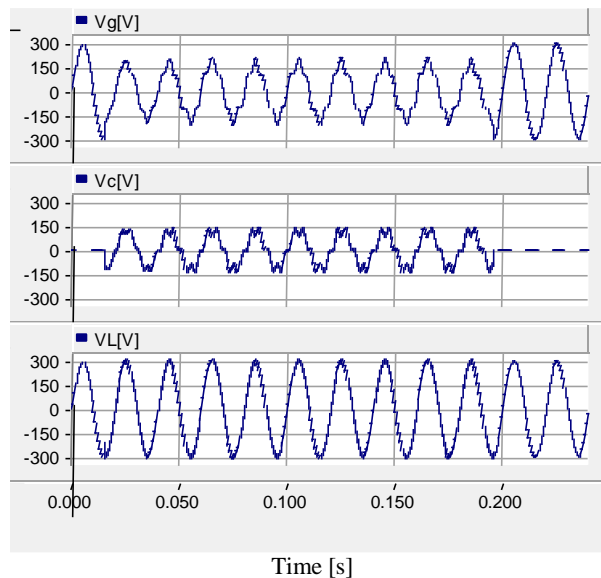


Fig. 14 The simulation results for compensating the harmonic distortion.

Table 3 Comparison of the proposed topology with other relevant topologies.

Reference	Type	Number of Switches	Transformer Type	Mass	Switches Voltage Stress
[23]	Single Phase to Single Phase	8	Low Frequency	High	Very Low
[24]	Single Phase to Single Phase	10	-	Low	Very High
[25]	Single Phase with ES	2	Low Frequency	High	Low
Proposed Topology	Three Phases to Single Phase	12	High Frequency	Low	Medium

7 Conclusion

Dynamic Voltage Restore (DVR) with high frequency link has been presented in this paper. The proposed structure is constructed by some bidirectional power-electronic switches, an inductor and a high-frequency isolation transformer. Due to high operation frequency of the injection transformer, the mass of the magnetic core has been reduced. As a result of using direct AC-AC converter, the energy storage element is not required in the proposed topology. Moreover, thanks to the high-frequency transformer, the volume and weight of the DVR is reduced. As the simulation results indicated, the proposed DVR system can cope with various types of voltage-related problems such as voltage sag, voltage swell and voltage harmonics. In Table 3, a comparison between the proposed DVR with the recent presented topologies is expressed. According the table, the compared topology is in single phase arrangement which need lower number of

switches due to lack of two other phases in the input side. On the other hand, the proposed topology is supplied by three phases and it causes the increasing of robustness in compensation under different types of disturbances. In the other word, if the mentioned topologies would be used in three phases to single phase mode, the number of switches will increase by three times. Lack of the transformer will result in incrementing of voltage stress in power switches [24]. As mentioned, using ESE in the topology will result in limitation of compensation energy and increasing the amounts of the weight and the volume.

References

- [1] S. M. Hietpas and M. Naden, "Automatic voltage regulator using an AC voltage-voltage converter," *IEEE Transactions on Industry Applications*, Vol. 36, No. 1, pp. 33–38, 2000.

- [2] H. M. Wijekoon, D. M. Vilathgamuwa, and S. S. Choi, "Interline dynamic voltage restorer: An economical way to improve interline power quality," *IEE Proceedings-Generation, Transmission and Distribution*, Vol. 150, No. 5, pp. 513–520, 2003.
- [3] E. Babaei, M. F. Kangarlu, and M. Sabahi, "Mitigation of voltage disturbances using dynamic voltage restorer based on direct converters," *IEEE Transactions on Power Delivery*, Vol. 25, No. 4, pp. 2676–2683, 2010.
- [4] E. Babaei, M. F. Kangarlu, and M. Sabahi, "Compensation of voltage disturbances in distribution systems using single-phase dynamic voltage restorer," *Electric Power Systems Research*, Vol. 80, No. 12, pp. 1413–1420, 2010.
- [5] E. Babaei and M. F. Kangarlu, "Operation and control of dynamic voltage restorer using single-phase direct converter," *Energy Conversion and Management*, Vol. 52, No. 8–9, pp. 2965–2972, 2011.
- [6] P. Jayaprakash, B. Singh, D. P. Kothari, A. Chandra, and K. Al-Haddad, "Control of reduced-rating dynamic voltage restorer with a battery energy storage system," *IEEE Transactions on Industry Applications*, Vol. 50, No. 2, pp. 1295–1303, 2014.
- [7] I. Chung, D. Won, S. Park, S. Moon, and J. Park, "The DC link energy control method in dynamic voltage restorer system," *Electric Power Systems Research*, Vol. 25, pp. 525–531, 2003.
- [8] H. K. Al-Hadidi, A. M. Gole, and D. A. Jacobson, "Minimum power operation of cascade inverter-based dynamic voltage restorer," *IEEE Transactions on Power Delivery*, Vol. 23, No. 2, pp. 889–898, 2008.
- [9] E. Babaei and M. Farhadi Kangarlu, "Voltage quality improvement by a dynamic voltage restorer based on a direct three-phase converter with fictitious DC link," *IET Generation, Transmission & Distribution*, Vol. 5, No. 8, pp. 814–823, 2011.
- [10] E. Babaei and M. Farhadi Kangarlu, "Cross-phase voltage sag compensator for three-phase distribution systems," *International Journal of Electrical Power & Energy Systems*, Vol. 51, pp. 119–126, 2013.
- [11] J. Kaniewski, Z. Fedyczak, and G. Benysek, "AC voltage sag/swell compensator based on three-phase hybrid transformer with buck-boost matrix-reactance chopper," *IEEE Transactions on Industrial Electronics*, Vol. 61, No. 8, pp. 3835–3846, 2013.
- [12] J. M. Lozano-Garcia and J. M. Ramirez, "Voltage compensator based on a direct matrix converter without energy storage," *IET Power Electronics*, Vol. 8, No. 3, pp. 321–332, 2015.
- [13] H. Sree and N. Mohan, "High-frequency-link cycloconverter-based DVR for voltage sag mitigation," in *Conference Record of the 2000 Twenty-fourth International Power Modulator Symposium*, pp. 97–100, 2000.
- [14] H. F. Ahmed, H. Cha, and A. A. Khan, "Design of dynamic voltage restorer for voltage sag and swell compensation using high-frequency-isolated direct AC-AC converter without commutation problem," in *IEEE 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, pp. 1–10, 2015.
- [15] H. F. Ahmed, H. Cha, and H. Kim, "A single-phase high-frequency transformer isolated buck converter with both in-phase and out-of-phase operations," in *IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Hefei, pp. 2204–2208, 2016.
- [16] H. F. Ahmed, H. Cha, A. A. Khan, and H. Kim, "A highly reliable single-phase high-frequency isolated double step-down AC-AC converter with both non-inverting and inverting operations," *IEEE Transactions on Industry Applications*, Vol. 52, No. 6, pp. 4878–4887, 2016.
- [17] A. Y. Goharrizi, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Three-phase HFL-DVR with independently controlled phases," *IEEE Transactions on Power Electronics*, Vol. 27, No. 4, pp. 1706–1718, 2012.
- [18] R. J. Satputaley and V. B. Borghate, "Performance analysis of DVR using "new reduced component" multilevel inverter," *International Transactions on Electrical Energy Systems*, Vol. 27, No. 4, p. e2288, 2017.
- [19] M. A. Norouzi, J. Olamaei, and G. B. Gharehpetian, "Compensation of voltage sag and flicker during thermal power plant turbo-expander operation by dynamic voltage restorer," *International Transactions on Electrical Energy Systems*, Vol. 26, No. 1, pp. 16–31, 2016.
- [20] S. Taghizadeh, N. Mei Lin Tan, and M. Karimi-Ghartemani, "Study of fuzzy based control algorithm for dynamic voltage restorer," *International Transactions on Electrical Energy Systems*, Vol. 25, No. 12, pp. 3600–3617, 2015.
- [21] M. Farhadi-Kangarlu, E. Babaei, and F. Blaabjerg, "A comprehensive review of dynamic voltage restorers," *International Journal of Electrical Power & Energy Systems*, Vol. 92, pp. 136–155, 2017.
- [22] M. Moradlou and H. R. Karshenas, "Compensation range calculation in an interline dynamic voltage restorer (IDVR) encountering different voltage sag types," *International Transactions on Electrical Energy Systems*, Vol. 24, No. 7, pp. 992–1005, 2014.

- [23] M. C. Jiang and T. C. Liu, "A soft-switching single-phase two-arm dynamic voltage restorer," in *IEEE 18th International Power Electronics and Motion Control Conference (PEMC)*, pp. 319-323, 2018.
- [24] D. Nazarpour, M. Farzinnia, and H. Nouhi, "Transformer-less dynamic voltage restorer based on buck-boost converter," *IET Power Electronics*, Vol. 10, No. 13, pp. 1767-1777, 2017.
- [25] J. Ye, H. B. Gooi, B. Wang, Y. Li, and Y. Liu, "Elliptical restoration based single-phase dynamic voltage restorer for source power factor correction," *Electric Power Systems Research*, Vol. 166, pp. 199-209, 2019.



B. Tousi received the B.Sc. degree in Electronic Engineering from University of Tabriz, Tabriz, Iran. He received the M.Sc. and Ph.D. degrees both in Electric Power Engineering from Amirkabir University of Technology, Tehran, Iran, in 1995 and 2001, respectively. He is now an Associate Professor at Faculty of Electrical and Computer Engineering, Urmia University, Urmia, Iran. His research interests include analysis and applications of power electronics and electric power system studies.



M. Farhadi-Kangarlu was born in Kangarlu, East Azarbaijan, Iran, in 1987. He received the B.Sc., M.Sc. and Ph.D. degrees (first class Hons.) all in Electrical Power Engineering from the University of Tabriz, Tabriz, Iran, in 2008, 2010, and 2014, respectively. His research interests include power electronic converters analysis and design, power quality, and custom power devices. Dr. Farhadi-Kangarlu received the Best Researcher Award of the East Azerbaijan Province in 2011, Khwarizmi Youth National Award and the University of Tabriz Best Student Award in 2012, Best Young Award (in science and technology) of the East Azerbaijan Province in 2013, IEEE Iran Section Distinguished Ph.D. Thesis Award, and Iran National Elites Foundation Research Grant Award in 2015 and 2018. He has published more than 50 research papers, registered 7 patents, and co-authored a book. He joined the Faculty of Engineering, Urmia University, Iran in September 2014, where he is an Assistant Professor.



M. Farzinnia was born in Miyaneh, Iran in 1991. He received B.Sc. degree in Electrical Engineering from Urmia University, Urmia, Iran, in 2012, the M.Sc. degree in 2014 from University of Tabriz, Tabriz, Iran. Currently, He is Ph.D. student in Electrical Engineering in Urmia University. He is also licensed as the after-sales engineer of Kraftpowercon Sweden AB and Castlet Co. in Middle East area. His current research interests include, power quality, and the related problems to renewable energy such as, MPPT.



© 2019 by the authors. Licensee IUST, Tehran, Iran. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution-NonCommercial 4.0 International (CC BY-NC 4.0) license (<https://creativecommons.org/licenses/by-nc/4.0/>).