Iranian Journal of Electrical and Electronic Engineering 01 (2020) 48–57
Special Issue on Electrical Machines and Drives

IUST
Iran University of Science and Technology

Iranian Journal of Electrical and Electronic Engineering

Journal Homepage: ijeee.iust.ac.ir

Research Paper

Conduction and Dead-Time Voltage Drops Estimation of Asymmetric Cascaded H-Bridge Converters Utilizing Level-Shifted PWM Scheme

S. Mohamadian*(C.A.) and H. Azizi Moghaddam**

Abstract: Linear AC power supplies can be replaced by their nonlinear switching counterparts due to the lower voltage drops and higher efficiency and power density of switching-mode inverters. Multilevel cascaded H-bridge (CHB) converters are the preferred inverter structure because of modular configuration, control, and protection. The output voltage quality in CHB converters depends on the number of output levels. Asymmetric CHBs (ACHBs) produce an output voltage with higher number of levels with respect to CHBs for the same number of cascaded modules. This results in the reduction of power supply size, voltage drops, and losses. Considering the relative high switch counts, analysis of the effect of conduction and dead-time voltage drops on the inverter output characteristics is an important challenge in designing multilevel converters. In this paper, a generic algorithm is presented to calculate the conduction and dead-time voltage drops of ACHBs utilizing level-shifted modulation. These voltage drops give the necessary information for the design of heatsinks, switch selection, output impedance estimation, and the compensation schemes. It is shown through theoretical and simulation studies that the aforementioned voltage drops of ACHBs are to be calculated in a different manner with respect to the CHBs which mostly use the phase-shifted modulation.

Keywords: ACHB, Conduction and Dead-Time Voltage Drops, Equivalent Impedance, Level-Shifted Modulation, Switching Pattern.

1 Introduction

AC power supplies are classified in linear and nonlinear (switching-mode) categories. The main advantage of the linear power supplies such as push-pull amplifiers, which employ the semiconductor devices in their active region, is their high dynamic response while their disadvantages are high voltage drops and power losses, the use of large heatsinks, and large size [1, 2]. On the other hand, nonlinear power supplies utilize the semiconductor devices as the ON/OFF switches in their saturation and cutoff regions within an inverter structure. Switching-mode nonlinear AC power supplies have benefits such as low power losses and high power density.

Multilevel structures can be used as the building-blocks of nonlinear AC power supplies in order to decrease the harmonic content of the output voltage and to decrease the voltage and current stresses across the semiconductor switches. Cascaded H-bridge (CHB) multilevel inverters are of great usage due to their modular structure, control, and protection [3, 4]. In conventional CHB inverters, all the single-phase H-bridges (SPHB) modules have the same dc-link voltage. While, in asymmetric CHB (ACHB) configuration, the dc-link voltages are in geometric progression with a factor of two (binary) [5, 6], three (ternary) [7-9], or other factors [10-14]. Consequently, higher numbers of output voltage levels are achieved by the ACHB compared to the conventional CHBs. As an example, an

Iranian Journal of Electrical and Electronic Engineering, 2020.
Paper first received 11 May 2019, revised 26 November 2019, and accepted 29 November 2019.
* The author is with the Department of Engineering, Damghan University, Damghan, Iran.
E-mail: s.mohamadian@du.ac.ir.
** The author is with the Rotating Electrical Machines Research group, Niroo Research Institute, Tehran, Iran.
E-mail: hmoghaddam@nri.ac.ir.
Corresponding Author: S. Mohamadian.

11-level waveform is obtained with 5 cascaded SPHBs in symmetrical configuration while, 63 voltage levels are synthesized through a binary ACHB inverter with the same number of cascaded SPHBs. Total harmonic distortion (THD) of the no-load voltage in an 11-level waveform is approximately 11% while it is less than 2% for a 63-level waveform. This results in a significant reduction in the size of the ACHB inverter compared to its symmetrical counterpart for the same output voltage THD. In addition, the reduction of the number of cascaded SPHBs is translated into the lower power losses arising from the conduction, switching and dead-time voltage drops which makes the application of ACHB converters very beneficial specifically in low-voltage high-current uses. Totally, ACHB converters are finding more and more industrial applications in recent years due to their aforementioned advantages [15, 16].

However, the issue of conduction and dead-time voltage drops in symmetrical and asymmetrical CHBs is very crucial, especially in low-voltage applications. As an illustration, considering an amplitude of 31 V for the output voltage of a binary 63-level ACHB, the dc-link voltage of the first SPHB, i.e., $1V_{DC}$ in Fig. 1, should be equal to 1 V irrespective of the voltage drops. This indicates the importance of estimation and compensation for the voltage drops and nonlinear effects of the SPHBs. In [17], after conducting a thorough literature review over the various methods used for the compensation of inverter nonlinearities, a comprehensive approach is presented for the estimation and compensation of nonlinear effects in conventional multilevel CHBs with the phase-shifted pulse-width-modulation (PS-PWM) switching scheme. In [18], a characterizing algorithm has been presented for the identification of multilevel CHBs nonlinearities. While, as will be shown in the following of this paper, the estimation procedure is different in ACHB multilevel inverters in which the level-shifted PWM (LS-PWM) is utilized. This is due to the fact that the devices' conduction voltage drops are functions of modulation scheme [19]. Furthermore, it will be shown in this paper that, unlike the PS-PWM strategy, the dead-time voltage drops change as the modulation index (MI) varies when LS-PWM is used. Besides, one crucial challenge in designing AC power supplies is the estimation of their output impedance to address the issue of impedance matching with the load [20].

In this paper, a novel methodology is devised to estimate the devices' ON-state and dead-time voltage drops in ACHB inverters with LS-PWM scheme. For the sake of brevity, the proposed method is explained for the case of voltage drops and nonlinear effects estimation in a generic binary ACHB circuit while it could be extended to any ACHB configuration. In addition, the output impedance of the multilevel inverter is calculated based on the proposed approach.

The paper is structured as follows. In Section 2, the switching concepts of the LS-PWM in a binary ACHB circuit are explained. A generic approach will be presented in Section 3 to estimate the conduction and dead-time voltage drops in an ACHB inverter. Section 4 is dedicated to the implementation and simulation studies of the proposed scheme in MATLAB/Simulink environment. The aforementioned voltage drops for an example of 7-level ACHB are calculated and compared based on both simulation and the proposed theoretical studies. Finally, the paper is concluded in Section 5.

2 Operation Principles, Level-Shifted Modulation, and Switching Pattern in Binary ACHB Inverter

The circuit diagram of a single-phase ACHB inverter is shown in Fig. 1. The maximum number of achievable levels in the output voltage of a binary ACHB is defined as in (1):

$$L_{ph}^{bin} = 2^{(N+1)} - 1 \tag{1}$$

in which, N indicates the number of SPHBs.

Multi-carrier PWM (MC-PWM) is the most prevalent switching scheme among various PWM strategies which have been proposed for switching of CHB multilevel inverters [15, 16]. MC-PWM strategy itself is generally categorized in phase-shifted (PS) and level-shifted (LS) schemes. PS-PWM is widely used in conventional symmetrical CHB inverters due to the uniform power distribution among different modules [3, 4, 17, 21]. In PS-PWM, N carriers are distributed horizontally in a period of reference voltage with a phase shift of $180^{o}/N$ in order to generate a $(2N+1)$-level voltage

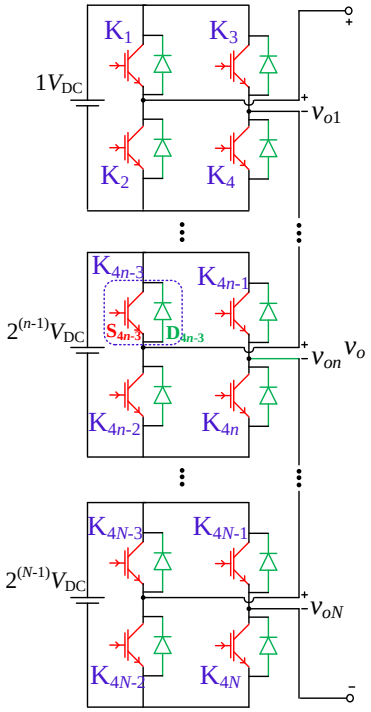

Fig. 1 Single-phase binary ACHB.

waveform [4]. Since the carrier waveforms are not in phase, excessive *dv*/*dt* stresses are created in the phase-to-phase and phase-to-neutral voltages [22]. On the other hand, various LS-PWM strategies are utilized for switching of ACHB multilevel inverters [4, 23]. In LS-PWM, there are $2(2^N\text{-}1)$ triangular carrier waveforms with the same frequency and amplitude which cover the interval of $[-(2^N\text{-}1)V_{DC}, (2^N\text{-}1)V_{DC}]$ contiguously in order to produce a $(2^{N+1}\text{-}1)$-level waveform at the output. $1V_{DC}$, is the dc-link voltage of the first SPHB. A single sinusoidal reference waveform is compared against the carrier waveforms to determine the switching instances of the semiconductor devices.

There are three possible schemes depending on how the carriers are disposed which are: (1) alternative phase opposition disposition (APOD) in which each carrier has a phase shift of 180 degrees with respect to the neighboring ones, (2) phase opposition disposition (POD) where all the carriers higher than the sinusoidal reference zero are in-phase and 180º-phase-shifted with respect to those which are lower than the sinusoidal reference zero, and (3) in-phase disposition (IPD) in which all the carriers are in-phase. Among the three schemes, IPD introduces the lowest harmonic content in the line voltage [22, 24].

Contrary to the PS-PWM used in symmetrical CHBs where a unique carrier is dedicated to each SPHB, a combination of the carriers is utilized for switching each SPHB in ACHB multilevel inverter. In this section, the procedure to generate the switching pulses is explained for a case of 7-level inverter. With N=2 in Fig. 1, $7=2^{2+1}\text{-}1$ levels are produced according to Eq. (1). As mentioned previously, there are $2^N\text{-}1$ carriers higher than the sinusoidal reference zero in a $(2^{N+1}\text{-}1)$-level ACHB. Consequently, in LS-PWM, $2^N\text{+}1$ regions, i.e., region 0 to region 2^N, are generated in the voltage positive half-cycle due to the intersection of the reference and carrier waveforms. For instance, these regions are illustrated for the 7-level ACHB in Fig. 2.
In Fig. 2, IPD-PWM is used in order to determine the switching instants. In this modulation method, six carriers are compared against the reference. Based on Fig. 2, the carriers cover an interval of $[-3V_{DC}, 3V_{DC}]$ contiguously. The modulation index (MI) is considered as 1 in Fig. 2. The purpose is to produce the switching commands for the devices by using the OR, AND, and XOR logic gates. The inputs to these gates come from the comparators which detect the difference between reference and each carrier waveform (Fig. 2(b)). If the reference voltage in the positive (negative) half-cycle is higher (lower) than the carrier, then the comparator output will be 1 otherwise it will be zero.

The outputs of the comparators shown in Fig. 2(b) are listed in Table 1 for a quarter-cycle of the reference waveform, i.e., regions 0-4. In this table, the symbol ☐ indicates that the output toggles between the two states of 0 and 1. According to Table 1 and Fig. 2, all the carriers cr1-cr3 are higher than the reference within $(0,\theta_1)$ (region 0) and the ACHB output voltage must be zero. Thus, in this interval, a freewheeling path is created by switches (K_2, K_4) and (K_6, K_8) in order to set v_{o1}, v_{o2}, and v_o to zero. It is worth mentioning that the voltages $+(2^n\text{-}1)V_{DC}$ and $-(2^n\text{-}1)V_{DC}$ are applied across the n-th SPHB output by switching (K_{4n}, $K_{4n\text{-}3}$) and ($K_{4n\text{-}1}$, $K_{4n\text{-}2}$), respectively. Also, the zero output voltage of v_{on} is applied by simultaneous conduction of K_{4n} and $K_{4n\text{-}2}$. Furthermore, the switching pulses of the devices in one leg, e.g., ($K_{4n\text{-}3}$, $K_{4n\text{-}2}$) or ($K_{4n\text{-}1}$, K_{4n}), must be complementary.

During (θ_1, θ_2) (region 1), the outputs of COMP2 and COMP3 are zero and that of COMP1 switches between the two states of 0 and 1. In this interval, v_o varies between 0 and $1V_{DC}$. In other words, a combination of (1,0,0) for the respective three comparator outputs (COMP1, COMP2, COMP3) indicates the conduction of (K_1, K_4) and (K_6, K_8) to apply $1V_{DC}$ and 0 at the first and second SPHB outputs, respectively. During (θ_2, θ_3) (region 2), the output of COMP2 is toggling while those of COMP1 and COMP3 are at 1 and 0, respectively. For the state of (1,1,0), switches (K_2, K_4) and (K_5, K_8) are ON to have $v_{o1}=0$ and $v_{o2}=2V_{DC}$ and the state of (1,0,0) shows that switches (K_1, K_4) and (K_6, K_8) are ON to have $v_{o1}=1V_{DC}$ and $v_{o2}=0$. Within (θ_3, θ_4) (region 3), the outputs of COMP1 and COMP2 are 1 and that of COMP3 is toggling. The state of (1,1,1) indicates the conduction of (K_1, K_4) and (K_5, K_8) to make $v_o=3V_{DC}$.

According to the above explanations, $v_{o1}=+1V_{DC}$ whenever the XOR of the three comparator outputs (COMP1-COMP3) is 1. Consequently, the XOR of these three outputs is applied to K_1 and the NOT of them is applied to K_2 as shown in Fig. 3. Also, $v_{o2}=+2V_{DC}$ whenever the output of COMP2 is 1 and, therefore, it can be directly applied to the gate of K_5 and its NOT to the gate of K_6. Based on the same principles,

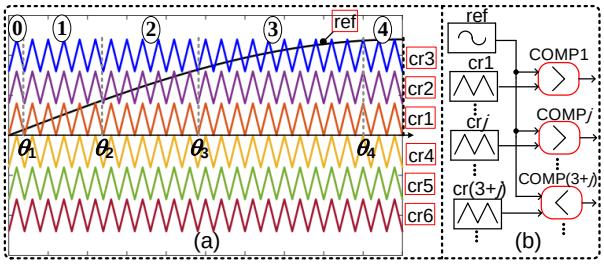

Fig. 2 a) Reference and carrier waveforms in a quarter-cycle for a 7-level ACHB converter and the regions created by the comparisons and b) comparison of the reference against the carrier signals.

Table 1 Comparators outputs for a quarter-cycle in 7-level ACHB.

Region	(COMP1, COMP2, COMP3)	v_o
0: $(0, \theta_1)$	(0, 0, 0)	0
1: (θ_1, θ_2)	(☐, 0, 0)	$0\text{-}1V_{DC}$
2: (θ_2, θ_3)	(1, ☐, 0)	$1V_{DC}\text{ -}2V_{DC}$
3: (θ_3, θ_4)	(1, 1, ☐)	$2V_{DC}\text{ -}3V_{DC}$
4: $(\theta_4, \pi/4)$	(1, 1, 1)	$3V_{DC}$

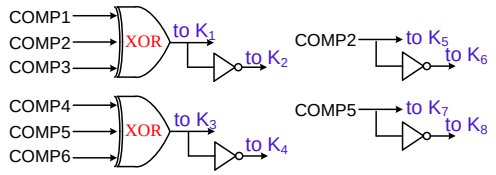

Fig. 3 Generating switching pulses for 7-level ACHB.

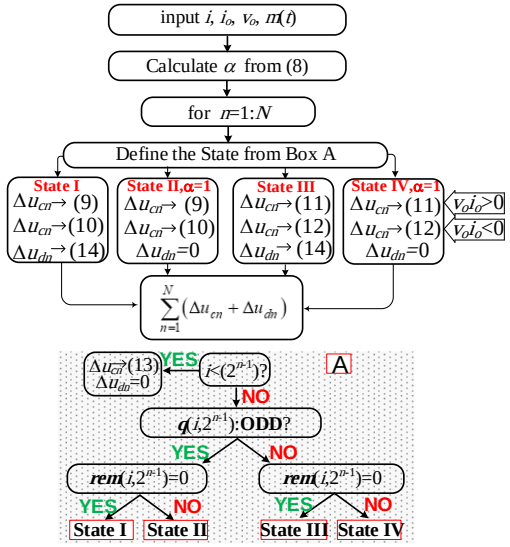

Fig. 4 Devised flowchart in estimating the conduction and dead-time voltage drops in ACHB converters (Box A indicates the procedure to determine the State of region *i*).

the gating signals for (K_3, K_4) and (K_7, K_8) are provided as shown in Fig. 3 according to the comparisons between the carrier signals cr4-cr6 and the reference waveform.

As a general rule, in the region *i*, with i=0,1,2,...,2^N, if $i<2^{n-1}$ then the *n*-th SPHB will apply zero voltage at its output. Otherwise, there are two possibilities: (1) the quotient of *i* divided by 2^{n-1}, i.e., $q(i, 2^{n-1})$, is odd. If the remainder of this division, that is $rem(i, 2^{n-1})$, is zero, then *n*-th SPHB will output $\pm(2^{n-1})V_{DC}$ for the periods in which the absolute reference waveform is higher than the absolute carrier, otherwise, it will output zero volts in region *i* (State I) and; conversely, if the $rem(i, 2^{n-1})$ is not zero, then *n*-th SPHB will apply $\pm(2^{n-1})V_{DC}$ for the entire region *i* (State II). (2) if $q(i, 2^{n-1})$ is even. In this case, if $rem(i, 2^{n-1})$ is zero, then *n*-th SPHB will output zero volts for the periods in which the absolute reference waveform is higher than the absolute carrier, otherwise, it will output $\pm(2^{n-1})V_{DC}$ volts in region *i* (State III) and; conversely, if the $rem(i, 2^{n-1})$ is not zero, then *n*-th SPHB will apply zero volts for the entire region *i* (State IV). Fig. 4 illustrates these explanations diagrammatically. It should be noted that in order to reduce the burden of online computations for ACHB inverters with high number of output levels and switching regions, the flowchart of Fig. 4 can be calculated offline. In other words, there is no need to compute the conditional loops of Fig. 4 online in each period of the carrier signal.

3 The Proposed Algorithm in Estimating Conduction and Dead-Time Voltage Drops of ACHB Converters Using LS-PWM

3.1 Conduction Voltage Drop of Semiconductor Devices

In [19], in order to calculate the devices' conduction voltage drops in a conventional two-level converter; first, the average local voltage drop is obtained in a period of carrier. Then, a mathematical equation based on the modulation index (MI) and load power factor ($\cos(\phi)$) is extracted for the total average conduction voltage drop by integrating the local voltage drops in a period of reference signal. Based on a similar approach, in [17], MI is sampled at the maximum and minimum points of every single carrier in a PS-modulated multilevel CHB and the SPHBs' local voltage drops are calculated according to the sampled MI and current polarity. Then, the local voltage drops are summed to achieve the total conduction voltage drop in the converter.

In the two aforementioned methods which use the unipolar PWM, the reference and carriers have intersections for different values of MI. While, in the LS-PWM and for lower values of MI, some of the carriers do not intersect with the reference. In addition, gating pulses of each SPHB in LS-PWM is a combination of the output of all comparators. On the other hand, pulses in PS-PWM are provided individually for each SPHB by comparing the reference with its specific carrier. Thus, the conduction voltage drop in LS-PWM scheme could not be independently calculated for each SPHB via integrating or summing the local voltage drops in each carrier period.

As mentioned in Section II, (2^N+1) regions are generated through comparing the carrier signals with the reference in LS- modulated $(2^{N+1}-1)$-level ACHB (Fig. 2). In this paper, a generic approach is extracted to compute the conduction voltage drops in each region for different SPHBs.

Based on Fig. 1 and Table 2, the conduction voltage drop, Du_{cn}, for each SPHB in each region is calculated depending on the current polarity. u_S and u_D in Table 2 are the instantaneous voltage drops of transistors and diodes, respectively. For instance, in Table 2, if the output voltage and current of the *n*-th SPHB are

Table 2 Conduction voltage drop, Δu_{cn}, based on the output voltage and current polarity.

(K_p, K_q)	v_{on}	i_o	Δu_{cn}
(S_{4n-3},S_{4n})	$(2^{n-1})V_{DC}$	>0	$-2u_S$
(D_{4n-2},S_{4n})	0	>0	$-(u_S+u_D)$
(D_{4n-2},D_{4n-1})	$-(2^{n-1})V_{DC}$	>0	$-2u_D$
(S_{4n},D_{4n-2})	0	>0	$-(u_S+u_D)$
(D_{4n-3},D_{4n})	$(2^{n-1})V_{DC}$	<0	$2u_D$
(S_{4n-2},D_{4n})	0	<0	(u_S+u_D)
(S_{4n-2},S_{4n-1})	$-(2^{n-1})V_{DC}$	<0	$2u_S$
(D_{4n},S_{4n-2})	0	<0	(u_S+u_D)

positive, then switches S_{4n-3} and S_{4n} are conducting and the module voltage drop will be $-2u_S$ compared to the case in which the devices are considered as ideal.

On the other hand, the instantaneous voltage drops of the devices, u_S and u_D in Table 2, are functions of their instantaneous current according to the following formula:

$$u_S = U_{SF} + r_S i_l; \quad u_D = U_{DF} + r_D i_l \tag{2}$$

In (2), U_{SF} and U_{DF} are transistor and diode threshold voltages, respectively. Also, r_S and r_D are the ON-state resistances of transistors and diodes, respectively.

The local average voltage drop is obtained via integrating the load current, i_o, in every switching or carrier period. For this purpose, the line equation representing the k-th carrier signal in Fig. 5, $a_c(t)$, is extracted first as (time origin of the line is assumed to be zero, i.e., t=0)

$$a_c(t) = \begin{cases} V_{DC}\left(\frac{2}{T_C}t + k - 1\right); & 0 \langle t \langle \frac{T_C}{2} \\ V_{DC}\left(\frac{-2}{T_C}t + k + 1\right); & \frac{T_C}{2} \langle t \langle T_C \end{cases} \tag{3}$$

where, T_C is the carrier period.

Intersection of the reference and the k-th carrier, that is point t_a in Fig. 5, can be calculated from (4).

$$t_\alpha = \frac{T_C}{2}\left(\frac{m(t)}{V_{DC}} + 1 - k\right) \tag{4}$$

in which, $m(t)$ is the modulation function with the following relation,

$$m(t) = M \sin(\omega t); \qquad M \in [0,1] \tag{5}$$

where

$$M = \frac{V^*}{(2^N - 1)V_{DC}} \tag{6}$$

V^* is the maximum of the reference voltage in (6).

Considering the load current as constant within [0, T_C/2] (equal to I_l), the average value of the device current, $i_{l(ave)}$, is calculated in (7a) when the device is conducting during [0, t_α] or in (7b) when the device is conducting within [t_α, T_C/2].

$$i_{l(ave)} = \frac{1}{\frac{T_C}{2}}\int_0^{t_\alpha} I_l dt = \frac{t_\alpha}{\frac{T_C}{2}} I_l = \alpha I_l; \quad 0 < t < t_\alpha \tag{7a}$$

$$i_{l(ave)} = \frac{1}{\frac{T_C}{2}}\int_{t_\alpha}^{\frac{T_C}{2}} I_l dt = (1-\alpha) I_l; \quad t_\alpha < t < \frac{T_C}{2} \tag{7b}$$

where, α is the device duty-cycle and is calculated for the k-th carrier as follows:

$$\alpha = \frac{t_\alpha}{\frac{T_c}{2}} = \frac{m(t)}{V_{DC}} + 1 - k \tag{8}$$

Accordingly, for State I and positive $v_o.i_o$ ($v_o.i_o$>0), Table 2 shows that two transistors of the SPHB are conducting during [0, t_α] with the instantaneous voltage drop of $\mp 2u_S$ (minus '-' for positive v_o and plus '+' for negative v_o) and one transistor and one diode are conducting during [t_α, T_C/2] with the instantaneous voltage drop of $\mp(u_S + u_D)$. Thus, the SPHB average ON-state voltage drop for State I is

$$\begin{aligned} \Delta u_{cn} &= -\big[2\times(U_{SF} + r_S I_l \alpha) + \\ &\quad + (U_{SF} + r_S I_l (1-\alpha) + U_{DF} + r_D I_l (1-\alpha))\big]\times \mathrm{sgn}(I_l) \\ &= -(U_{1F} + r_S I_l (1+\alpha) + r_D I_l (1-\alpha))\mathrm{sgn}(I_l) \end{aligned} \tag{9}$$

In (9), sgn() is the signum function and U_{1F} = $3U_{SF}$+U_{DF}. If the current, i_o, and voltage, v_o, are of opposite polarity, that is negative $v_o.i_o$, then Table 2 shows that

$$\begin{aligned} \Delta u_{cn} &= -\big[2\times(U_{DF} + r_D I_l \alpha) + \\ &\quad + (U_{SF} + r_S I_l (1-\alpha) + U_{DF} + r_D I_l (1-\alpha))\big]\times \mathrm{sgn}(I_l) \\ &= -(U_{2F} + r_D I_l (1+\alpha) + r_S I_l (1-\alpha))\mathrm{sgn}(I_l) \end{aligned} \tag{10}$$

where, U_{2F}=$3U_{DF}$+U_{SF}.

By replacing a =1, U_{1F} =$2U_{SF}$, and U_{2F} =$2U_{DF}$ in (9) and (10), the respective equations of the average ON-state voltage drops for positive and negative $v_o.i_o$ are obtained for State II.

For State III and positive $v_o.i_o$, according to Table 2, one transistor and diode in SPHB conduct during [0, t_α] with the instantaneous conducting voltage drop of $\mp(u_S + u_D)$and two transistors conduct during [t_α, T_C/2] with the instantaneous voltage drop of $\mp 2u_S$. Thus, the SPHB average ON-state voltage drop for State III is

$$\begin{aligned} \Delta u_{cn} &= -\big[2\times(U_{SF} + r_S I_l (1-\alpha)) + \\ &\quad + (U_{SF} + r_S I_l \alpha + U_{DF} + r_D I_l \alpha)\big]\times \mathrm{sgn}(I_l) \\ &= -(U_{1F} + r_S I_l (2-\alpha) + r_D I_l \alpha)\mathrm{sgn}(I_l) \end{aligned} \tag{11}$$

and for negative $v_o.i_o$, we have

$$\begin{aligned} \Delta u_{cn} &= -\big[2\times(U_{DF} + r_D I_l (1-\alpha)) + \\ &\quad + (U_{SF} + r_S I_l \alpha + U_{DF} + r_D I_l \alpha)\big]\times \mathrm{sgn}(I_l) \\ &= -(U_{2F} + r_D I_l (2-\alpha) + r_S I_l \alpha)\mathrm{sgn}(I_l) \end{aligned} \tag{12}$$

By replacing α =1, U_{1F} =$2U_{SF}$, and U_{2F} =$2U_{DF}$ in (11) and (12), the respective equations of the average ON-state voltage drop for positive and negative $v_o.i_o$ are obtained for State IV.

It should be mentioned that for $i < 2^{n-1}$, switches D_{4n-2}

and S_{4n} conduct for positive current and switches D_{4n} and S_{4n-2} conduct for negative current for the entire region, i.e., α =1. Hence, one transistor and one diode conduct and the voltage drop is as follows

$$\Delta u_{cn} = -\left(U_{SF} + r_S I_l + U_{DF} + r_D I_l\right)\mathrm{sgn}(I_l) \quad (13)$$

Finally, the total voltage drop is obtained through adding all the SPHBs' voltage drops based on the flowchart shown in Fig. 4. As an example, the procedure is summarized in Table 3 for seven-level ACHB.

3.2 Dead-Time Voltage Drop

Assuming ideal transistors, the ON/OFF pulses of the upper and lower devices in each SPHB's leg are complementary. In other words, one transistor is gated OFF once the ON pulse is sent to the other. However, in reality, the devices have turn-on and turn-off delay times, t_{don} and t_{doff}. Consequently, if the ON and OFF commands of the two transistors are sent simultaneously, one transistor may turn on prior to the complete turn-off of the other one resulting in a short-circuit of the DC-link voltage source. In order to avoid this short-circuit, a time interval in the range of few microseconds called dead-time, T_d, is exerted between the gating pulses of the two switches in a leg. Although dead-time is negligible compared to the period of the output voltage in industrial applications, it results in voltage drop which could be significant specifically at low voltages [17, 25].

In [17], comprehensive explanations are presented for the computation of dead-time voltage drop in multilevel CHBs utilizing PS-PWM. In PS-PWM, the reference and carrier signals have intersections for different values of MI. In other words, devices in each SPHB's leg are turned off twice and turned on once or vice versa in every period of carrier waveform. This results in constant dead-time voltage drop irrespective of MI [17, 19, 25]. However, the situation is different for LS-PWM scheme because: (1) switching of each SPHB device is determined based on the combination of different comparator outputs and; therefore, some switches may be constantly ON or OFF in some regions. (2) Contrary to PS-PWM in which the switching occurs in both legs of the SPHB in every carrier period, switch S_{4n-1} is constantly OFF in LS-PWM for positive v_{on} and the switching does not occur in the right leg. Similarly, S_{4n-3} is constantly OFF for negative v_{on} and switching does not take place in the left leg.

Obviously, if the SPHB outputs constant 0 or $\pm(2^{n-1})V_{DC}$ volts within a region, i.e., States II and IV, the dead-time voltage drop will be zero. Otherwise, there will be a case of only one leg switching and the dead-time voltage drop, Δu_{dn}, will be half of that calculated in [17], i.e.,

$$\Delta u_{dn} = -\left(T_d + t_{don} - t_{doff}\right) f_c\, 2^{n-1} V_{DC}\, \mathrm{sgn}(I_l) \quad (14)$$

Table 3 Conduction voltage drops of two SPHBs, Du_{c1} and Du_{c2}, in 7-level ACHB converter.

Δu_{c2}		2nd SPHB State	Δu_{c1}		1st SPHB State	Region
$v_o i_o$<0	$v_o i_o$>0		$v_o i_o$<0	$v_o i_o$>0		
(13)	(13)		(13)	(13)		0
(13)	(13)		(10)	(9)	I	1
(10)	(9)	I	(12)	(11)	III	2
(10)**	(9)*	II	(10)	(9)	I	3
(12)	(11)	III	(12)	(11)	III	4

* with α = 1, $U_{1F} = 2U_{SF}$
** with α = 1, $U_{1F} = 2U_{DF}$

Thus, the total dead-time voltage drop of multilevel ACHB is obtained based on the proposed algorithm shown in Fig. 4.

4 Simulation Studies

In order to verify the correctness of the presented approach in estimating the ON-state and dead-time voltage drops, a seven-level ACHB is implemented in MATLAB/Simulink environment. The implemented model is shown in Fig. 6. As shown in Fig. 6(a), a detailed model of the switching devices can be utilized. In other words, ON-state resistance and threshold voltage of the devices and dead-time can be adjusted in the software. Two seven-level ACHB converters one without losses (Fig. 6(b)) and the other considering the non-idealities (Fig. 6(a)) are simulated simultaneously and the output voltages of both are compared. The difference between the two outputs must correspond to the voltage drop acquired from the proposed algorithm shown in Fig. 6(c).

Simulation results for the case of unity modulation index and nearly resistive load are shown in Fig. 7. The ON-state resistance of transistors and diodes are set to 80mΩ and 60mΩ, respectively. Also, the diode threshold voltage is adjusted to 0.8V. In Fig. 7, $\Delta u_{c,sim}$ is the conduction voltage drops obtained from the difference between the output voltages of ideal and real converters and $\Delta u_{c,th}$ is that computed based on the presented algorithm.

From Fig. 7, the voltage drops are almost the same disregarding a little discrepancy in the amplitude of voltage drops. This is because of the fact that the load current in the real converter is somehow different from that of ideal one due to the voltage drops. Based on FFT analysis, the difference between the RMS values of the two converters' outputs is 21.52–16.21 = 5.35V which is very close to the RMS value of $\Delta u_{c,th}$ that is 5.72V. Simulation results in Fig. 7 are dedicated to the low output voltage and high current conditions (23V and 30A disregarding the losses) in which the conduction losses are obviously remarkable compared to the load voltage. Furthermore, the simulation results for duty-cycle, α in (8), are shown in Fig. 8. As mentioned

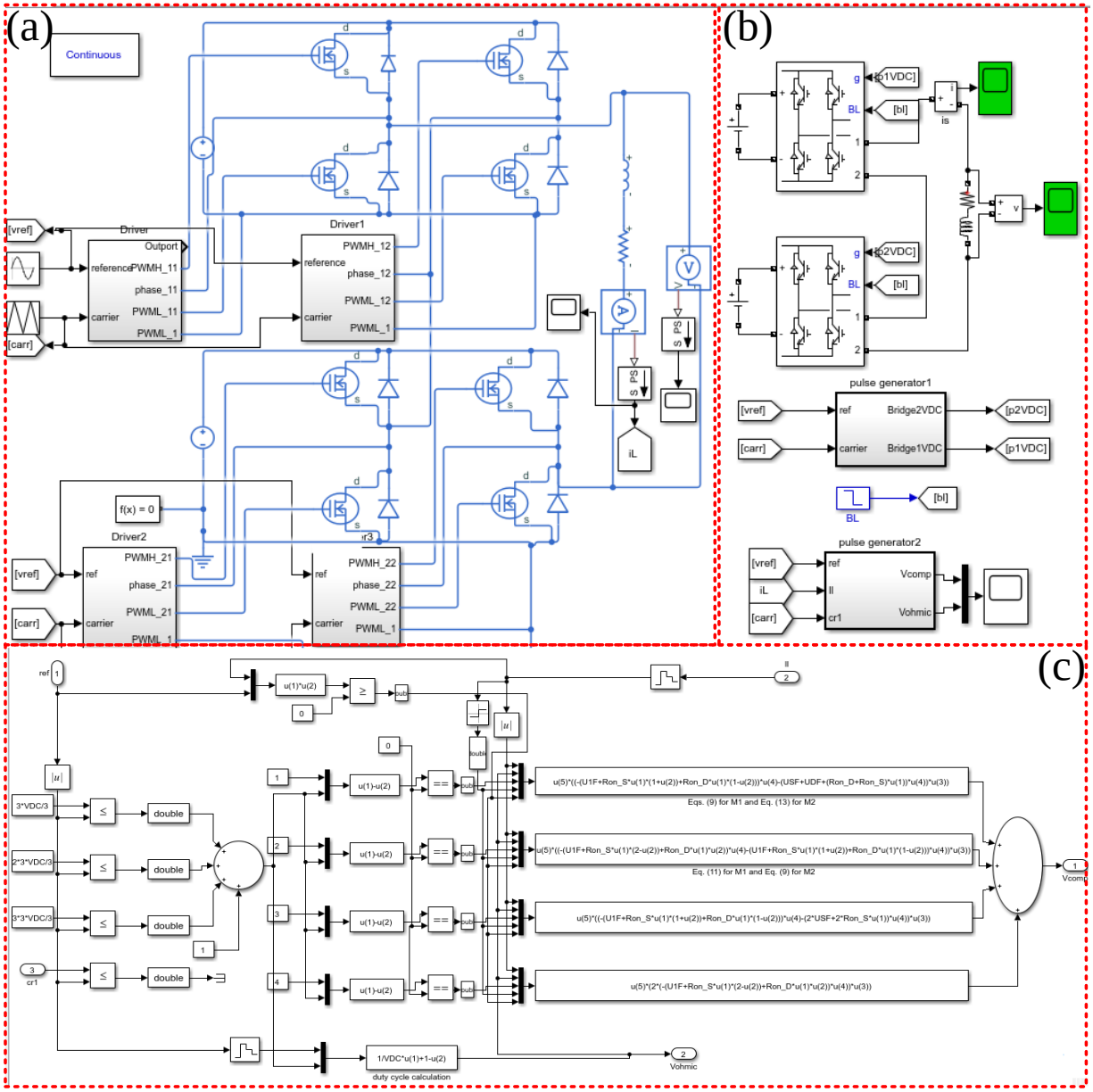

Fig. 6 Implemented 7-level ACHB in MATLAB/Simulink: a) detailed model, b) ideal model, and c) implemented proposed algorithm to obtain the theoretical voltage drop.

previously, the reference waveform is sampled twice in a carrier period (f_c = 10kHz) for the sake of α calculation. According to Fig. 8, α varies between 0 and 1 in different regions for the unity MI.

Then, ON-state resistances of the devices are set to a negligible value and a dead-time equal to 2 microseconds is applied to one of the converters. The results for the dead-time voltage drop based on the proposed scheme, $\Delta u_{d,sim}$, is shown in Fig. 9. In this figure, f_c = 10kHz, MI=1, V_{DC}=100V, and the load is almost resistive. Based on Fig. 9, for i=1, 3 (2nd and 4th regions), the first SPHB is only switched and a voltage drop proportional to $1V_{DC}$ is expectable. While, for i=2, both SPHBs are switched and the equivalent voltage drop will be proportional to $3V_{DC}$. Besides, the RMS value of dead-time voltage drop is 2.487V calculated form the difference between ideal and real converters outputs and it is equal to 2.511V from the proposed algorithm.

In the next stage, the effect of both conduction and dead-time voltage drops are included simultaneously. The simulation results for the output voltages in ideal and real converters and the estimated voltage drop are shown in Fig. 10. In the simulations, V_{DC} =100V, MI=0.1, T_d = 2μsec, and the load power factor angle is 26 degrees. Also, the ON-state resistance of the transistors and diodes are set to 80mΩ and 60mΩ, respectively. As it is obvious from Fig. 10, the switching takes place in regions 0 and 1 due to the low MI and the output voltage is of three-level. According to

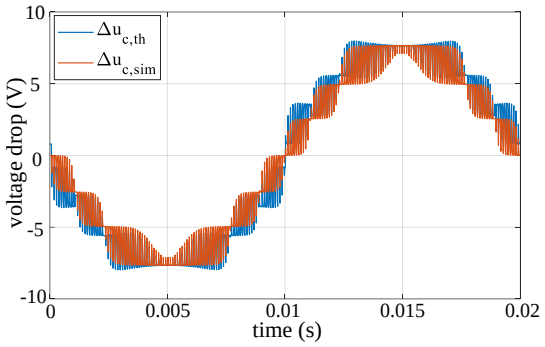

Fig. 7 Simulation and theoretical results for the conduction voltage drop, $\Delta u_{c,sim}$ and $\Delta u_{c,th}$, for resistive load and MI=1.

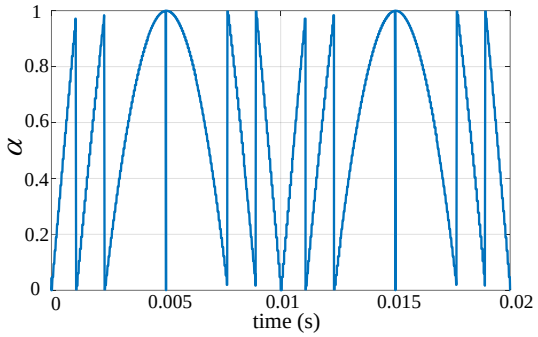

Fig. 8 Duty-cycle, *a*, for MI=1.

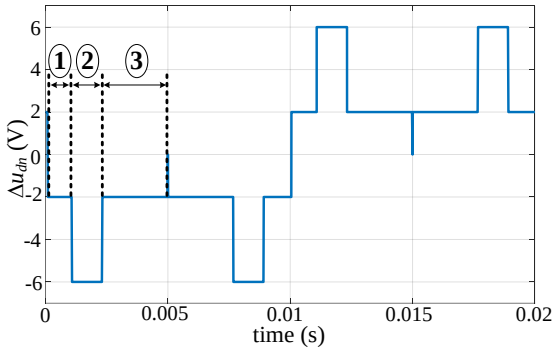

Fig. 9 Dead-time voltage drop calculation based on the proposed algorithm.

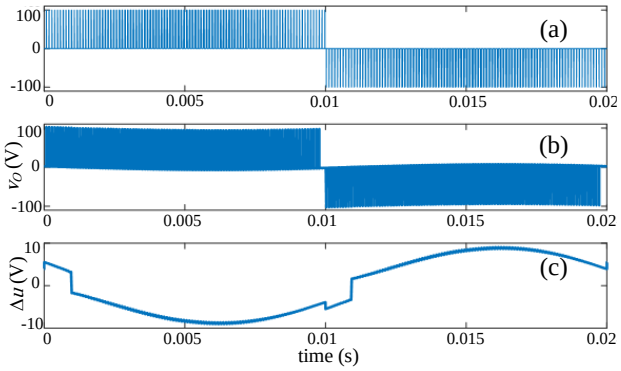

Fig. 10 Output voltage of a) ideal converter, b) real converter, and c) calculated voltage drop via the proposed scheme.

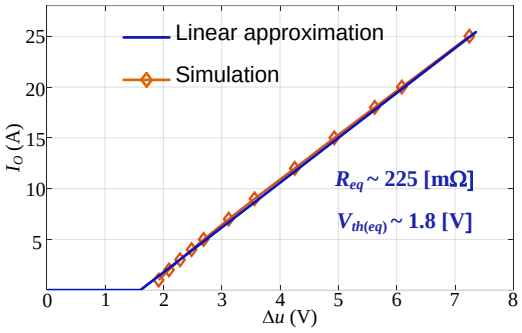

Fig. 11 Output resistance and threshold voltage estimation of 7-level ACHB converter.

FFT analysis, the RMS value of the output voltage is 21.17V in the ideal converter and it is equal to 16.24V in the real converter. The RMS value of the estimated voltage drop is 4.93V which is in great accordance to the simulation results.

One of the advantages of the proposed scheme is its capability in estimating equivalent output impedance of the ACHB converter for various MIs and loading conditions. This could be helpful for applications such as designing power amplifiers and programmable power supplies. For this purpose, the converter equivalent resistance and threshold voltage, R_{eq} and $V_{th(eq)}$, are calculated as 225mΩ and 1.8V, respectively, for the modulation index of 1 and different loading conditions as shown in Fig. 11 (load power factor is equal to 26 degrees).

Table 4 Output equivalent resistance of ACHB for different MIs.

MI	0.1	0.2	0.3	0.4	0.5
R_{eq} [mΩ]	195	220	230	232	230
MI	0.6	0.7	0.8	0.9	1
R_{eq} [mΩ]	235	240	235	233	226

On the other hand, the equivalent output resistance is listed in Table 4 for different MIs. In order to extract R_{eq}, RMS value of the voltage drop is computed for the load currents of 10A and 12A based on the proposed algorithm and their difference is divided by the current difference, i.e., 2A. As can be seen, for low MIs (e.g., 0.1), since the diodes are conducting in the second SPHB and considering lower ON-state resistance of the diodes, the estimated equivalent resistance is lower. Although, transistors in the second SPHB are also conducting for higher MIs and the equivalent will be higher consequently.

5 Conclusion

In this paper, a generic algorithm is presented to estimate the conduction and dead-time voltage drops in multilevel ACHB converters. For this purpose, the switching principles of level-shifted PWM in ACHB inverter is described first and then, the average voltage

drop is estimated based on the calculated duty-cycle and average current of semiconductor devices in each switching period. It is shown by the implementation of the proposed scheme in MATLAB/Simulnik that the conduction and dead-time voltage drops are functions of modulation index and load power-factor angle. Conversely, the dead-time voltage drop is constant in conventional CHB multilevel inverters. Also, the capability of the proposed scheme in estimating output equivalent resistance of ACHB is illustrated. It should be mentioned that the estimation of the voltage drops is mandatory in selecting the appropriate semiconductor devices, designing heatsinks, estimation of the equivalent resistance of the AC power supply, and compensating the nonlinear effects of the inverter voltage drops.

References

[1] G. Gong, D. Hassler, and J. W. Kolar, "A comparative study of multicell amplifiers for AC-power-source applications," *IEEE Transactions on Power Electronics*, Vol. 26, No. 11, pp. 149–164, Jan. 2011.

[2] H. Ertl, J. W. Kolar, and F. C. Zach, "Basic considerations and topologies of switched-mode assisted linear power amplifiers," *IEEE Transactions on Industrial Electronics*, Vol. 44, No. 1, pp. 116–123, Feb. 1997.

[3] M. Malinowski, K. Gopakumar, J. Rodriguez, and M A. Pérez, "A survey on cascaded multilevel inverters," I*EEE Transactions on Industrial Electronics*, Vol. 57, No. 7, pp. 2197–2206, Jul. 2010.

[4] B. P. McGrath, .and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Transactions on Industrial Electronics*, Vol. 49, No. 4, pp. 858–867, Aug. 2002.

[5] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: A competitive solution for high-power applications," *IEEE Transactions on Industry Applications*, Vol. 36, No. 3, pp. 834–841, 2000.

[6] M. MaVnjrekar and T. Lipo, "A hybrid multilevel inverter topology for drive applications," in *IEEE Applied Power Electronics Conference*, Vol. 2, pp. 523–529, Feb. 1998.

[7] J. Dixon, A. A. Breton, F. E. Rios, J. Rodriguez, J. Pontt, and M. A. Perez, "High-power machine drive, using nonredundant 27-level inverters and active front end rectifiers," *IEEE Transactions on Power Electronics*, Vol. 22, No. 6, pp. 2527–2533, Nov. 2007.

[8] C. Rech and J. R. Pinheiro, "Hybrid multilevel converters: Unified analysis and design considerations," *IEEE Transactions on Industrial Electronics*, Vol. 54, No. 2, pp. 1092–1104, Apr. 2007.

[9] N. Prabaharan, Z. Salam, C. Cecati and K. Palanisamy, "Design and implementation of new multilevel inverter topology for trinary sequence using unipolar pulse width modulation," *IEEE Transactions on Industrial Electronics*, May 2019.

[10] J. Song-Manguelle, S. Mariethoz, M. Veenstra, and A. Rufer, "A generalized design principle of a uniform step asymmetrical multilevel converter for high power conversion," in *European Conference on Power Electronics and Applications*, Vol. 1, pp. 1–12, 2001.

[11] S. Mariethoz and A. Rufer, "Design and control of asymmetrical multilevel inverters," IEEE *28th Annual Conference of the Industrial Electronics Society*, IECON 02, Sevilla, Vol. 1, pp. 840–845, 2002.

[12] M. Perez, J. Rodrıguez, J. Pontt, and S. Kouro, "Power distribution in hybrid multi-cell converter with nearest level modulation," in *IEEE International Symposium on Industrial Electronics*, Vigo, pp. 736–741, 2007.

[13] K. Sano and M. Takasaki, "A transformerless D-STATCOM based on a multivoltage cascade converter requiring no DC sources," *IEEE Transactions on Power Electronics*, Vol. 27, No. 6, pp. 2783–2795, Jun. 2012.

[14] J. Pereda and J. Dixon, "High-frequency link: A solution for using only one DC source in asymmetric cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, Vol. 58, No. 9, pp. 3884–3892, Sep. 2011.

[15] M. Soltani, H. Pairo, and A. Shoulaie, "Modelling approach for multi-carrier-based pulse-width modulation techniques utilised in asymmetrical cascaded H-bridge inverters," *IET Power Electronics*, Vol. 12, No. 14, pp. 3822–3832, Nov. 2019.

[16] R. Sajadi, H. Iman-Eini, M. K. Bakhshizadeh, Y. Neyshabouri, and S. Farhangi, "Selective harmonic elimination technique with control of capacitive DC-link voltages in an asymmetric cascaded H-bridge inverter for STATCOM application," *IEEE Transactions on Industrial Electronics*, Vol. 65, No. 11, pp. 8788–8796, Nov. 2018.

[17] A. Mora, J. Juliet, A. Santander, and P. Lezana, "Dead-time and semiconductor voltage drop compensation for cascaded H-bridge converters," *IEEE Transactions on Industrial Electronics*, Vol. 63, No. 12, pp. 7833–7842, Dec. 2016.

[18] S. M. Seyyedzadeh, S. Mohamadian, M. Siami, and A. Shoulaie, "Modeling of the nonlinear characteristics of voltage source inverters for motor self-commissioning," *IEEE Transactions on Power Electronics*, Vol. 34, No. 12, pp. 12154–12164, Dec. 2019.

[19] J. W. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *IEEE Transactions on Industry Applications*, Vol. 27, No. 6, pp. 1063–1075, 1991.

[20] G. Gong, H. Ertl, and J. W. Kolar, "A multi-cell cascaded power amplifier," in *21st Annual IEEE Applied Power Electronics Conference and Exposition (APEC'06)*, Dallas, TX, pp. 7–pp, 2006.

[21] J. Ma, X. Wang, F. Blaabjerg, W. Song, S. Wang and T. Liu, "Real-time calculation method for single-phase cascaded H-bridge inverters based on phase-shifted carrier pulsewidth modulation," *IEEE Transactions on Power Electronics*, Vol. 35, No. 1, pp. 977–987, Jan. 2020.

[22] M. Angulo, P. Lezana, S. Kouro, J. Rodriguez, and B. Wu, "Level-shifted PWM for cascaded multilevel inverters with even power distribution," in *IEEE Power Electronics Specialists Conference*, Orlando, FL, pp. 2373–2378, 2007.

[23] H. Belkamel, S. Mekhilef, A. Masaoud, and M. A. Naeim, "Novel three-phase asymmetrical cascaded multilevel voltage source inverter," *IET Power Electronics*, Vol. 6, No. 8, pp. 1696–1706, Sep. 2013.

[24] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, Vol. 57, No. 8, pp. 2553–2579, Aug. 2010.

[25] M. C. Kang, S. H. Lee, and Y. D. Yoon, "Compensation for inverter nonlinearity considering Voltage drops and switching delays of each leg's switches," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, pp. 1–7, 2016.

S. Mohamadian received his B.Sc. and Ph.D. degrees in Electrical Engineering from Iran University of Science and Technology (IUST), Tehran, Iran, in 2007 and 2016, respectively. Between February 2014 and March 2015, he spent a period as a Visiting Scholar at the University of Trieste, Trieste, Italy, where he worked on research projects regarding high-power multiphase motor drives and multiphase machine modeling and analysis. In 2016, he joined the University of Damghan, Damghan, Iran, where he is currently an Assistant Professor. His research interests include power quality, power electronics, and electrical machines.

H. Azizi Moghaddam received the B.Sc. degree in Electrical Engineering from Shiraz University, Shiraz, Iran, in 2001, and the M.Sc. and Ph.D. degrees in Electrical Engineering from Iran University of Science and Technology (IUST), Tehran, Iran, in 2004 and 2013, respectively. Currently, he is an Assistant Professor at Rotating Electrical Machines group at Niroo Research Institute (NRI), Tehran, Iran. His research interests include design and optimization of electrical machines, electrical machines drives and testing, and power electronics.