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Research Paper

A Dual-Band Low Noise Low Power Local LC Oscillator

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Abstract: In this paper a novel design is presented for a dual-band LC oscillator, using an analytical approach. The core of the proposed circuit contains a cross-coupled CMOS LC oscillator with two serried LC tanks so that the inductors of these tanks have mutual inductance. There are some switches in the circuit that directly changes mutual inductance to produce two different frequencies. This technique increases the oscillation amplitude in the same power consumption that leads to the decrement of phase noise. In other words, using two serried LC tank compensates the injected phase noise from switches. The symmetrical structure is another advantage of the presented design that makes it possible to be used in multiphase oscillator. To assess the quality of the proposed circuit, a dual-band quadrature LC oscillator has been designed to oscillate at 3.6 GHz and 6.4 GHz with 1.5 V supply and 1 mA current consumption, with TSMC 0.18 CMOS practical model. Lastly, simulation results confirm the correctness of analytical results and high proficiency of the proposed design.

Keywords: Dual Band Oscillator, Phase Noise, RF CMOS, Analysis.

1 Introduction

RECENT developments in the communication industry requires coverage of various standards such as GSM, PCS/DCS, and Bluetooth with minimum hardware resources and cost. The main dare for these standards is to design a local oscillator (LO) that meets a wide spectrum, in addition to desirable phase noise performance. On the other hand, a LO covering all of those standards requires the use of steep varactor characteristics and is difficult to implement. Not only varactor tuning cannot provide sufficient tuning range but also its big size is sensitive to input noise. That is why there are growing efforts to get multi-standard LO, focusing on implementation of both broadband LOs and dual-band and multiband LO topologies with low phase noise and low current consumption [1-4].

Various methods have been proposed in order to design multi-band VCO. One scheme is presented in [5] and [6], that a circuit element is added to the oscillator to produce new frequency. In this approach, each time some elements of the circuit are inactive while occupying the chip area. Another approach is switching capacitors and inductors of LC tanks [7-9]. This approach is implemented in many different forms but their main problem is the increment of phase noise resulted from the effects of switches. Although in [10], the effects of switches have been reduced by using a transformer-based current driver, this methodology increases the power consumption. Moreover, some other approaches tried to use a different switching structure to decrease its effects [11, 12]. One more routine is to apply various LC oscillators at different frequencies and enable one of them each time [13] that makes the circuit more voluminous. The other technique is created on the coupling of multiple resonators for low phase noise multi-band RF transceivers. Two units of composite right-/left-handed (CRLH) resonators weaken the phase noise because of the series resonance effect to generate dual frequencies [14]. Also, in [15, 16], mode-switching resonator creates the even and odd-mode of the LC oscillators using MOS switches which avoids the effect of steady-state series resistance and reduction of the phase noise at both frequencies.

As a result, most of the previous works in multi-band oscillators need more power than single band but in this work, not only it does not consume higher power, but

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also less power is needed than single band one, using a novel design. Overall, this paper proposes a dual-band LO architecture that uses two serried LC tank with mutual inductance in which the phase noise of the switches is compensated.

The rest of the paper is organized a follows: Section 2 introduces the basics of the proposed circuit. In Section 3, the impacts of switches are considered. Section 4 shows and analyses the simulation results. Finally, a conclusion is given in Section 5.

2 The Proposed Dual Band Oscillator

The proposed dual-band VCO architecture shown in Fig. 1(a) is designed based on the use of two serried LC tank. Its architecture is almost like the LC cross-coupled oscillator (shown in Fig. 1(b)) that the resonator consists of two LC tanks on each side of cross-couple pair. These two LC tanks have mutual inductors. There are also four switches that are used to change the structure for producing new frequency. The oscillator has two distinct modes. In the first mode switches S1 and S2 are connected while S3 and S4 are OFF. In this state, each two LC tanks with mutual inductors are serried and placed in one side of the LC oscillator. In the second mode, S1 and S2 are disconnected while S3 and S4 are ON. In this state, each side of the cross-coupled oscillator consist two serried LC tank too, but the difference is that they have cross mutual inductance as shown in Fig. 1. In the following, it is shown that how the circuit works.

First, the first state is analyzed; S1 & S2: ON and S3 & S4: OFF. Here two LC resonators with mutual inductance are on one side. Fig 2 shows two serried LC on each side. Regarding Fig. 2, the equivalent impedance of one side can be written as below:

$$Z_{in} = Z_1 + Z_2 \tag{1}$$

where

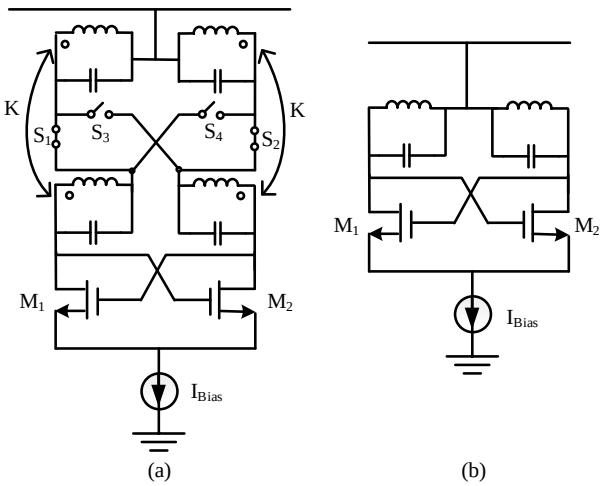


Fig. 1 a) The proposed dual-band cross-coupled oscillator and b) Conventional LC cross-coupled oscillator.

$$Z_{1,2} = \frac{\left(\frac{1}{C_{1,2}}\right)S}{S^2 + \left(\frac{1}{R_{1,2}C_{1,2}}\right)S + \left(\frac{1}{L_{1,2}C_{1,2}}\right)} \tag{2}$$

$$Z_{in} = \frac{\left(\frac{2}{C}\right)S}{S^2 + \left(\frac{1}{RC}\right)S + \left(\frac{1}{LC}\right)} \tag{3}$$

According to KCL and KVL law, we reach:

$$I = I_{R_{1,2}} + I_{C_{1,2}} + I_{L_{1,2}} \tag{4}$$

$$V_{R_{1,2}} = V_{C_{1,2}} = V_{L_{1,2}} \tag{5}$$

As shown in Fig. 2, voltage of inductors can be written as:

$$V_{L_{1,2}} = Ls(I_{L_{1,2}} + KI_{L_{1,2}}) \tag{6}$$

That currents of inductors will be defined as below:

$$I_{L_{1,2}} = I - (I_{R_{1,2}} + I_{C_{1,2}}) \tag{7}$$

where $I_{R1,2}$ and $I_{C1,2}$ are the currents that flow in resistors and capacitors, respectively. Considering the above equations, we have:

$$I_{L_{1,2}} = I - \left(\frac{Ls(I_{L_{1,2}} + KI_{L_{2,1}})}{R} + CLs^2(I_{L_{1,2}} + KI_{L_{2,1}}) \right) \tag{8}$$

By subtracting equations in (8) for indexes 1 and 2, we reach:

$$I_{L_1} = I_{L_2} = I_L \tag{9}$$

So, (6) is rewritten as (10):

$$V_{L_1} = V_{L_2} = V_L = L(1+K) \cdot I_L \cdot s \tag{10}$$

According to the equation above, we can replace two tank of each side by an equivalent tank, which is shown in Fig. 3, as below:

$$Z_{in(eq)} = \frac{\left(\frac{1}{C_{eq}}\right)s}{s^2 + \left(\frac{1}{R_{eq}C_{eq}}\right)s + \left(\frac{1}{L_{eq}C_{eq}}\right)} \tag{11}$$

where

$$C_{eq} = \frac{C}{2},\ R_{eq} = 2R,\ L_{eq} = 2L(1+K) \tag{12}$$

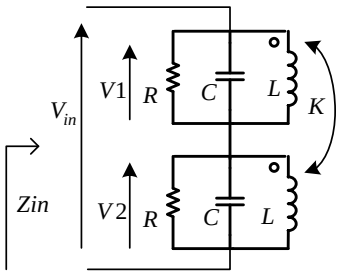


Fig. 2 Two series LC resonator for the first state.

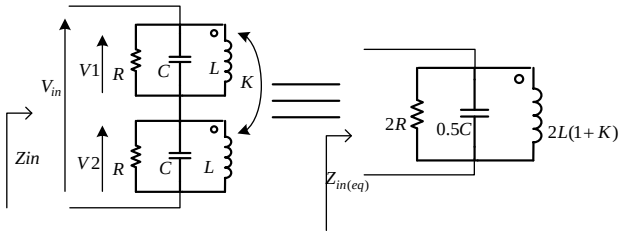


Fig. 3 An equivalent LC tank from two series LC resonator in the first state.

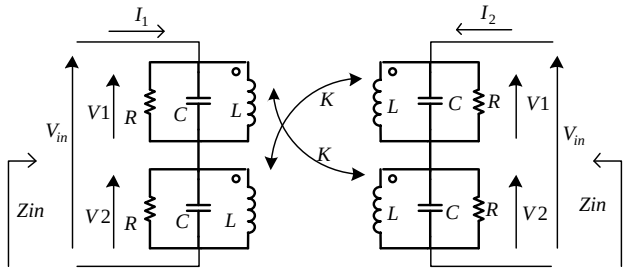


Fig. 4 Two series LC resonator for the second state.

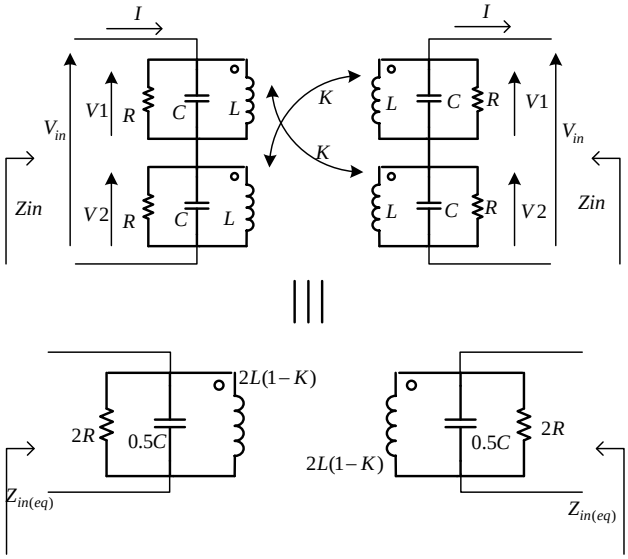


Fig. 5 An equivalent LC tank from two series LC resonator in the second state.

Table 1 Summaries the two states.

Switch states		R_{eq}	C_{eq}	L_{eq}	$\omega_{\circ(eq)}$	Q_{eq}
S1=on	S3=off	$2R$	$0.5C$	$2L(1+K)$	$\omega_{\circ 1(eq)}=1/\sqrt{C\cdot L(1+K)}$	$\frac{1}{\sqrt{(1+K)}}Q$
S2=on	S4=off					
S1=off	S3=on	$2R$	$0.5C$	$2L(1-K)$	$\omega_{\circ 2(eq)}=1/\sqrt{C\cdot L(1-K)}$	$\frac{1}{\sqrt{(1-K)}}Q$
S2=off	S4=on					

Analyzing the second state: S1 & S2: OFF, S3 & S4: ON. Fig 4 shows the mutual inductance in this state. Concerning the symmetry of the circuit in a steady oscillation, the currents of the two sides are differential that means $I_1= -I_2$. By considering this point and using similar calculations in the first state, we can find and an equivalent LC tank which is shown in Fig. 5.

As mentioned earlier, there are two key points in the proposed circuit. The first is that serializing two LC tanks increases the amplitude of the oscillation that leads to the reduction of the phase noise. The second one is the use of the mutual inductance between two tanks, which creates two distinct frequencies for the dual-band oscillator. In the following, these two points are detailed.

Based on the switching of the proposed structure, two oscillation frequencies along with the quality factor in two states can be obtained as follows:

$$Q_{eq1}=R_{eq}\sqrt{\frac{C_{eq}}{L_{eq}}}=2R\sqrt{\frac{0.5C}{2L(1+K)}}=R\sqrt{\frac{C}{L(1+K)}}$$
$$=\frac{1}{\sqrt{(1+K)}}Q,\quad Q_{eq1}<Q \tag{13}$$

$$Q_{eq2}=R_{eq}\sqrt{\frac{C_{eq}}{L_{eq}}}=2R\sqrt{\frac{0.5C}{2L(1-K)}}=R\sqrt{\frac{C}{L(1+K)}}$$
$$=\frac{1}{\sqrt{(1-K)}}Q,\quad Q_{eq2}>Q \tag{14}$$

Table 1 shows that the proposed circuit oscillates at a specific frequency in each switch state. Also, in both states, the equivalent parallel resistance of the LC tank has been doubled.

According to [17-20], the oscillation amplitude in the proposed oscillator (V_m) is:

$$V_m=\frac{2}{\pi}I_{bias}R_{eq} \tag{15}$$

where I_{bias} is the tail current. As (15) shows, the amplitude of the oscillation will be increased by growing the equivalent parallel resistance of the LC tank.

To explain the phase noise reduction in the proposed oscillator, we used a general expression of the phase noise equation, based on the Hajimiri theory [21, 22], as follows:

$$L\left(\Delta\omega\right)=10Log\left[\frac{4KT}{P_{RF}}\Gamma_{rms}^{2}\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right] \tag{16}$$

where P_{RF} is the output signal power that indeed is the power dissipation in the tank, Γ_{rms} denotes the root mean square of the impulse sensitivity function (ISF), Q is the effective quality factor of the LC oscillator, ω_o represents the resonance frequency of the LC tank, and $\Delta\omega$ is the offset frequency. Equation (16) shows that phase noise is reduced by increasing output signal

power. A designer can improve phase noise by increasing the power consumption (P_{DC}) whilst this method does not improve oscillator performance. Notice that increasing the power consumption (P_{DC}) increases the output signal power (P_{RF}) and, according to (16), reduces the phase noise. On the other hand, this goal can be achieved by increasing the output signal while power consumption is stable. As a result, in the proposed topology and on the basis of the above equation, phase noise will be reduced because of the increment of P_{RF}, which is the result of raised output amplitude.

Considering $P_{RF} = P_{DC}\,(P_{RF} / P_{DC}) = P_{DC}\,\eta$, where η is the power efficiency of oscillator [22, 23], the below equation shows that when consumption power is the same, the proposed design has more power efficiency in comparison to the single-band structure. Note the bellow equation.

$$\begin{cases} P_{RF\,(single\ band)} = \frac{1}{2}V_m.(\frac{2}{\pi}I_{bias}) = \frac{1}{2}R(\frac{2}{\pi}I_{bias})^2 \\ P_{RF\,(proposed)} = \frac{1}{2}V_m.(\frac{2}{\pi}I_{bias}) = \frac{1}{2}R_{eq}(\frac{2}{\pi}I_{bias})^2 \end{cases}$$
$$\Rightarrow P_{RF\,(proposed)} \gg P_{RF\,(single\ band)} \quad (17)$$

As the above equation shows, increasing the LC tank equivalent resistance in this work increases the output voltage amplitude and the output signal power while the current and power consumption are constant. As a result, the phase noise is reduced according to Equation (16). Also, due to the increase in the output voltage amplitude in a power consumption equal to the single-band structure, this oscillator can oscillate in less current. As a result, this structure will also be a low power structure.

Also, according to [22], this leads to the decrement of phase noise and power consumption in the proposed design.

3 Non-Ideal Effects of Switches on the Phase Noise

In multi-band oscillators, switches are usually implemented by MOS transistors, which adds parasitic inductors and capacitors that makes the oscillation frequency deviate from design values. Also, it has undesirable impacts on phase noise. That is why designers try to cancel these effects in multi-band oscillation. In the proposed circuit, serializing two LC tanks improves the oscillator's performance and somehow compensates for the unwanted impacts.

Fig. 6 shows the output impedance of the oscillator by considering capacitance and resistance effects of switches, which are shown as *Cp* and R_{SW}, respectively. The impedance of Fig. 6 can be obtained as below:

$$H(S) = \frac{Vo}{I_o} = \frac{a_1 \cdot S^2 + b_1 \cdot S + c_1}{a_2 \cdot S^3 + b_2 \cdot S^2 + c_2 \cdot S + d_2} \quad (18)$$

where $a_1 = R_{sw}\,R_{eq}\,L_{eq}\,C_{eq}$, $b_1 = (R_{sw} + R_{eq})\,L_{eq}$, $c_1 = R_{sw}\,R_{eq}$, $a_2 = R_{sw}\,R_{eq}\,L_{eq}\,C_{eq}\,C_p$, $c_2 = L_{eq} + R_{eq}\,R_{sw}\,C_p$, $b_2 = L_{eq}\,C_p\,(R_{sw} + R_{eq}) + R_{eq}\,L_{eq}\,C_{eq}$, and $d_2 = R_{eq}$. Non-ideal switch, shown in Fig. 6, cause the load impedance of drain to be different from a LC tank, so the oscillation condition should be re-studied assuming G_m and the closed loop transfer function as below.

$$\frac{V_{out}(S)}{V_{in}(S)} = \frac{(G_m \cdot H(S))^2}{1+(G_m \cdot H(S))^2} \quad (19)$$

As it does not worth directly analyze the above transfer function, we investigate the problem in another view. Based on Barak-Hausen's conditions, the proposed oscillator oscillates if the phase of the drain load will be zero, in addition to considering the condition for amplitude. In Fig. 7, the bode diagram of drain impedance is plotted based on the frequency. As it shows, increasing R_{SW}, decreases the oscillation frequency, and based on $Q = \frac{\omega_o}{2}(d\varphi/d\omega)$, the effective quality factor (Q) declines, too [24]. Since phase noise is inversely proportional to Q^2, switches with higher resistance will impair the phase noise performance.

The only way to reduce the switch resistance is to increase the size of the transistors which increases the parasitic capacitors of the switch and leads to the reduction of the tuning range of the VCO [10]. In this work, it is shown that however real switches upturn phase noise, increasing the amplitude by two series tank can tackle this problem.

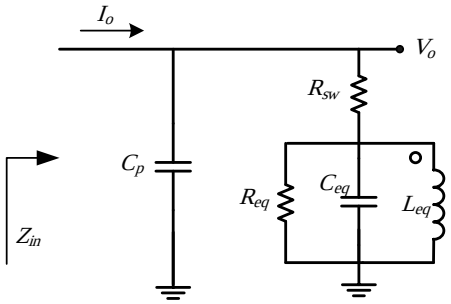


Fig. 6 An equivalent impedance with non-ideal effects switch.

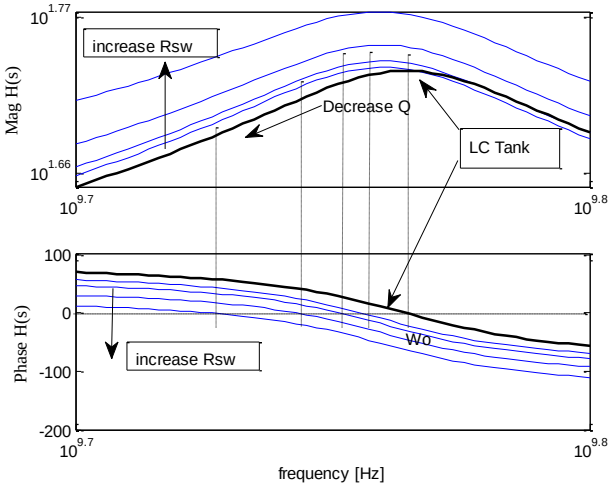


Fig. 7 Bod diagram of impedance LC tank with non-ideal effects switch for L = 1.5 nH, C = 0.5 pf, Q_{res} = 10 and R_{SW} between 10 to 80 ohm.

4- Simulation Results

To evaluate the proposed topology, a Local Oscillator (LO) [18] is simulated using TSMC, 0.18 µm CMOS technology. Also, it is designed for two frequencies of 3.6 GHz and 6.4 GHz, which its further information is detailed in Table 2. (K is the mutual induction coefficient of two inducers)

The output transient waveform of the circuit is shown in Fig. 8(a) and (b), for lower and upper frequency.

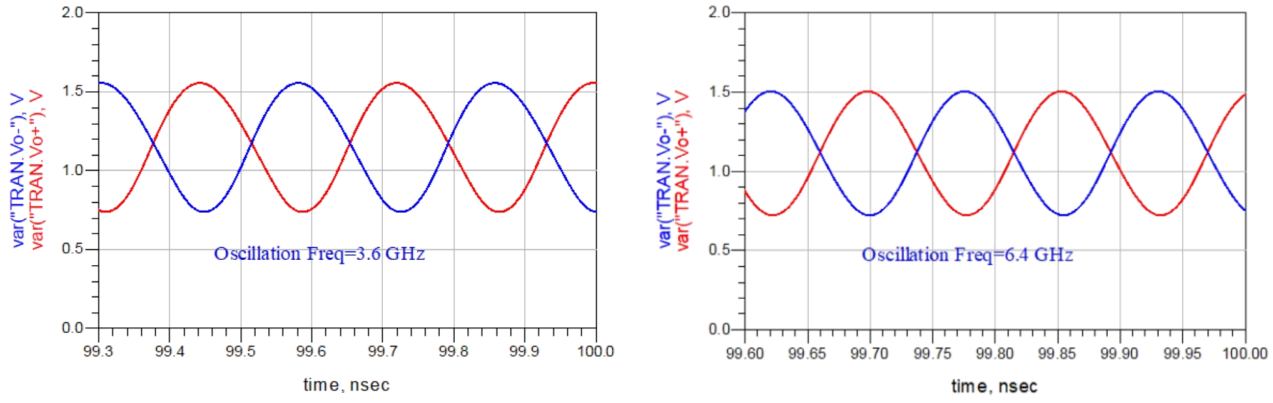
Fig. 9 depicts the phase noise spectrum for a single band oscillator and the proposed dual-band oscillator that oscillates at the lower and upper frequencies. It was assumed that switches used in this work are ideal. As can be seen in Fig. 10, using two series LC resonator degrade phase noise by about 5 to 7 dBc/Hz.

As mentioned in Section 3, switching transistors reduce the oscillator performance, especially in phase noise. In Fig. 10, the phase noise is plotted versus switches' widths. As it is shown, increasing the width of the switches decreases the R_{SW} and consequently the phase noise. Moreover, according to $Q = R_p \cdot \sqrt{C_{eq}/L_{eq}}$ [18], increasing the transistor's size will increase C_{eq}, which leads to the increment of Q and decrement of phase noise.

In order to confirm the IC implementation, simulation of the corner with temperature verification are done to make sure that the proposed design works in those situations. The corner analysis results are shown in Table 3. Also, a Monte Carlo simulation with 100 times iteration is performed. Fig. 11 shows phase noise curves using Monte Carlo simulation that indicate the high productivity of the proposed design.

Table 2 Details of simulation parameters.

VDD [V]	*L* [nH]	*C* [pF]	*K*	$(W/L)_{tran}$ [µm/µm]	Tail current [mA]	*Q*	Power [mW]
1.5	1.1	0.8	0.5	(20/0.18)	1	12	1.5



(a) (b)

Fig. 8 Output transient wave form of the circuit a) in lower frequency and b) in upper frequency.

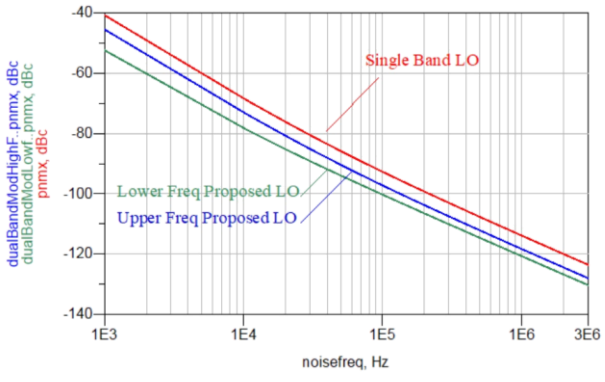


Fig. 9 The curve of phase noise and compression single band QO and proposed dual band QO.

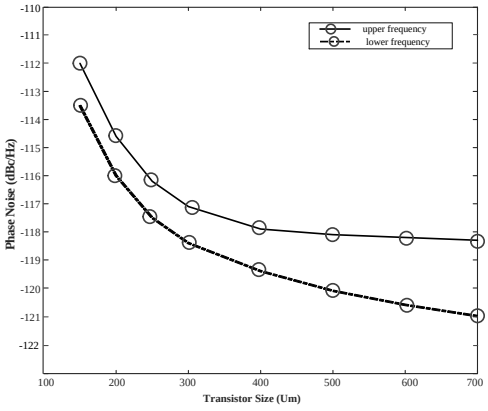
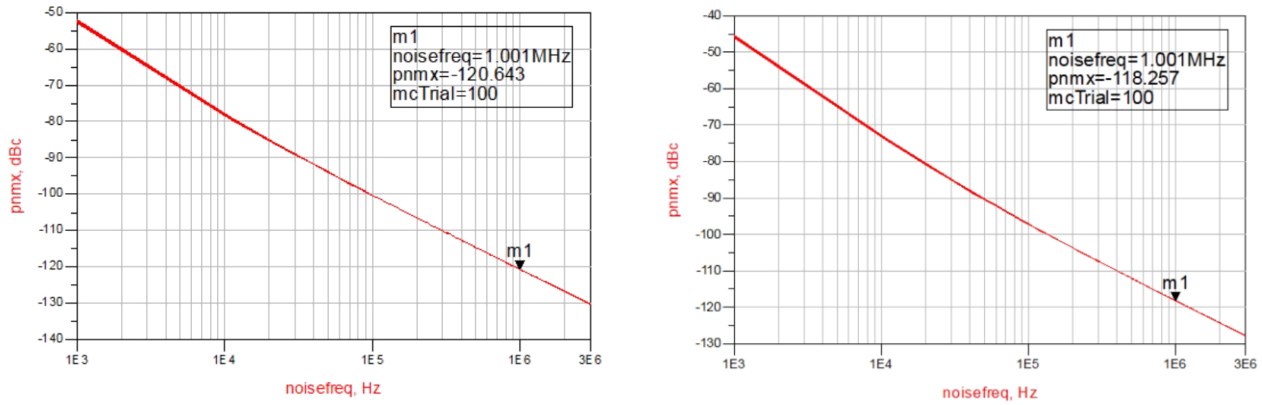


Fig. 10 Phase noise versus transistor size.

Table 3 The corner analysis results on phase noise.

Process corners	FF (@-40ºC)	SS (@85ºC)	TT (@27ºC)
Phase Noise [dBc/Hz] @ 1MHz offset in 6.4 GHz	-118.9	-115.6	-118.2
Phase Noise [dBc/Hz] @ 1MHz offset in 3.6 GHz	-121.6	-118.4	-120.6



(a) (b)

Fig. 11 The phase noise curve using Monte Carlo simulation a) in lower frequency and b) in upper frequency.

Table 4 Comparison of the performance of this work against others.

Ref.	Freq. [GHz]	Tech. [nm]	PN [dBc/Hz] @1MHz	P_{DC} [mW]	FOM [dBc/Hz]
[1]	62.25	65	-107.2/-116.3 (@10MHz)	7.4/11.2	172.6/183.5
[2]	3.52/5.28	180	-109.0/-123.2	4.8/5.7	177.3/188.3
[3]	40/80	65	-94/-81	42	170/163
[9]	2.4/5.0	180	-134/-125	4.6/6	195/192
[12]	1.85/2.66	180	-120.8/-121.7	5.37/6.8	172.5/177.2
[25]	24/60	130	-120/-114 (@10MHz)	24/11	177/176
[26]	2.7/5.4	130	-118.8/-109.5	5.4	182/177
This Work	**3.6/6.4**	**180**	**-118.2/-120.6**	**1.5**	**189.9/192.5**

The simulation results are summarized in Table 4 and compared against the other state-of-the-art duad band oscillators.

5 Conclusions

This paper presents a low noise low power dual-band oscillator. The main idea of the proposed design is to use two serried LC tank on each side of the cross-coupled transistor. By changing the mutual inductions of the two inductors, the oscillation amplitude is increased that leads to the reduction of phase noise. What is more, the parasitic elements of real switches increases phase noise that the proposed technique can compensate it. Another advantage of this work is that it can reduce current consumption due to increasing amplitude while the oscillator is in steady states. Finally, many simulations are done in TSMC 0.18 Um that all of them confirm the high capability of the proposed method and high accuracy of the results obtained from the theory sections.

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