IUST
Iran University of Science and Technology

Iranian Journal of Electrical and Electronic Engineering

Journal Homepage: ijeee.iust.ac.ir

Research Paper

A Two-Stage Grid-Connected Single-Phase SEPIC-based Micro-Inverter with High Efficiency and Long Lifetime for Photovoltaic Systems Application

S. Saeedinia*, M. A. Shamsi-Nejad*(C.A.), and H. Eliasi*

Abstract: This paper proposes a grid-connected single-phase micro-inverter (MI) with a rated power of 300 W and an appropriate control strategy for photovoltaic (PV) systems. The proposed MI is designed based on a two-stage topology. The first stage consists of a SEPIC DC-DC converter with high voltage gain to step up the voltage of the PV panel and harness the maximum power, while the second stage includes a full-bridge DC-AC converter. The advantages of the proposed MI are the use of fewer components to provide suitable output voltage level for connection to a single-phase grid, continuous input current, limited voltage stress on the switch, high efficiency, long operational lifetime, and high reliability. Lower input current ripple and the presence of film capacitors in the power decoupling circuit increase the lifetime and reliability of the proposed MI. In the proposed MI, the active power decoupling circuit, which is normally used in a typical single-stage SEPIC-based MI, is eliminated to achieve both a long lifetime and high efficiency. The operating principles of the proposed MI are analyzed under different conditions. The results of design and simulation confirm the advantages and proper performance of the proposed MI.

Keywords: Film Capacitor, Grid-Connected Micro-Inverter, High Efficiency, Long Lifetime, PV System.

1 Introduction

SOLAR energy systems are promising renewable energy sources due to their ability to generate electricity from sunlight in a completely clean and reliable way [1]. Renewable energy sources such as photovoltaic (PV) systems have attracted more attention in recent years. In general, the configuration of solar inverters in grid-connected PV systems are categorized into three common groups based on their location concerning solar modules, as follows: a) centralized inverter topologies, b) string topologies, and c) PV-module-integrated AC inverters also known as micro-inverters [2].

In the past, a central inverter was generally used in PV systems to cover all modules; this technique was cost-effective. However, this type of system had a serious drawback, which could drastically degrade the performance of all solar modules as well as cause other problems when the solar modules were operated under shading conditions [3]. The inverter that is used in an AC module is called a micro-inverter (MI) because it is usually a low-power inverter .MIs are usually placed behind PV modules and their typical power is in the range of 100-300 W [4]. Compared to centralized and string PV systems, PV-module-integrated AC inverters have gained more attention due to their advantages, such as receiving maximum power from the solar panel, higher safety compared to other topologies, easy development, operating independently of the modules, and low cost in large volume production [4-7]. MIs have many advantages, while there are still many challenges that must be addressed. These challenges correspond to

Iranian Journal of Electrical and Electronic Engineering, 2022.
Paper first received 23 November 2021, revised 23 January 2022, and accepted 29 January 2022.
* The authors are with the Faculty of Electrical Engineering and Computer, University of Birjand, Birjand, South of Khorasan, Iran.
E-mails: saeedsaeedinia@birjand.ac.ir, mshamsi@birjand.ac.ir, and h_eliasi@birjand.ac.ir.
Corresponding Author: M. A.Shamsi-Nejad.
https://doi.org/10.22068/IJEEE.18.2.2355

1) achieving high efficiency, 2) improving system lifetime and reliability, 3) providing adequate output voltage level for grid-connected operation, 4) the number of the used switches, and 5) the quality of power injected into the grid [2, 5, 8].

Therefore, the disadvantage of MIs compared to centralized PV systems is low efficiency, which reduces the competitiveness of AC modules. Thus, improving the efficiency of MIs is an important research area [9]. The operational lifetime of PV panels is typically about 25 years. Hence, another important challenge facing MIs is to meet the operational lifetime of PV panels. The input-side power generated by a PV panel is constant in steady-state. However, grid-side power is determined by the grid current and voltage, which have very large instantaneous oscillation amplitudes. Therefore, there is a power difference between the DC input-side and AC grid-side in an MI. To balance this power difference, a capacitor has to be used, but an electrolytic capacitor reduces the lifetime of the MI [10]. A high-capacity electrolytic capacitor is usually used as a power decoupling element in parallel with the PV panel to control the power ripple between the input and output terminals of a single-phase system. However, electrolytic capacitors are temperature-sensitive and cannot meet the reliability and lifetime requirements of grid-connected MIs. The lifetime of electrolytic capacitors is typically in the range of 1000-7000 hours at an operating temperature of 105 °C [11]. Although a film capacitor has a smaller capacitance than an electrolytic capacitor with the same dimensions, it has a longer lifetime Therefore, to increase the reliability and lifetime of MIs, film capacitors should be replaced by electrolytic ones [2]. The topologies of MIs are divided into two categories of single-stage and two-stage [4]. In single-stage topologies, power is decoupled using electrolytic capacitors in parallel with the PV panel [12, 13] or active power decoupling circuits (APDCs) [2], [14-16]. In MIs, additional APDCs are employed to enable the use of film capacitors, and consequently, to increase the lifetime and reliability of MIs. However, APDCs increase the cost, complexity, and power losses as well as reduce the efficiency of MIs [4]. In [12], a single-stage grid-connected MI with a rated power of 100 W is presented for PV systems. The proposed MI has some desirable specifications, such as low switching loss, high voltage gain, and fewer switches, which make it suitable for PV systems. The efficiency of the proposed MI is 93.6% at rated power, but the presence of a 4000-µF electrolytic capacitor in parallel with the PV panel leads to a shorter lifetime and less reliability. Reference [13] proposes a zeta converter with a rated power of 220 W. The most distinctive feature of the MI proposed in this reference is that it can operate in continuous conduction mode (CCM) in a wide load range, which leads to 93% efficiency at rated power and low current stress. However, the disadvantage of this converter is the use of 18800-µF electrolytic capacitors for power decoupling, which reduces the MI lifetime. In [14], a flyback topology with an APDC and a rated power of 100 W is used to increase MI lifetime by replacing the electrolytic capacitors with film capacitors. However, the efficiency of this design is 89% at rated power. A three-port single-stage converter with a rated power of 100 W is introduced in [15] to connect PV panels to a single-phase power system. To control the input-output power difference, an APDC is used in the MI. Moreover, high-capacity electrolytic capacitors, which limit system reliability, are replaced by thin-film capacitors with limited capacity and long lifetime. However, the efficiency reaches 88.9% at rated power. A single-stage MI with high MPPT efficiency and a rated power of 240 W is proposed in [16]. In this reference, an APDC is employed to enable the use of long lifetime film capacitors, but the efficiency of the proposed MI is less than 90%. In [2], a single-stage MI with a rated power of 100 W is introduced based on a single-ended primary inductance converter (SEPIC) with an APDC. The MI introduced in this reference has better reliability and a longer lifetime due to using film capacitors instead of electrolytic capacitors, while its efficiency is 90% at rated power. APDCs allow using film capacitors to increase the lifetime, while the efficiency is not high. Hence, APDC should be eliminated to achieve high efficiency along with a long lifetime. Accordingly, in the present study, the single-stage topology in [2] is converted into a two-stage topology. The purpose of this paper is to present a high-efficiency grid-connected MI with a few switches and components. The proposed MI uses a suitable control strategy, long-lifetime high-reliability film capacitors for power decoupling without needing an additional APDC, high efficiency, and continuous input current as well as imposing low voltage stress on switches. The remainder of this paper is structured as follows. The configuration and operating principles of the proposed MI are presented in Section 2. The design details of the MI components are expressed in Section 3. The efficiency and losses of the proposed MI are analyzed, and the control system is introduced in Sections 4 and 5, respectively. The simulation results and concluding remarks are presented in Sections 6 and 7, respectively.

2 Proposed MI Topology

In the present study, the design of the proposed MI is based on a two-stage topology with a rated power of 300 W. Two-stage topologies are very commonly used in grid-connected MIs for industrial applications. The output capacitor of the DC/DC converter balances the power difference between the DC input-side and AC grid-side to mitigate voltage fluctuations. Moreover, this capacitor acts as a passive power decoupling element in the DC-link. The overall structure of the proposed MI is shown in Fig. 1.

By eliminating APDC and using a two-stage topology to achieve high efficiency, a SEPIC DC-DC converter with high voltage gain and high efficiency should be designed for the first stage of the MI. Then, a low-capacity film capacitor is installed at the DC-link to decouple power without requiring any additional circuit. The film capacitor can increase the lifetime of the MI. Furthermore, a single-phase full-bridge DC-AC converter with an LC filter is used in the second stage to realize a single-phase grid-connected PV MI. In two-stage MIs, voltage increasing by series connection of PV panels has limitations due to shading power losses. Therefore, DC-DC converters with high voltage gain should be used at the output terminal of the panels to boost the input voltage of the panels into the required voltage (200-400 V), which is necessary for the DC-AC converter in the second stage [17]. Hence, a high voltage gain SEPIC DC-DC converter has to be designed. If a conventional DC-DC boost converter is used for an MI, it must have a very high duty ratio. This issue leads to large peak currents, conduction losses, switching losses of electric power components in the converter, and reduction in efficiency [3]. Therefore, a conventional boost converter cannot be used to achieve the output voltage required for the DC-link and the inverter input, and this is an important challenge for the efficiency of two-stage MIs. The two-stage topology of MI requires more active and passive components, leading to a reduction in performance, and an increase in volume and weight [8]. Therefore, to increase the efficiency, fewer components have to be used in the MI design along with a high voltage gain SEPIC DC-DC converter at a minimum duty ratio. Moreover, it is essential to limit the voltage stress on the switch of the SEPIC DC-DC converter to increase the efficiency of the proposed two-stage MI. High voltage gain should be achieved with limited voltage stress on the switch. Therefore, a low-voltage MOSFET with a small on-state resistance $R_{ds(on)}$ is used as the main switch to reduce both switching and conduction losses [18]. To increase the lifetime of MIs, their input current ripple must be continuous besides using film capacitors for power decoupling. The high input current ripple significantly reduces the MI lifetime [19]. Moreover, a continuous input current facilitates the maximum power point tracking (MPPT) in PV panels [20]. The first stage of the proposed MI includes a SEPIC DC-DC converter [18], which provides a proper voltage gain for the MI by using a coupled inductor with a well-adjusted turns ratio and a limited number of components. Voltage gain increases by adjusting the turns ratio of the coupled inductor at a low duty ratio, and there is no overvoltage on the switch during the turn-off process. Hence, a low-voltage MOSFET with low $R_{ds(on)}$ can be used as the switching element, while there is no need for an additional clamp circuit, which reduces the efficiency of the converter. The proposed MI has a long lifetime due to the power decoupling film capacitors and continuous input current ripple.

2.1 Operating Principles and Steady-State Analysis of MI

This section describes the operating principles of the proposed MI and its steady-state analysis. Fig. 2 shows the proposed SEPIC-based MI. The first stage of this MI includes a SEPIC DC-DC converter with a coupled inductor structure and a small number of components at a rated power of 300 W.

According to Fig. 2, the SEPIC-based MI topology consists of five switches S_1–S_5, two diodes (D_1 and D_2), three capacitors C_{in}, C_1, and C_{dc}, as well as a coupled inductor and an LC output filter. The MI can operate in continuous conduction mode (CCM). A capacitor is connected in series with the secondary winding to prevent the flow of DC current, and thus, the saturation caused by the DC current. To further analyze the operation of the MI, the following assumptions are made: 1) switches and diodes of the MI are ideal, so $R_{ds(on)}$ of the switches and voltage drop across the diodes are negligible, 2) all capacitors are large enough, so the voltage ripple in them is small, and 3) the leakage inductance of the coupled inductor is negligible. Moreover, the coupled inductor, which is in parallel with the primary winding, is considered as an ideal transformer with the turns ratio $a = N1{:}N2$ and magnetizing inductance L_m.

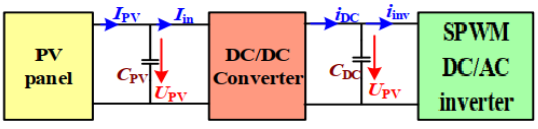

Fig. 1 Overall structure of the proposed MI.

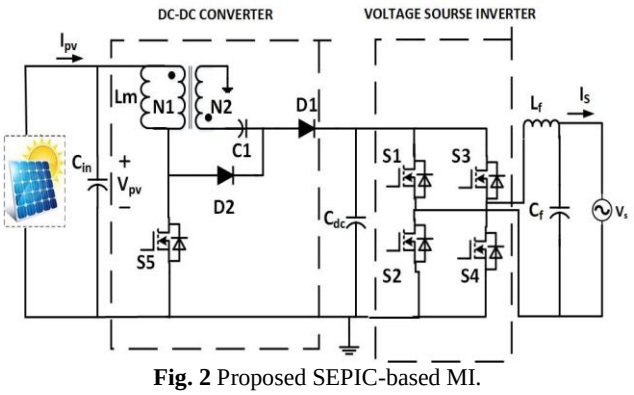

Fig. 2 Proposed SEPIC-based MI.

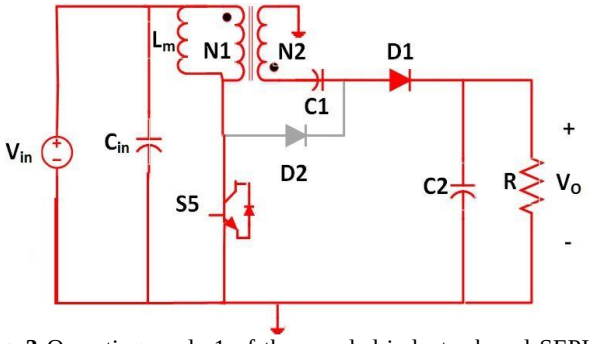

Fig. 3 Operating mode 1 of the coupled-inductor-based SEPIC DC-DC converter.

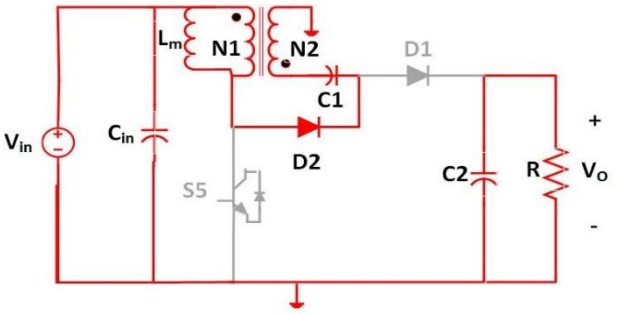

Fig. 4 Operating mode 2 of the coupled-inductor-based SEPIC DC-DC converter.

These assumptions are used in the following to discuss the operating principles of the first stage of the proposed MI. Each switching cycle of the DC-DC converter is divided into two operating modes as shown in Figs. 3 and 4.

In operating mode 1 (Fig. 3) switch S_5 is turned on, and the voltage across L_m is equal to the input voltage. Moreover, in this mode, D_1 is on, D_2 is off, and C_1 supplies energy to the load, which is connected to the output capacitor C_2. Therefore,

$$V_{Lm}\left(\text{mode}_1\right) = V_{in} = VN_1 \tag{1}$$

By applying Kirchhoff's voltage law (KVL) to the secondary winding, one obtains.

$$V_o = VC_1 + nV_{in}; \qquad n = \frac{N2}{N1} \tag{2}$$

In operating mode 2, S_5 is turned off, so D_2 is on and provides a path for the magnetizing current. During operation mode 2, D_1 is off and the output capacitor C_2 supplies the required energy to the load. The KVL based on Fig. 4 gives the voltage across L_m as follows:

$$-\mathrm{nV_{Lm}} - \mathrm{VC_1} - \mathrm{V_{Lm}} + \mathrm{V_{in}} = 0$$

$$\Rightarrow \mathrm{V_{Lm}}\left(\mathrm{mode_2}\right) = \frac{\mathrm{V_{in}} - \mathrm{VC_1}}{1+\mathrm{n}} \tag{3}$$

According to the voltage balance of L_m, the voltage of capacitor C_1 can be calculated as follows:

$$VC_1 = \frac{(1+nD)}{1-D}.V_{in} \tag{4}$$

By inserting (4) into (2), the output voltage can be obtained as follows:

$$V_o = \frac{1+n}{1-D}.V_{in} \tag{5}$$

Using (5), the voltage gain of the first stage of MI is given by:

$$G = \frac{V_o}{V_{in}} = \frac{1+n}{1-D} \tag{6}$$

Therefore, the output voltage is a function of the turns ratio (n) and the duty cycle (D). By applying KVL, as shown in Fig. 4, the voltage stress on S_5 is given by:

$$V_{s5} = V_{in} - V_{Lm} \tag{7}$$

By inserting (3) into (7), one obtains

$$V_{S_5} = \frac{V_{in}}{1-D} = \frac{V_o}{1+n} \tag{8}$$

Comparing (5) and (8) show that the voltage stress on switch S_5 is always less than the output voltage for each n. Similarly, the voltage across the diodes can be calculated using the following equations.

$$V_{D1(\text{mode}\,2)} = \frac{n}{1-D}.V_{in} \tag{9}$$

$$V_{D1(\text{mode}1)} = 0 \tag{10}$$

$$V_{D2(\text{mode}1)} = V_O = \frac{1+n}{1-D}.V_{in} \tag{11}$$

$$V_{D2(\text{mode}\,2)} = 0 \tag{12}$$

The maximum currents through diodes D_1 and D_2 can be determined by (13) and (14).

$$I_{D_1} = \frac{I_o}{D} \tag{13}$$

$$I_{D_2} = \frac{I_o}{1-D} \tag{14}$$

By applying KCL to Fig. 3, the current of S_5 is obtained as follows:

$$I_{S_5} = I_{Lm} - IN_1 \tag{15}$$

Since the average primary and secondary side currents of the coupled inductor are zero, the average current of S_5 is equal to:

$$\overline{I_{S_5}} = \overline{I_{in}} - n\,I_o \Rightarrow \overline{I_{S_5}} = \frac{1+Dn}{1-D}.I_o \tag{16}$$

Moreover, the maximum current through switch S_5 can be calculated using (17):

$$I_{S_{5\max}} = \frac{1+Dn}{D.(1-D)}.I_o \quad (17)$$

3 Calculating Design Parameters of MI

The main design equations of the proposed MI are presented in this section. These equations are validated using the simulation results in Section 6.

First, the parameter values of the proposed MI are determined using the following considerations:

1) The input voltage varies between 20 and 40 V at a rated value of 30 V.
2) Assuming a voltage gain of 10 and a rated power of 300 W for the MI, the output voltage of the DC-DC converter is fixed at 300 V.
3) The switching frequency of the DC-DC converter is 100 kHz.
4) The MI operates in CCM.
5) The voltage stress on the switch has to be less than the allowable voltage for the corresponding switch.
6) The voltage ripple across capacitors has to be 1% less than their voltage rating.

3.1 Coupled-Inductor Turns Ratio

In (18), the coupled-inductor turns ratio is given as follows:

$$n = \frac{V_o - V_{s5}}{V_{s5}} \quad (18)$$

According to (18), to achieve a voltage stress of 60 volts across switch S_5, the turns ratio (n) has to be equal to or greater than 4. Therefore, $n = 4$ is considered.

The minimum magnetizing inductance for the MI in CCM operation can be calculated as follows:

$$L_m \geq \frac{D.(1-D)^2.V_o}{2.f_S.I_o.(1+n)^2} \quad (19)$$

To achieve proper performance in CCM operation at the half output load and maximum input voltage, the minimum magnetizing inductance has to be equal to 17.77 µH according to (19).

3.2 Duty Ratio Selection

Using (20), the duty ratio of MI is calculated as follows:

$$D = 1 - \frac{(1+n).V_{in}}{V_o} \quad (20)$$

The minimum and maximum values of the duty cycle can be determined in (21) and (22) by using (20).

$$D_{\min} = 1 - \frac{(1+n).V_{in\max}}{V_o} = 1 - \frac{5\times 40}{300} = 0.33 \quad (21)$$

$$D_{\max} = 1 - \frac{(1+n).V_{in\min}}{V_o} = 1 - \frac{5\times 20}{300} = 0.667 \quad (22)$$

Moreover, the value of the rated duty cycle (D) is equal to 0.5.

3.3 Selecting Switches and Diodes

The maximum voltages across diodes D_1 and D_2 are given according to (23) and (24).

$$V_{D1} = \frac{n}{1-D}.V_{in} = \frac{4}{0.5}.30 = 240 \text{ V} \quad (23)$$

$$V_{D2} = V_{dc} = 300\,\text{V} \quad (24)$$

Based on (25) and (26), the maximum current of diodes D_1 and D_2 are as follows:

$$I_{D1\max} = \frac{I_o}{D_{\min}} = 3.03\,\text{A} \quad (25)$$

$$I_{D2\max} = \frac{I_o}{1-D_{\max}} = 3\,\text{A} \quad (26)$$

Therefore, the part number of power diodes D_1 and D_2 is C3D03060E with a DC blocking voltage of 600 V and a continuous forward current of 11 A.

The maximum current of S_5 can be obtained using (27):

$$I_{s5\max} = \frac{1+D_{\max}.n}{D_{\max}.(1-D_{\max})}.I_o = 16.5 \text{ A} \quad (27)$$

The maximum voltage across S_5 (main switch of the MI) can be obtained using (28):

$$V_{S_5} = \frac{V_o}{1+n} = \frac{300}{1+4} = 60 \quad (28)$$

Therefore, a power MOSFET FDMS86180 with V_{DS} = 100 V and I_D = 151 A is selected.

Moreover, the maximum voltages across S_1–S_4 are equal to the DC link voltage. Therefore, a power MOSFET IXFX55N50 with V_{DS} =500 V and I_D = 50 A is selected.

3.4 Selecting Capacitors

After calculating the voltage across C_1 from (4), the minimum capacitance of C_1 can be determined by (29), assuming a voltage ripple of 1%.

$$C_{1(\min)} \geq \frac{I_o}{f_S.\Delta V_{Cdc}} = \frac{1}{100000.1.8} = 5.55\ \mu\text{F} \quad (29)$$

The capacitance of the DC-link capacitor in the MI can be obtained as follows:

$$C_{dc} = \frac{P_{\text{rms}}}{\omega.V_{dc}.\Delta V_{dc}} \quad (30)$$

where P_{rms} is the output power value, V_{dc} is the DC-link

average voltage, ΔV_{dc} is the voltage ripple of the DC-link, and ω is the angular frequency of the grid. After inserting the values, three parallel 100 µF film capacitors in the DC-link are determined.

3.5 LC Filter Design

To connect the proposed MI to a single-phase grid, a second-order passive LC filter was used to suppress harmonics. The first step in designing the LC filter is to calculate the base impedance values Z_b and the base capacitance C_b as follows:

$$Z_b = \frac{V^2_{g,\text{rms}}}{P_n} \tag{31}$$

$$C_b = \frac{1}{Z_b.\omega_g} = \frac{1}{Z_b.2\pi.f_g} = \frac{P_n}{V^2_{g,\text{rms}}.2\pi.f_g} \tag{32}$$

The second step corresponds to calculating the capacitance and inductance of the filter given by (33) and (34).

$$C_f = 0.05.C_b = \frac{0.05.P_n}{V^2_{g,\text{rms}}.\omega_g} \tag{33}$$

$$L_f = \frac{V_{dc}}{8.f_{sw}.\Delta i_{L,\text{peak}}} \tag{34}$$

where $\Delta i_{L,\text{peak}}$ is the inductor current ripple ranging from 10% to 20% of the output current($I_{g,\text{peak}}$). The value of $I_{g,\text{peak}}$ can be calculated from (35).

$$I_{g,\text{peak}} = \frac{\sqrt{2}.P_n}{V_{g,\text{rms}}} \tag{35}$$

The cut-off frequency (f_c) of the low-pass filter is chosen so that the output THD is less than 5%. The value of f_c is maintained at less than one-half of the inverter switching frequency. Then, after designing the filter, in the third step, the resonant frequency can be calculated to ensure that the third constraint on filter design is met [21, 22]. Consequently, the resonant frequency can be calculated from (36).

$$10\omega_g \le \omega_f = \frac{1}{\sqrt{L_f.C_f}} \le \frac{\omega_{sw}}{2} \tag{36}$$

Finally, the values of inductance and capacitance of the filter were selected as L_f = 5 mH and C_f = 2 µF.

4 Analyzing Power Loss and Efficiency of MI

The proposed MI with parasitic elements and internal resistance of the components is shown in Fig. 5. The resistances of the primary and secondary windings of the coupled inductors are denoted by r_{N1} and r_{N2}, respectively; r_{D2} and r_{D1} are the internal resistances; V_{FD1} and V_{FD2} denote the forward voltage of the diodes.

The equivalent series resistance (ESR) of the capacitor and inductor of the filter are r_{cf} and r_{Lf}; the input capacitor and DC link capacitor are denoted by r_{cin} and r_{cdc}, respectively. The ON-state resistance of MOSFET switches is represented by r_{s1}-r_{s5}.

The efficiency of the proposed MI can be calculated as follows:

$$\eta = \frac{\overline{P_{pv}} - P_{loss}}{\overline{P_{pv}}} \tag{37}$$

The total power loss and power efficiency of the proposed MI can be calculated as follows:

$$P_{loss} = \sum\left(P^S_{loss} + P^D_{loss} + P^C_{loss} + P^L_{loss}\right) \tag{38}$$

where P^S_{loss}, P^D_{loss}, P^C_{loss}, and P^L_{loss} denote the power losses of switches, diodes, capacitors, and inductors, respectively. Power losses of switches include switching and conduction losses. Switching losses can be calculated by (39) according to [23] and [24].

$$P^{S,switching}_{loss} = \frac{1}{2}V_{ds}I_{ds}f_{sw}\left(t_r + t_f\right) \tag{39}$$

where V_{ds} is the drain-source voltage of the switch, I_{ds} is current, f_s is the switching frequency, and t_r and t_f can be calculated using the switch datasheet. Considering the on-state resistance, $R_{ds(on)}$, the conduction losses of the switches can be calculated as follows:

$$P^{S,conduction}_{loss} = R_{ds(on)}.I^2_{ds,rms} \tag{40}$$

Consequently, the total losses of the switches (P^S_{loss}) can be obtained as follows:

$$P^S_{loss} = P^{S,switching}_{loss} + P^{S,conduction}_{loss} \tag{41}$$

Power losses of diodes are calculated as follows:

$$P^D_{loss} = R_D.I^2_{D(\text{rms})} + V_f.I_{D(\text{avg})} \tag{42}$$

where $I_{D(\text{avg})}$, V_f, $I_{D(\text{rms})}$, and R_D are, respectively, the average current, forward voltage drop, effective current, and resistance of the diodes. The conduction losses of capacitors and inductors can be calculated using the equivalent series resistance and effective current as follows:

$$P^C_{loss} = r_c.I^2_{C(\text{rms})} \tag{43}$$

$$P^{L,ohmi}_{loss} = r_L.I^2_{L(\text{rms})} \tag{44}$$

5 Proposed Control System of MI

The control system of the proposed grid-connected single-phase MI is based on the P-Q theory as shown in

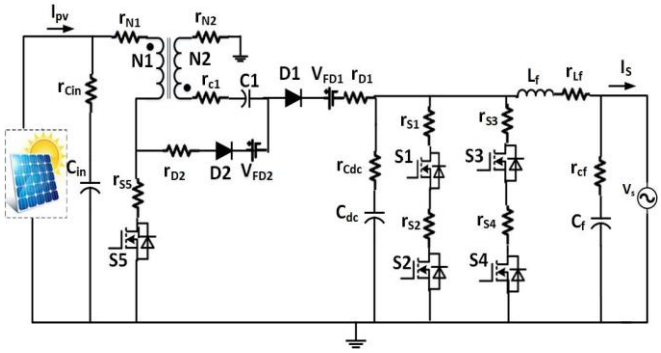

Fig. 5 Proposed MI with parasitic elements and internal resistance of components. ($R_{ds5(on)}$ = 3.2 mΩ, $R_{ds1\text{-}4(on)}$ = 80 mΩ, $V_{FD1,2}$ = 1.5 V, $r_{D1,2}$ = 20 mΩ, r_C = 15 mΩ, r_L = 15 mΩ, r_{N1} = 24 mΩ, r_{N2} = 96 mΩ).

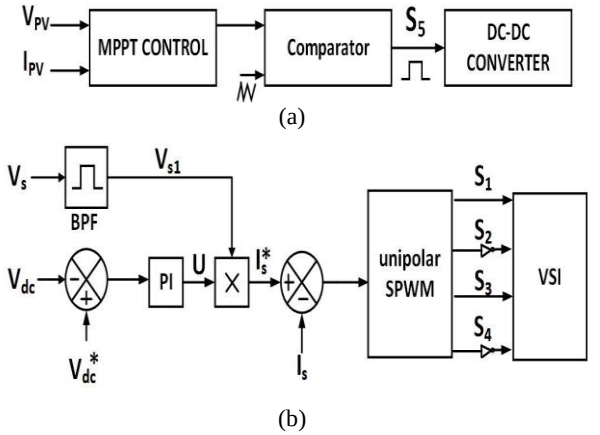

Fig. 6 Control system of the proposed MI; a) MPPT control of MI and b) voltage and current control of MI.

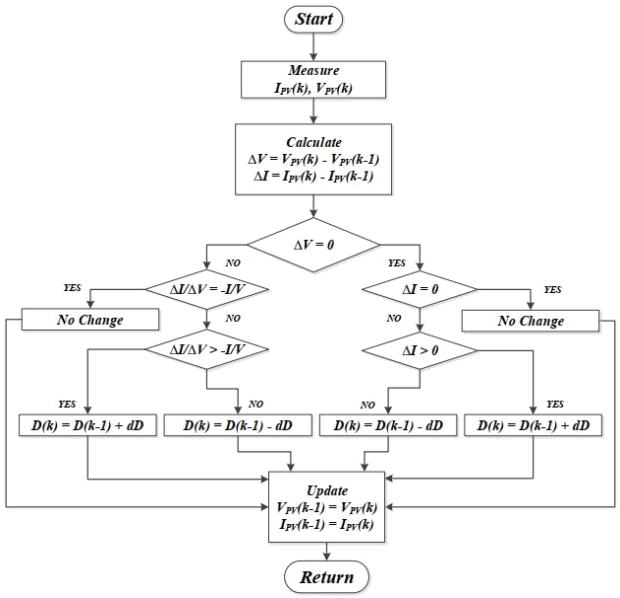

Fig. 7 INC algorithm based on switch duty ratio [25].

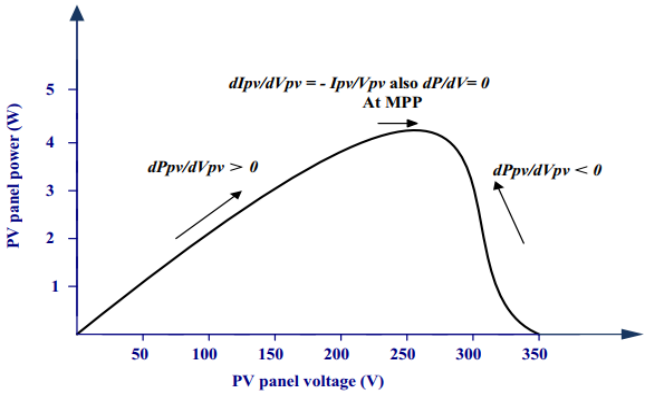

Fig. 8 P-V characteristic of PV panel.

Fig. 6. The control system consists of two parts. Part (a) includes an MPPT control system of the proposed MI to extract maximum power from the PV panel. Part (b) includes the voltage and current control system of the proposed MI with the following purposes. DC-link voltage stabilization, low-THD sinusoidal current injection into the grid, and unity-power-factor control for active power injection into the grid.

5.1 DC-DC Converter Control

The aim of the DC-DC converter control system is to maximize the power production from the solar panel connected to the proposed MI. The incremental conductance (INC) algorithm is used to track the maximum power point, as shown in Fig. 7 [25].

The DC-DC converter control system is based on the duty ratio of the converter switch. The duty ratio of S_5 is adjusted directly by the control system. The output power of the PV panel can be calculated as follows:

$$p_{pv} = V_{pv}.I_{pv} \tag{45}$$

Moreover, according to the concept of incremental conductance:

$$\frac{dP_{pv}}{dV_{pv}} = \frac{d\left(I_{pv}.V_{pv}\right)}{dV_{pv}} = \frac{V_{pv}.dI_{pv}}{dV_{pv}} + I_{pv} \tag{46}$$

This equation is the basis of the INC algorithm shown on the (P-V) curve in Fig. 8.

In this algorithm, the present and previous values of voltage and current of the PV panel are used to calculate the values of dP_{pv} and dV_{pv}. According to this algorithm, if dP_{pv}/dV_{pv} = 0, the MPPT algorithm operates at maximum power point (MPP). If dP_{pv}/dV_{pv} > 0, then the operating point of the PV array is at the left of MPP on

the P-V curve (Fig. 8). Therefore, S_5 must be increased to track MPP as shown in Fig. 7.

$$\frac{dP_{pv}}{dV_{pv}} > 0 \Rightarrow \frac{V_{pv}.dI_{pv}}{dV_{pv}} + I_{pv} > 0 \Rightarrow \frac{dI_{pv}}{dV_{pv}} > -\frac{I_{pv}}{V_{pv}} \quad (47)$$

Similarly, if $dP_{pv}/dV_{pv} < 0$, the operating point of the PV array is at the right of MPP on the P-V curve, as shown in Fig. (8). Therefore, the duty ratio of S_5 must be reduced to track the MPP as shown in Fig. 7.

$$\frac{dP_{pv}}{dV_{pv}} < 0 \Rightarrow \frac{V_{pv}.dI_{pv}}{dV_{pv}} + I_{pv} < 0 \Rightarrow \frac{dI_{pv}}{dV_{pv}} < -\frac{I_{pv}}{V_{pv}} \quad (48)$$

5.2 DC-AC Converter Control

The aim of the voltage and current control system of the proposed MI is to stabilize the DC-link voltage, inject low THD sinusoidal current into the grid, and control the active power injected into the grid at the unity power factor. The output of the bandpass filter (BPF) is the fundamental voltage component of the source at 50 Hz. The reference DC-link voltage is compared to the actual DC-link voltage and a proportional-integral (PI) controller with coefficients K_p = 0.09 and K_i = 1.8 is used to adjust the DC-link voltage at 300 V. The output of the PI controller can be calculated using (49).

$$U = K_p.\left(V_{dc}^* - V_{dc}\right) + \left[K_i.\int\left(V_{dc}^* - V_{dc}\right)\right] \quad (49)$$

To obtain sinusoidal current for the grid, first, the reference current is determined from the product of the outputs of PI controller and BPF using (50). Next, the result is compared with the actual current of the grid, and then, the unipolar voltage switching controlled sinusoidal pulse width modulation (SPWM) technique is used to produce the gate pulses of S_1–S_4 in the proposed MI, as shown in Fig. 9.

$$\mathbf{i}_s^* = \mathbf{U} \times \mathbf{V}_{s1} \quad (50)$$

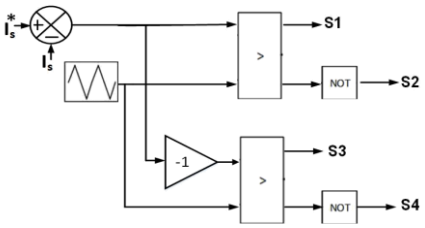

Fig. 9 Switching of S_1–S_4 based on the unipolar voltage switching technique.

Table 2 Specifications of the proposed MI.

Switching frequency	DC-DC converter:100 kHz DC-AC converter:10 kHz
Single-phase grid voltage	$110\sqrt{2}\sin(100\pi t)$
Rated power	300 W
Specifications of switches	S_5: FDMS86180 S_1–S_4: IXFX55N50 D_1–D_2: C3D03060E
Capacitors	C_{dc} = 300 µF C_1=6 µF C_{in} =200 µF C_f = 2 µF
Inductors	L_m = 20 µH L_f = 5 mH N = 4

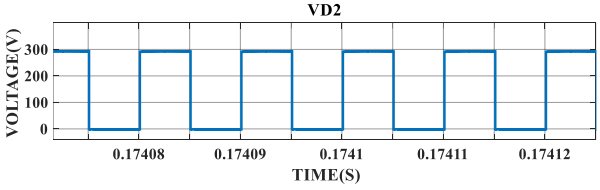

Fig. 12 Voltage across D_2.

6 Simulation Results

The PV panel and the specifications of the proposed MI are shown in Tables 1 and 2, respectively.

The voltage stress on S_5 is 60 V according to (28), which can also be seen in Fig. 10. Moreover, the voltage stress on the switch is much smaller than the converter output voltage, so a low voltage switch with a small $R_{ds(on)}$ can be used. This reduces the conduction losses of S_5 and increases the MI efficiency.

According to (23), the voltage of diode D_1 is 240 V, which agrees with the results in Fig. 11.

Table 1 PV panel specifications.

Notation	Parameter	Value
I_{sc}	Short-circuit current	8.68 A
V_{oc}	Open-circuit voltage	45.3 V
V_{mp}	Voltage at maximum power	36.7 V
I_{mp}	Current at maximum power	8.18 A
P_m	Maximum power	300 W

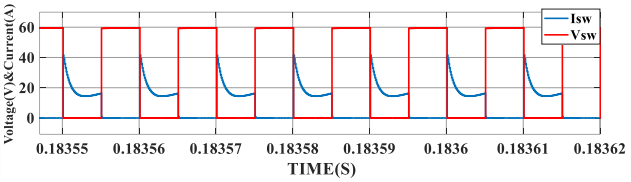

Fig. 10 Voltage and current of the DC-DC converter switch.

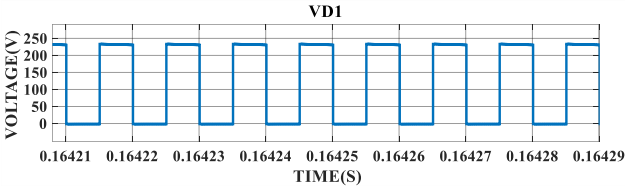

Fig. 11 Voltage across D_1.

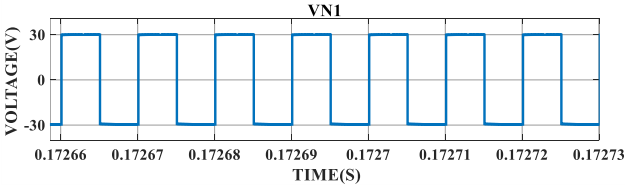

Fig. 13 Primary side voltage of the coupled inductor.

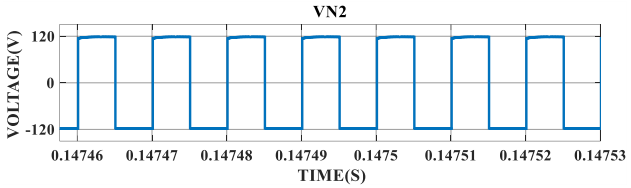

Fig. 14 Secondary side voltage of the coupled inductor.

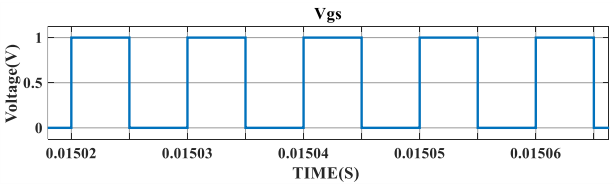

Fig. 15 Gate-source voltage of S_5.

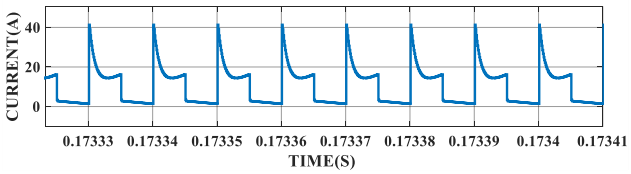

Fig. 16 Input current of MI.

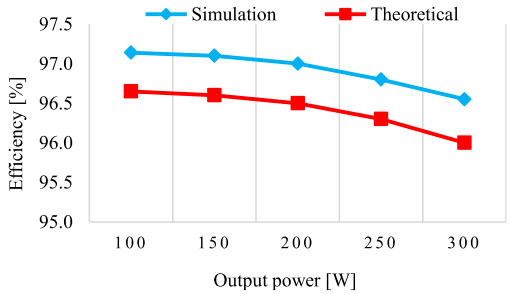

Fig. 17 DC-DC converter efficiency curve.

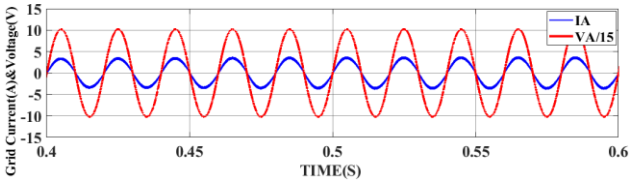

Fig. 18 Voltage and current injected into the grid.

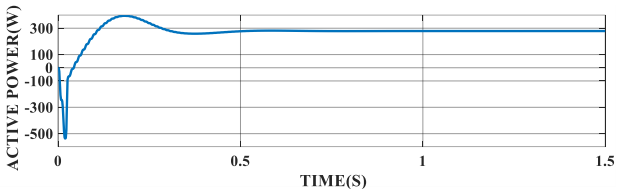

Fig. 19 Active power injected into the grid.

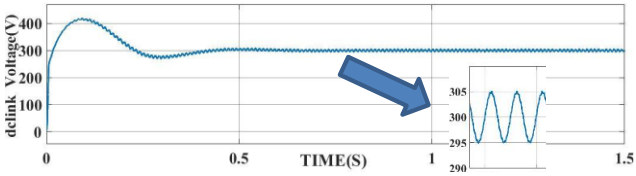

Fig. 20 DC-link decoupling capacitor voltage.

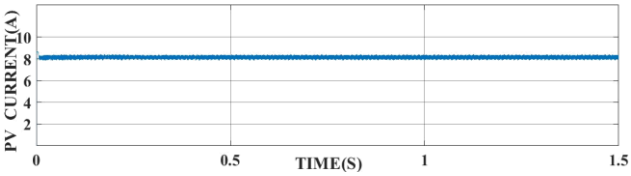

Fig. 21 PV panel current from the INC algorithm.

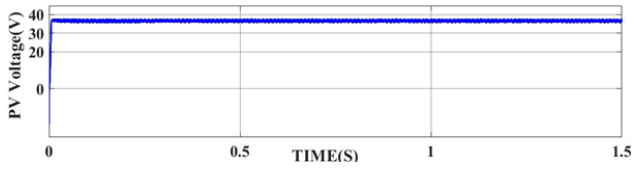

Fig. 22 PV panel voltage from the INC algorithm.

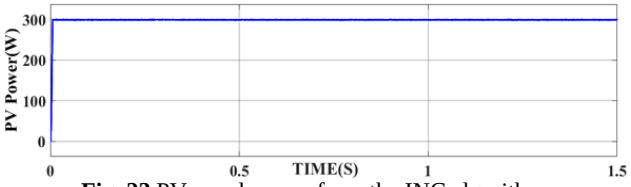

Fig. 23 PV panel power from the INC algorithm.

According to (24), the voltage of diode D_2 is 300 V, as can also be seen in Fig. 12

From the design equations, the conversion ratio of the coupled inductor is selected to be 4. Therefore, Eqs. (1) and (2) give the primary and secondary voltages as 30 V and 120 V, respectively, as shown in Figs. 13 and 14, respectively. Moreover, from the design equations, the duty ratio of S_5 is 50% as can be seen in Fig. 15.

Fig. 16 shows the continuous input current of the proposed MI. This current leads to a longer lifetime and higher reliability of the MI, as well as it allows maximum power point tracking in the PV system.

Fig. 17 shows the first stage efficiency curve of the proposed MI. This stage includes the SEPIC DC-DC converter. The efficiency values from theoretical calculations and simulation results are, respectively, 96% and 96.5% at rated power.

Fig. 18 shows the voltage and current injected into the grid by the proposed MI at 300 W.

As shown, the proposed MI and its control system properly inject current and voltage into the single-phase grid at unity power factor. Fig. 19 shows the active power injected into the grid.

The proposed control system can inject an effective active power of 283.7 W into the power grid. Fig. 20 shows the DC-link capacitor voltage of the proposed MI, which is well adjusted to the reference value of 300 V by the PI controller. Furthermore, according to (30) and the capacitor ripple voltage shown in Fig. 20, it can be confirmed that three parallel film capacitors with a total capacitance of 300 µF are used in the proposed MI.

Figs. 21, 22, and 23 show, respectively, the current, voltage, and power curves of the PV panel based on the INC algorithm.

From Table 1, the INC algorithm properly tracks the points of maximum current (I_{mp}), voltage (V_{mp}), and power (P_m). Moreover, this algorithm achieves an MPPT efficiency of 99% and the average power of the PV panel is 298.4 W.

Figs. 24, 25, 26, and 27 show, respectively, S_1, S_2, S_3, and S_4 of the proposed MI using SPWM with unipolar voltage switching. The accurate switching of S_1–S_4 can be confirmed by the switching pattern shown in Fig. 9.

Fig. 28 shows the total harmonic distortion (THD) of the proposed MI with an LC filter at a switching frequency of 10 kHz.

The THD of the proposed grid-connected MI is 2.01%, which is less than 5%, according to the standards IEEE1547.2 and IEC61727 [26].

Figs. 29–33 show the dynamic response of the proposed MI when the solar radiation intensity in the PV panel decreases from 1000 to 800 W/m^2 at 0.7 s. At this moment, the current and power of the PV panel decrease. In this situation, the output power of the MI is greater than the input power, so the DC-link voltage of the MI is reduced to maintain power balance. Then, the PI controller senses the voltage drop and issues the corresponding reduction command to control the output current of the MI and regain the system balance. Under these conditions, the response is relatively fast and smooth and the current is sinusoidal despite the changes in radiation. The controller properly adapts itself to the new conditions and tracks the appropriate reference.

Fig. 34 shows the theoretical results of loss analysis of the proposed MI, which are obtained from the loss analysis equations in Section 4. From this figure, the total loss of the proposed MI is equal to 18.43 W. The efficiency values from theoretical calculations (Eq. (37)) and simulation results are, respectively, 93.8% and 95% at a rated power of 300 W.

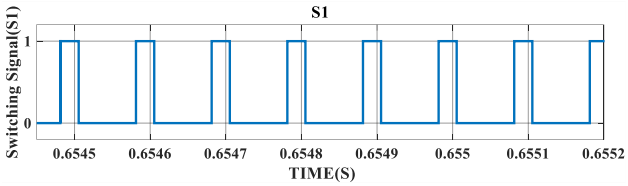

Fig. 24 S_1 of the proposed MI.

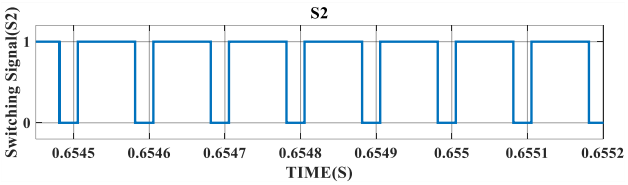

Fig. 25 S_2 of the proposed MI.

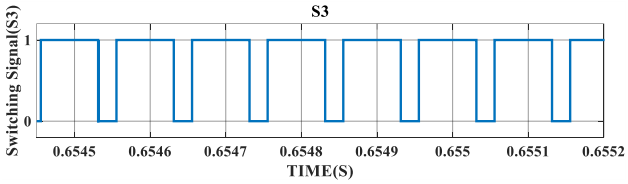

Fig. 26 S_3 of the proposed MI.

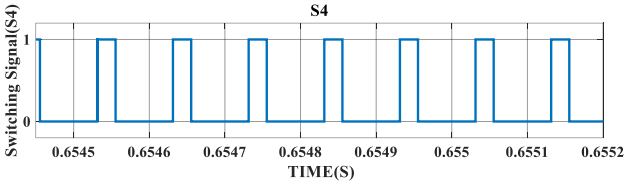

Fig. 27 S_4 of the proposed MI.

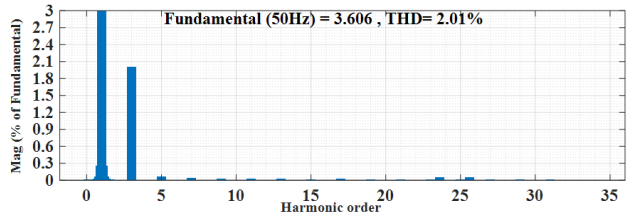

Fig. 28 THD curve of the proposed grid-connected MI.

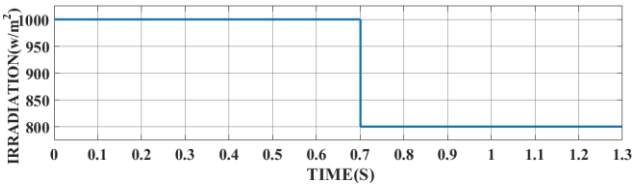

Fig. 29 Solar radiation variation at 0.7 s.

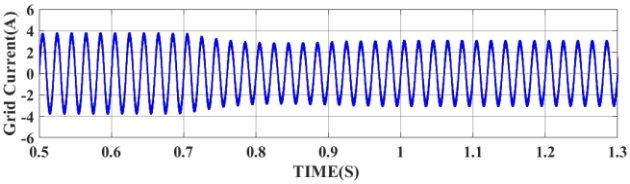

Fig. 30 Grid current variation at 0.7 s.

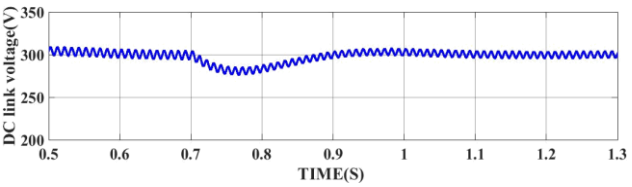

Fig. 31 PV DC-link variation at 0.7 s.

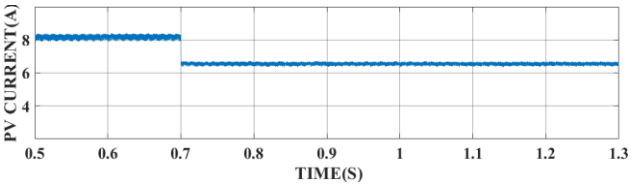

Fig. 32 PV current variation at 0.7 s.

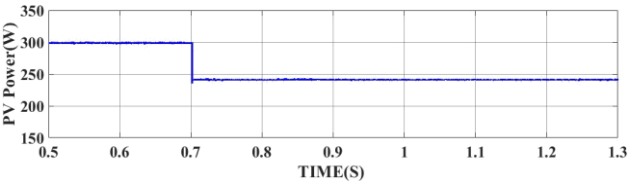

Fig. 33 PV power variation at 0.7 s.

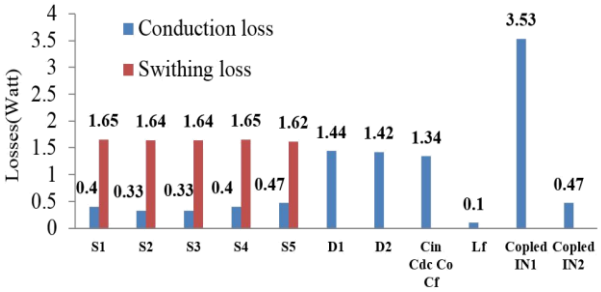

Fig. 34 MI loss analysis curve.

7 Conclusion

This paper proposed a grid-connected single-phase micro-inverter (MI) with a rated power of 300 W and an appropriate control strategy for photovoltaic (PV) systems.

By eliminating the APDC, which is typically used in single-stage SEPIC-based MIs, both long lifetime and high efficiency were achieved.

The advantages of the proposed MI are the use of fewer components to provide suitable output voltage level for connection to a single-phase grid, continuous input current, limited voltage stress on the switch, high efficiency, long operational lifetime, and high reliability. Lower input current ripple and the presence of film capacitors in the power decoupling circuit increased the lifetime and reliability of the proposed MI. Moreover, the proposed MI had a two-stage topology. In the first stage, a SEPIC DC-DC converter with high voltage gain was used to step up the voltage of the PV panel and harness the maximum power, while the second stage included a full-bridge DC-AC converter. The performance of the proposed control system was verified with the purposes of harvesting maximum PV power, stabilizing the DC-link voltage, injecting low THD sinusoidal current into the grid, and controlling the active power injected into the grid at unity power factor. Moreover, the performance of the proposed control system was studied for a sudden change in solar radiation. Using film capacitors in the DC-link, power decoupling was realized without requiring additional circuits (i.e., APDC). The long lifetime of the proposed MI is guaranteed by the presence of film capacitors for power decoupling and lower input current ripple to the MI. The proposed MI achieves a high voltage output due to the use of coupled inductors, so this topology operates well even under low input voltage conditions. Moreover, the efficiencies from theoretical calculations and simulation results are 93.8% and 95%, respectively.

Intellectual Property

The authors confirm that they have given due consideration to the protection of intellectual property associated with this work and that there are no impediments to publication, including the timing of publication, with respect to intellectual property.

Funding

No funding was received for this work.

CRediT Authorship Contribution Statement

S. Saeedinia: Conceptualization, Methodology, Software, Formal analysis, Writing - Original draft. **M. A. Shamsi-Nejad:** Supervision. **H. Eliasi:** Data curation.

Declaration of Competing Interest

The authors hereby confirm that the submitted manuscript is an original work and has not been published so far, is not under consideration for publication by any other journal and will not be submitted to any other journal until the decision will be made by this journal. All authors have approved the manuscript and agree with its submission to "Iranian Journal of Electrical and Electronic Engineering".

References

[1] O. P. Mahela and A. G. Shaik, "Comprehensive overview of grid interfaced solar photovoltaic systems," R*enewable and Sustainable Energy Reviews*, Vol. 68, pp. 316–332, Feb. 2017.

[2] M. Keshani, E. Adib, and H. Farzanehfard, "Micro-inverter based on single-ended primary-inductance converter topology with an active clamp power decoupling," *IET Power Electronics*, Vol. 11, No. 1, pp. 73–81, Feb. 2018.

[3] H. S. Lee and J. J. Yun, "Quasi-resonant voltage doubler with snubber capacitor for boost half-bridge DC-DC converter in photovoltaic micro-inverter," *IEEE Transactions on Power Electronics*, Vol. 34, No. 9, pp. 8377–8388, Sep. 2019.

[4] J. Kan, Y. Wu, Y. Tang, and L. Jiang, "DLFCR reduction based on power predictive scheme for full-bridge photovoltaic micro-inverter," *IEEE Transactions on Industrial Electronics*, Vol. 67, No. 6, pp. 4658–4669, Jun. 2020.

[5] R. Hasan, W. Hassan, M. Farhangi, S. Mekhilef, and W. Xiao, "Enhanced soft-switching strategy for flyback based microinverter in PV power systems," *IET Renewable Power Generation*, Vol. 13, No.15, pp. 2830–2839, Nov. 2019.

[6] A. Jamatia, V. Gautam and P. Sensarma, "Power decoupling for single phase PV system using C´uk derived micro-inverter," *IEEE Transactions on Industry Applications*, Vol. 54, No. 4, pp. 3586–3595, 2018.

[7] J. Kan, Y. Wu1, Y. Tang, and S. Xie, "Flexible topology converter used in photovoltaic micro-inverter for higher weighted-efficiency," *IET Power Electronics*, Vol. 12, No. 9, pp. 2361–2371, Aug. 2019.

[8] D. Mathew and R. C. Naidu, "Investigation of single-stage transformerless buck–boost microinverters," *IET Power Electronics*, Vol. 13, No. 8, pp. 1487–1499, May. 2020.

[9] J. Kan, Y. Wu, Y. Tang, S. Xie, and L. Jiang, "Hybrid control scheme for photovoltaic micro-inverter with adaptive inductor," IE*EE Transactions on Power Electronics*, Vol. 34, No. 9, pp. 8762–8774, Sep. 2019.

[10] D. Wu, Y. Wu, J. Kan, Y. Tang, J. Chen, and L. Jiang, "Full-Bridge current-fed PV microinverter with DLFCR reduction ability," IEE*E Transactions on Power Electronics*, Vol. 35, No. 9, pp. 9541–9552, Sep. 2020.

[11] Y. Zhang, J. Xiong, P. He, and S. Wang, "Review of power decoupling methods for micro-inverters used in PV systems," *Chinese Journal of Electrical Engineering*, Vol. 4, No. 4, pp. 26–32, Dec. 2018.

[12] T. Sreekanth, N. Lakshminarasamma, and M. K. Mishra, "A single-stage grid-connected high gain buck–boost inverter with maximum power point tracking," *IEEE Transactions on Energy Conversion*, Vol. 32, No.1, pp. 330–339, Mar. 2017.

[13] R. K. Surapaneni and A. K. Rathore, "A single-stage CCM zeta microinverter for solar photovoltaic AC module," *IET Power Electronics*, Vol. 3, No. 4, pp. 892–900, Dec. 2015.

[14] H. Hu, S. Harb, N. H. Kutkut, Z. J. Shen, and I. Batarseh, "A single-stage microinverter without using eletrolytic capacitors," *IEEE Transactions on Power Electronics*, Vol. 28, No. 6, pp. 2677–2687, Jun. 2013

[15] M. Hadi Zare, M. Mohamadian, and R. Beiranvand, "A single-phase grid-connected photovoltaic inverter based on a three-switch three-port flyback with series power decoupling circuit," *IEEE Transactions on Industrial Electronics*, Vol. 64, No. 3, pp. 2062–2071, Mar. 2017.

[16] C. Liao, W. Lin, Y. Chen, and C. Chou, "A PV micro-inverter with PV current decoupling strategy," *IEEE Transactions on Power Electronics*, Vol. 32, No. 8, pp. 6544–6557, Aug. 2017.

[17] H. Do, "Soft-switching SEPIC converter with ripple-free input current," *IEEE Transactions on Power Electronics*, Vol. 27, No. 6, pp. 2879–2887, Jun. 2012.

[18] Y. P. Siwakoti, A. Mostaan, A. Abdelhakim, P. Davari, M. N. Soltani, M. N. Habib Khan , L. Li, and F. Blaabjerg, "High-voltage gain quasi-SEPIC DC–DC converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. 7, No. 2, pp. 1243–1257, June. 2019.

[19] S. Lee and H. Do, "Isolated SEPIC DC–DC converter with ripple-free input current and lossless snubber," IE*EE Transactions on Industrial Electronics*, Vol. 65, No. 2, pp. 1254–1262, Feb. 2018.

[20] R. Moradpour, H. Ardi, and A. Tavakoli, "Design and implementation of a new SEPIC-based high step-up DC/DC converter for renewable energy applications," *IEEE Transactions on Industrial Electronics*, Vol. 65, No. 2, pp. 1290–1297, Feb. 2018.

[21] M. Büyük, A. Tan, M. Tümay, and K. C. Bayındır, "Topologies, generalized designs, passive and active damping methods of switching ripple filters for voltage source inverter: A comprehensive review", *Renewable and Sustainable Energy Reviews*, Vol. 62, pp. 46–69, April. 2016.

[22] A. Khoshkbar-Sadigh, V. Dargahi, K. Lakhera, and K. Corzine, "Analytical design of LC filter inductance for two-level inverters based on maximum ripple current," in *45th Annual Conference of the IEEE Industrial Electronics Society (IECON 2019)*, pp.1621–1626, Dec. 2019.

[23] S. A. Ansari, J. N. Davidson, and M. P. Foster, "Evaluation of silicon MOSFETs and GaN HEMTs in soft-switched and hard-switched DC-DC boost converters for domestic PV applications," *IET Power Electronics*, Vol. 14, No. 5, pp. 1023–1043, Feb. 2021.

[24] S. A. Ansari and J. S. Moghani," A novel high voltage gain noncoupled inductor SEPIC converter," *IEEE Transactions on Industrial Electronics*, Vol. 66, No. 9, pp. 7099–7108, Sep. 2019.

[25] T. Radjai, L. Rahmani, S. Mekhilef, and J. P. Gaubert, "Implementation of a modified incremental conductance MPPT algorithm with direct control based on a fuzzy duty cycle change estimator using dSPACE," *Elsevier Solar Energy*, Vol. 110, pp. 325–337, Nov. 2014.

[26] R. Hasan, S. Mekhilef, M. Seyedmahmoudian, and B. Horan, "Grid-connected isolated PV microinverters: A review," *Renewable and Sustainable Energy Reviews*, Vol. 67, pp. 1065–1080, Jan. 2017.

S. Saeedinia was born in Birjand, Iran, in 1997. He received his B.Sc. in Power Electrical Engineering in 2019 from the University of Birjand, Birjand, Iran, and his M.Sc. degree in Power Electronics Engineering from the University of Birjand, Birjand, Iran, in 2021.His research interests include micro-inverter, DC-DC converters, efficiency improvements, grid-connected photovoltaic systems.

M. A. Shamsi-Nejad received the B.Sc. degree in Electrical Engineering and the M.Sc. degree from the Sharif University of Technology, Tehran, Iran, in 1990 and 1996, respectively, and the Ph.D. degree from the Institut National Polytechnique de Lorraine (INPL), Nancy, France, in 2006. He is currently an Associate Professor at Birjand University, Iran. His research interests include Birjand University deal with control of electrical machines, renewable energies, and power electronics.

H. Eliasi received the B.Sc. degree in Electrical Engineering from the Ferdowsi University of Mashhad (FUM), Iran, in 2001. He received the M.Sc. and the Ph.D. degrees from Amirkabir University of Technology (Tehran), Iran, in 2005 and 2011, respectively. He is currently an Assistance Professor in the Faculty of Electrical Engineering at the University of Birjand, Iran. His research interests include constrained nonlinear dynamics systems, robust control, parameter optimization of model predictive control, transient stability in power systems, and load following by nuclear power plants.