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Research Paper

An Area Efficient Low Dropout Voltage Regulator With Improved Transient Response for Hearing-aid Applications

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Abstract: This paper presents a low dropout voltage regulator, with the specifications suitable for hearing aid devices. The proposed LDO occupies very less area on chip and provides an excellent transient response. A novel voltage spike suppressor block is employed in the LDO architecture which reduces undershoot and overshoot of the output voltage during the abrupt load transition. It introduces a secondary negative feedback loop whose delay is lesser than the main loop and also steers the quiescent current to output node when required. This not only improves overall current efficiency but also reduces the on chip capacitance. The proposed LDO is laid out in 180 nm standard CMOS technology and post layout simulations are carried out. The LDO produces 0.9 V output when a minimum supply voltage of 1 V is applied. A maximum load of 0.5 mA can be driven by the regulator. The LDO exhibits 4.4 mV/V and 800 μV/mA line and load regulations respectively. When subjected to a step load change, an undershoot of 20.34 mV and an overshoot of 30.28 mV are recorded. For proper operation of the LDO, it requires only 4.5 pF on-chip capacitance.

Keywords: LDO, Voltage Regulator, Hearing-aid, Transient Response, Area Efficient, Bio-Medical Applications.

1 Introduction

AN electronic hearing aid is a device which is worn by those who are suffering from hearing loss. It basically consists of microphone for converting sound from physical to electrical form, signal conditioning, a receiver for converting electrical signals back to sound and a battery for powering the electronics [1], [2].

There are four types of hearing-aids [3] namely, behind the ear (BTE), in the ear (ITE), in the canal (ITC) and completely in the canal (CIC). A hearing-aid device can be analog or digital but digital hearing aid is more popular due to its better performance and flexibility. Fig. 1 shows functional block diagram of a digital hearing-aid [3].

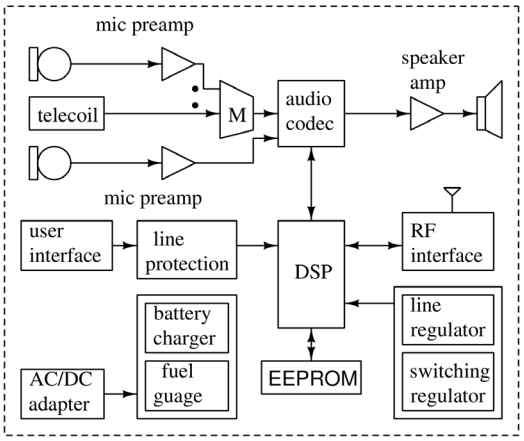

Fig. 1 Functional block diagram of a digital hearing-aid.

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The batteries used in hearing aid are usually lithium ion or zinc air. The switching regulators are primarily used for stepping down the voltage level to a lower value. Later, linear voltage regulators are required for providing supply voltage to individual components since they are fast, simple and induce less noise. Typical voltages produced by linear regulators are around 1 V and they deliver load ranging from 0.5 mA to 5 mA depending on the type of hearing-aids. However, the area occupancy and transient response are the main constraints while designing linear voltage regulators for hearing-aid applications.

In linear regulators, Low Drop Out (LDO) voltage regulators are the most preferred, since they have better power efficiency and suitable for low power applications [4]. LDO is basically a negative feedback system which provides a constant output voltage (Which is slightly less than input voltage) irrespective of variations in supply voltage and load demand, by adjusting the conductivity of pass device. Depending on whether LDO is internally or externally compensated, the design strategy varies. Externally compensated LDO requires a large off-chip capacitor which prohibits complete system on chip solution. Hence the LDO which is going to be used in hearing aid device must be internally compensated. However, internal compensation also demands an output on-chip capacitor whose value can reach up to 100 pF [5]-[10].

Though the system can be integrated on a chip, it occupies a large area. In recent years, many have proposed [7], [11]-[21] modifications in the architecture of the LDO which try to reduce area occupancy and improve transient response. In [11], [19], [21], the authors have used two feedback loops, one being the fast and the other being the slow. Fast loop tries to minimize the variation in the spikes. The LDO needs only a 4 pF on-chip capacitance. But, undershoot and overshoot values during load transition is high. The author of [12] has proposed an LDO for bio-medical applications which is based on flipped voltage follower and adaptive biasing technique. High loop gain is established and different compensation techniques are included to achieve stability. Though better line and load regulations are obtained, transient response is degraded. The quiescent current of the LDO can be increased momentarily during abrupt load change for better transient response and power efficiency. This technique is implemented in [5], [13], [22], but the circuit used to detect undershoot and overshoot at the output voltage and pump the additional current to system consumes an idle current which degrades the current efficiency. In [7], an LDO which consists of three input error amplifier and buffered flipped voltage follower is proposed. The topology includes three different feedback loops for improving the performance of the LDO. However, it suffers from poor line and load regulations. In the present work, an LDO is proposed which not only occupies less area on chip but also exhibits a better transient response. The circuit includes a novel voltage spike suppressor block, from which a better transient response is obtained.

This article consists of four sections. In the first section, introduction and literature review is given. The design and working principle of the LDO is elaborated in the second section. It is followed by a section which presents the simulation results and discusses on the same. Finally, the article ends with the conclusion.

2 Design of the Proposed LDO

Figure 2 shows the basic structure of the proposed LDO. The main blocks are Operational Trans-Conductance Amplifier (OTA), pass transistor, voltage spike suppressor and feedback network. In this section, each block of the LDO is explained.

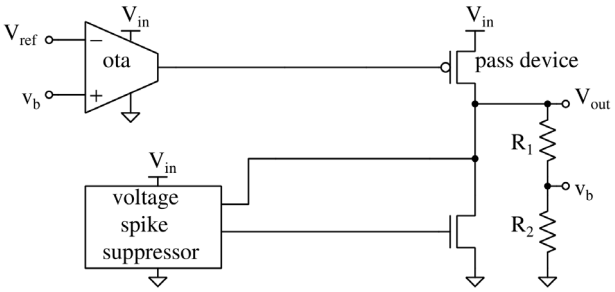

Fig. 2 Basic structure of the proposed LDO.

2.1 OTA

OTA basically acts as error amplifier which compares feedback voltage with the reference voltage. The OTA used in the proposed LDO is depicted in Fig. 3 [23]. PMOS differential input pair is used to facilitate better common mode input range. One of the advantages of using OTA is that it has a single dominant pole which resides at the output node. Hence, it does not need any compensation capacitance, which reduces the area occupancy on chip. The large parasitic capacitance

present at the gate of the pass transistor is the load capacitance of the OTA.

2.2 Voltage Spike Suppressor Block

In a LDO, whenever there is an abrupt change in load, the voltage spike is observed at the output node. This is due to the large parasitic capacitance of pass device needs to be charged and discharged in a short period of time. This demands an increase in quiescent current of OTA. However, in the proposed LDO, instead, a secondary loop is introduced which avoids the above path that consists of pass device. The loop delay of the secondary feedback is less, this aids in reducing the spike at the output voltage. A voltage controlled current source along with RC differentiator constitute voltage spike suppressor block. Hence, it comes into action only during the abrupt load transition and adjusts the quiescent current accordingly. Figure 4 shows the circuit diagram of the proposed novel voltage spike suppressor. The capacitor CB and RB form a differentiator circuit. The RB acts as miller resistor, so the effective resistance value is higher than the actual value. During undershoot of the output voltage, a negative voltage spike is detected at node 1. Since, M_{12} is in common source configuration, a positive voltage spike appears at node 2.

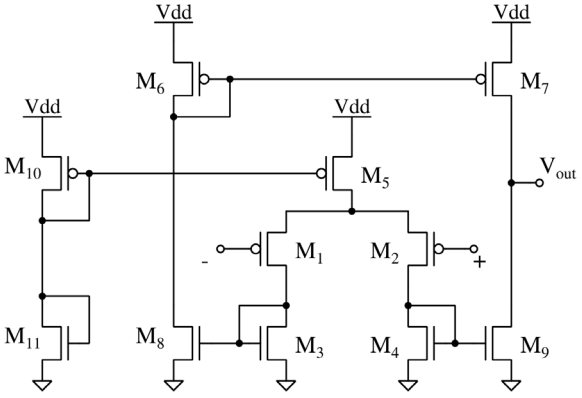

Fig. 3 Circuit diagram of OTA used in the LDO.

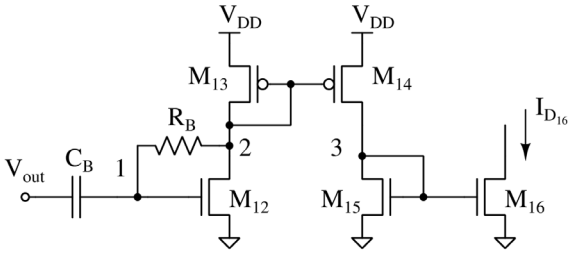

Fig. 4 Circuit diagram of voltage spike suppressor.

The M_{14} is also in common source configuration, so a negative spike at node 3 forces M_{16} to draw less current. This way, during undershoot, a less current is drawn by M_{16} , the pass transistor can steer this current to output node, which will aid in reducing voltage variation. Similarly, during the overshoot, transistor M_{16} draws more current, thereby decreases the voltage spike.

The small signal equivalent model of the proposed voltage spike suppressor is shown in Fig. 5.

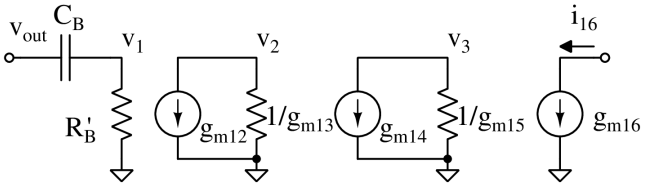

Fig. 5 Small signal circuit of voltage spike suppressor.

The notation convention used in the small signal analysis is given below.

- g_{m12}, g_{m13}, g_{m14}, g_{m15}, g_{m16} → Trans-conductance of M_{12}, M_{13}, M_{14}, M_{15} and M_{16} respectively.
- r_{op12}, r_{op13}, r_{op14}, r_{op15}, r_{op16} → Output resistance of M_{12}, M_{13}, M_{14}, M_{15} and M_{16}, respectively.
- v_1, v_2, v_3 → Small signal voltage at node 1, 2 and 3, respectively.
- I_{D16} → Small signal drain current of M_{16}.

In the small signal analysis shown below, feedback resistor R_B and C_B together act like a high pass filter which senses the instantaneous changes in the output voltage. R_B is split using Miller's theorem into R_B' and R_B". Where:

$R_B' = R_B\,(1 + A_v/g_{m13})$, $R_B'' \approx R_B$ and $A_v = v_2/v_1$. Also, we have assumed following:

- $R'' \parallel r_{op12} \parallel r_{op13} \parallel (1/g_{m13}) = (1/g_{m13})$
- $r_{op14} \parallel r_{op15} \parallel (1/g_{m15}) = (1/g_{m13})$
- Parasitic capacitance at node 2 and 3 create poles beyond unity gain frequencies because of low impedance. Hence they are ignored.

$$v_3 = \frac{-g_{m14}}{g_{m15}} v_2$$

$$v_3 = \frac{g_{m14}}{g_{m15}} \times \frac{g_{m12}}{g_{m13}} v_1 \qquad (1)$$

$$i_{16} = g_{m16} v_3$$

$$i_{16} = g_{m16} \frac{g_{m14}}{g_{m15}} \times \frac{g_{m12}}{g_{m13}} v_1$$

Let G_{Msup} be the total trans-conductance of the voltage spike suppressor which is given by Eq. (2).

$$G_{\text{Msup}} = \frac{i_{16}}{v_1} = \frac{g_{m16} \times g_{m14} \times g_{m12}}{g_{m15} \times g_{m13}} v_1 \qquad (2)$$

The loop delay of the voltage spike suppressor is lesser than the main feedback loop, which is very crucial in reducing the voltage spike. Figure 6 shows the transient response of gate voltage of pass transistor during undershoot (when load changes from 0 mA to 0.5 mA in 1 µs) of the LDO output. It can be seen that main negative feedback takes 1.228 µs to respond. Whereas, negative feedback created by voltage spike suppressor loop takes only 0.25 µs to respond as shown in Fig. 7, where, transient response of gate voltage of M_{16} is plotted. To investigate the impact of the voltage spike suppressor on load transient response of the proposed LDO, it is subjected to abrupt load transition with and without the voltage spike suppressor. A pulse of load with minimum to maximum value, 1 µs transition time and 6 µs pulse width is applied and output voltages for the both cases are plotted in Fig. 8. During this time, the variation of gate voltage of M_{16} (when the voltage suppressor block is used) is shown in Fig 9. There is 28.83% reduction in undershoot voltage and 9.46% reduction in overshoot voltage when proposed voltage spike suppressor is employed.

2.3 Complete Circuit

A PMOS transistor with 100 mV as saturation voltage for the maximum load is used as pass device for the LDO. A reference voltage of 500 mV is required at the inverting terminal of the OTA which is supplied from an external source. The capacitor C M and CC are added to improve the phase margin of the LDO [24]. The resistors R_1 and R_2 form a resistive divider network with 10 µA as biasing current. Figure 10 shows the complete circuit diagram of the proposed LDO. Table 1 shows the values of the components used in LDO.

3 Stability Analysis

The small signal model of the proposed LDO is shown in Fig. 11. The notation convention used in the Fig. 11 is explained below,

- g_{mE} → Trans-conductance of the error amplifier.
- g_{mp} → Trans-conductance of the pass transistor.
- c_{oE} → Effective parasitic capacitance at the output of the error amplifier.
- c_o → Effective parasitic capacitance at the output of the LDO.
- r_{oE} → Output resistance of error amplifier.
- r_{op} → Output resistance of pass transistor.

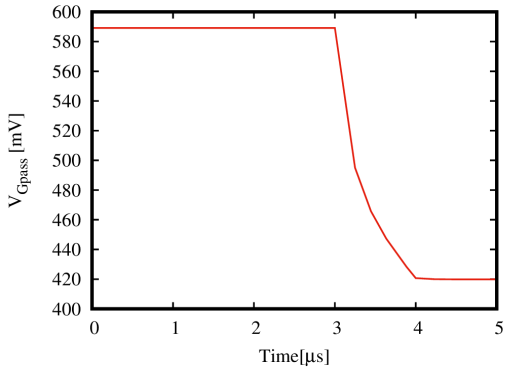

Fig. 6 Transient response of gate voltage of pass transistor.

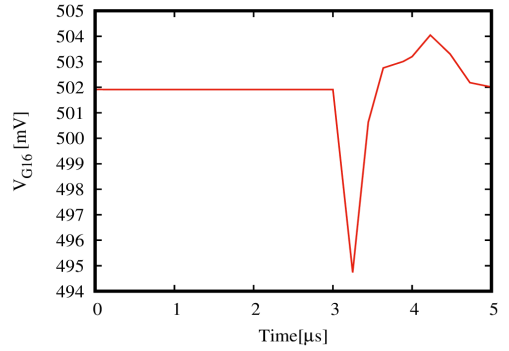

Fig. 7 Transient response of gate voltage of M_{16} transistor.

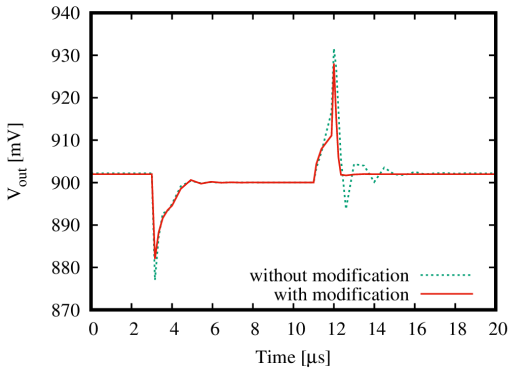

Fig. 8 Comparison of the load transient response of proposed LDO with and without voltage suppressor block.

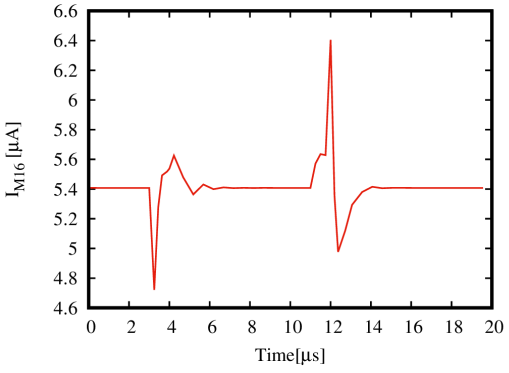

Fig 9. Transient response of drain current of M_{16} transistor.

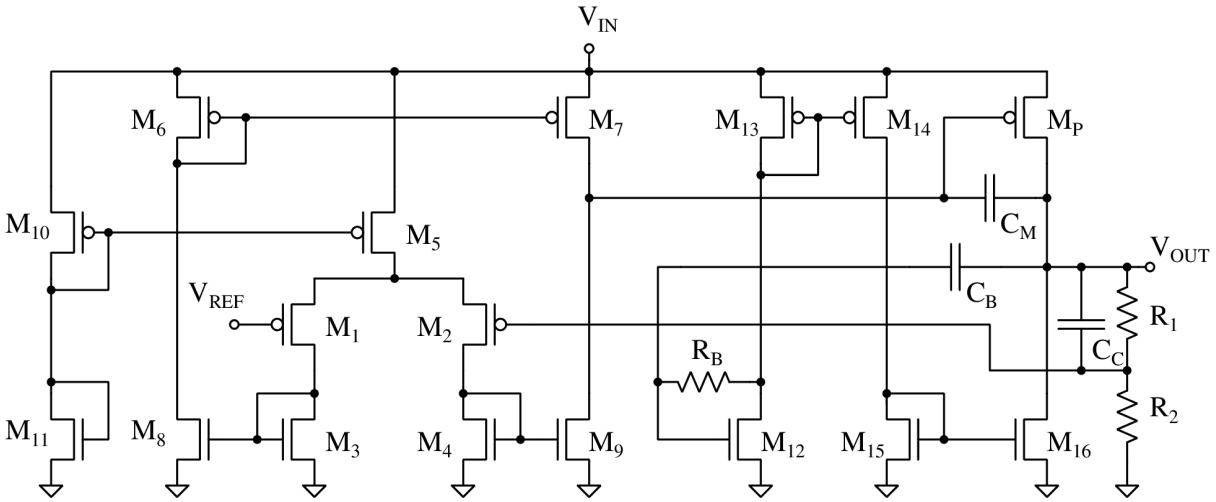

Fig. 10 The complete circuit diagram of the proposed LDO.

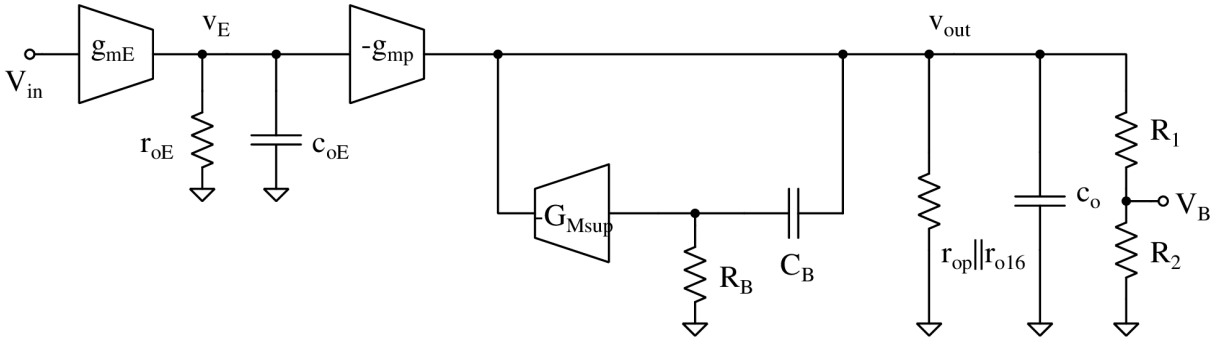

Fig. 11 Small signal model of the proposed LDO.

Table 1 Component valued used in LDO.

Component	Value
M_1-M_{10}	5 µm / 1 µm
M_{11}	1 µm / 5 µm
M_{12}	16 µm / 1 µm
M_{13}	8 µm / 1 µm
M_{14}	4 µm / 1 µm
M_{15}	10 µm / 1 µm
M_{16}	8 µm / 1 µm
M_P	20 µm / 0.2 µm, M=20
C_M	0.5 p
C_C, C_B	2 p
R_1	40 kΩ
R_2	50 kΩ
R_B	200 kΩ

Let Zo be the output impedance of the LDO. It is given by:

$$Z_O = r_{op} \parallel r_{16} \parallel \frac{1}{\omega c_O} \parallel \left[\left(R_1 \parallel \frac{1}{\omega c_C}\right) + R_2\right]$$

Let ($r_{op} \parallel r_{16}$) = r_o

$$v_{out} = \frac{-g_{mE} g_{mp} V_{in} r_{oE} r_o}{(1+\omega c_{oE} r_{oE})(1+\omega c_o r_o)} - \frac{v_{out} g_{Msup} r_o \omega C}{(1+\omega c_o r_o)(1+\omega C_B R_B)} \quad (3)$$

$$v_{out} = \frac{-g_{mE} g_{mp} V_{in} r_{oE} r_o}{(1+\omega C_{oE} r_{oE})(1+\omega c_o r_o)} \frac{(1+\omega C_B R_B)}{\left(1+\omega C_B R_B + \frac{g_{Msup} C_B R_B r_o}{1+\omega c_o r_o}\right)}$$

$$V_B = \left(\frac{R_2}{R_1+R_2}\right) v_{out} = \beta v_{out}$$

$$\frac{V_B}{V_{in}} = \beta \frac{-g_{mE} g_{mp} V_{in} r_{oE} r_o}{(1+\omega C_{oE} r_{oE})(1+\omega c_o r_o)}$$

The system has three poles and one zero. In that, the pole at the output of error amplifier and at the output of LDO are two main poles of concern in terms of the stability. The pole at the output of error amplifier consists of r_{oE} and c_{oE}. The c_{oE} includes the parasitic capacitances of pass transistor and output stage of error amplifier and miller capacitance C_M. The LDO output pole is formed due to the parallel combinations of r_{op}, r_{o16} and feedback resistors and capacitance c_o. The output parasitic capacitance of pass transistor, wiring bonds and pads are included in c_o. The parasitic capacitance c_{oE} is large because of Miller capacitance and large pass transistor. At the same time, the effective resistance at the output of LDO is reduced due to the presence of M_{16} and C_C. This way, the pole at the error amplifier output dominates. To verify the above, frequency response of the LDO is tested under different loads which are shown in Fig. 12. As mentioned earlier, a 50 pF capacitor is considered at the output of LDO to

model the parasitic capacitance of external bond wires and pads. In Table 2, the phase margin for fast and slow corners under different loads are listed. It can be observed that, in all the cases the phase margin of the LDO is greater than 45°, which proves the stability of the proposed LDO.

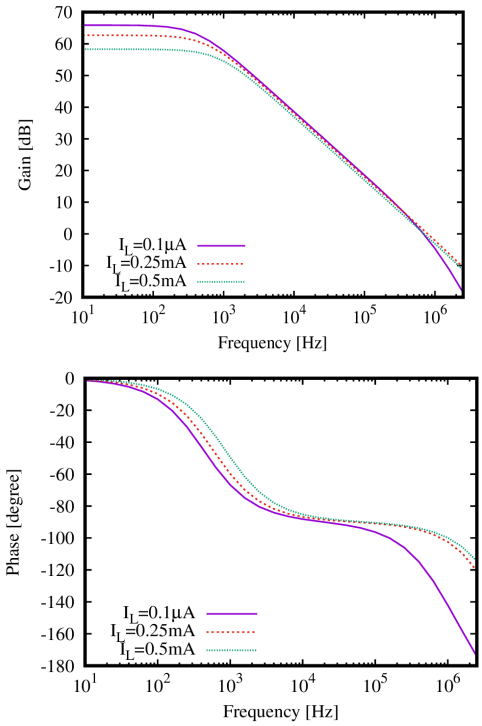

Fig. 12 Frequency response of the LDO under different loads.

Table 2 Phase margin of proposed LDO for process corners.

Process corner	Load	PM
Fast	0.1 µA	45.04 °
Fast	0.25 mA	75.70 °
Fast	0.5 mA	79.38°
Slow	0.1 µA	67.12°
Slow	0.25 mA	81.56°
Slow	0.5 mA	85.40 °

4 Results and Discussion

The proposed LDO has been laid out in standard 180 nm CMOS technology and post layout simulations have been carried out to verify the major performance parameters. In this section, simulation results have been presented and performance is compared with other state-of-the-art of LDOs.

The proposed LDO requires a minimum supply voltage of 1 V and it is varied from 1 V to 1.4 V considering different loads to find the line regulation. Figure 13 shows the line response of the LDO. It exhibits an average line regulation of 4.44 mV/V. For a supply voltage of 1 V, the LDO is subjected to different loads ranging from 0 to 0.5 mA under three process corners namely, typical (tt), fast (ff) and slow (ss) and result is shown in Fig. 14. A load regulation 800 µV/mA is recorded at typical corner.

Dynamic characteristics of the LDO are revealed in its load transient responses. To observe the load transient response, a pulse of 0.5 mA load with 1 µs transition time and pulse width of 6 µs is applied. The measured undershoot and overshoot voltage at typical corner are 20.34 mV and 30.28 mV respectively as shown in Fig. 15. The settling time during undershoot is 2.29 µs and during overshoot is 1.63 µs.

Figure 16 depicts the power supply rejection ratio (PSRR) of the designed LDO for different frequencies. At 1 kHz and full load, LDO exhibits a PSRR of 40 dB. The temperature response of the LDO is shown in Fig. 17. The output voltage of the LDO is plotted for different temperatures ranging from 0°C to 80°C under different process corners. At typical corner, the variation in output voltage for entire range of temperature is 0.73 V.

To investigate the robustness of LDO against global process variations and local mismatch, Monte-Carlo statistical analysis is carried out. The major device parameters, which are mobility and threshold voltage of MOSFETS are considered for variations and mismatch. Under the Gaussian distribution, 500 different samples of LDO are considered and steady state DC output voltages are measured. Histogram plot of DC output voltage versus different samples are plotted as shown in Fig. 18.

The mean and standard deviation of DC output voltage are 897.7 mV and 9.93 mV respectively. Similarly, undershoot voltage during load transient response are noted for different samples of the LDO and the corresponding histogram plot is shown in Fig. 19. The mean value of the undershoot voltage is 16.9 mV and standard deviation value is 10 mV. In both cases, it can be seen that mean value is close to typical value and standard deviation is less which proves the robustness of the LDO.

Figure 20 shows the layout picture of the proposed LDO. It occupies an area of 23 mm × 45 mm on chip. Table 3 shows the performance comparison of the proposed LDO with other state-of-the-art LDOs. The proposed LDO along with [11] has the lowest dropout voltage which leads to a better power efficiency. In the load transient variation parameter (ΔV_{out}), the proposed LDO exhibits an excellent response. The obtained ΔV_{out}

is the lowest among all. The area occupancy of an LDO is mainly dependent on the value of On-chip capacitance used in the design. Since the proposed LDO uses only 4.5 pF of On-chip capacitance, makes it suitable for hearing aid devices. However, quiescent current consumption of the proposed LDO can be reduced further. Since, dropout voltage is only 100 mV, the pass transistor is large and to achieve a good load transient response, relatively more quiescent current is required. The Figure of Merit (FOM) of all the tabulated lower the FOM, better the performance.

$$FOM = \frac{C_{on,chip} \times \Delta_{out} \times I_Q}{I_L} \quad (4)$$

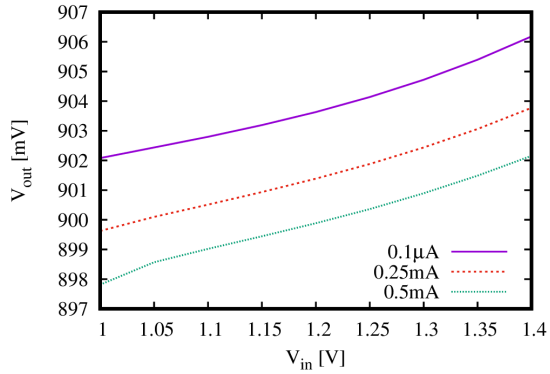

Fig. 13 Line response of the LDO.

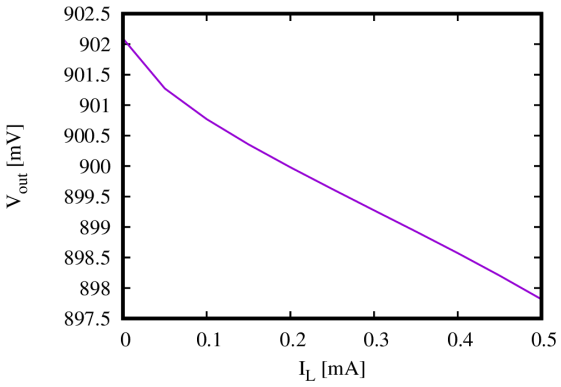

Fig. 14 Load response of the LDO.

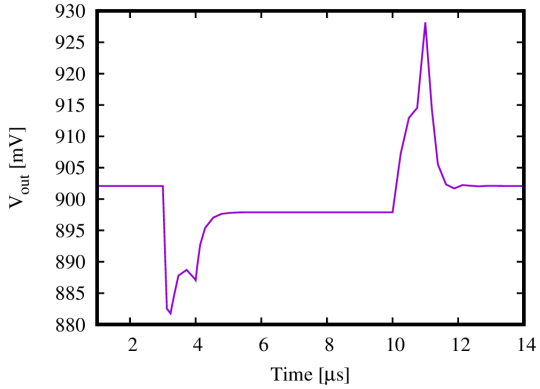

Fig. 15 Load transient response of the LDO.

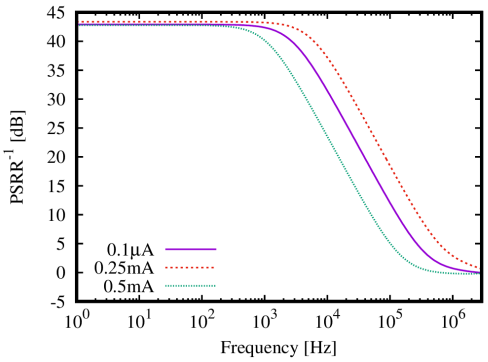

Fig. 16 Power supply rejection ratio of the LDO.

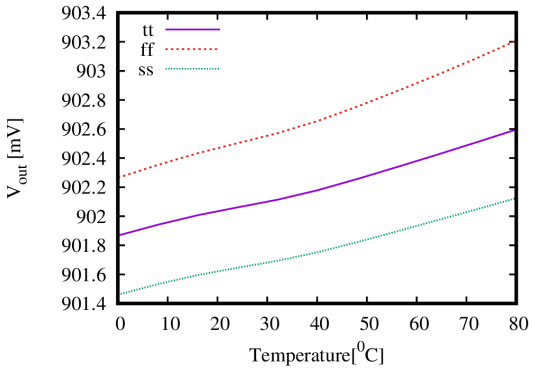

Fig. 17 Temperature response of the LDO.

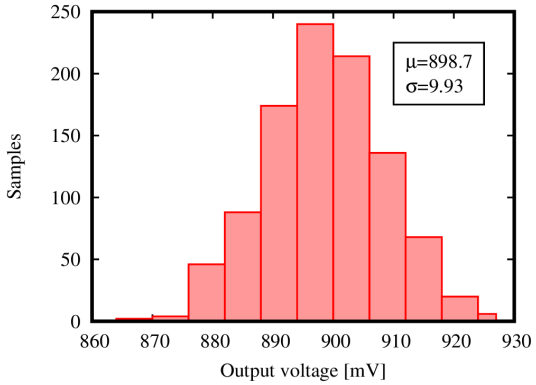

Fig. 18 Histogram plot of DC output voltage for different samples of the LDO.

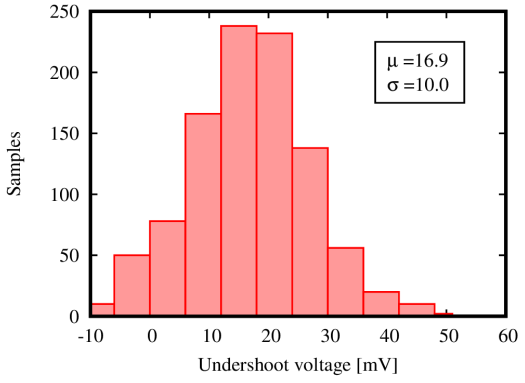

Fig. 19 Histogram plot of undershoot voltage during load transient response for different samples of the LDO.

Table 3 Performance Comparison with other LDOs.

Parameter	[11]	[17]	[13]	[25]	[16]	[7]	This work
Tech. [nm]	180	180	130	350	65	65	180
V_{out} [V]	0.9	1	1.2	1.6	0.5	1	0.9
I_L [mA]	0.5	5	50	12	10	10	0.5
I_Q [µA]	10.3	120	4.1	28.6	49.4	50	36.9
V_{DO} [mV]	100	200	200	400	250	150	100
Δ_{out} [mV]	64	148	198	105	41.6	82	26
$C_{on,chip}$ [pF]	4	44	100	28	16	140	4.5
t_{settle}[µs]	3	4.8	1.16	--	0.4	--	2.29
FOM [x10^{-21}]	5.2k	15.6k	1.6k	7k	3.2k	57.4k	8.6k

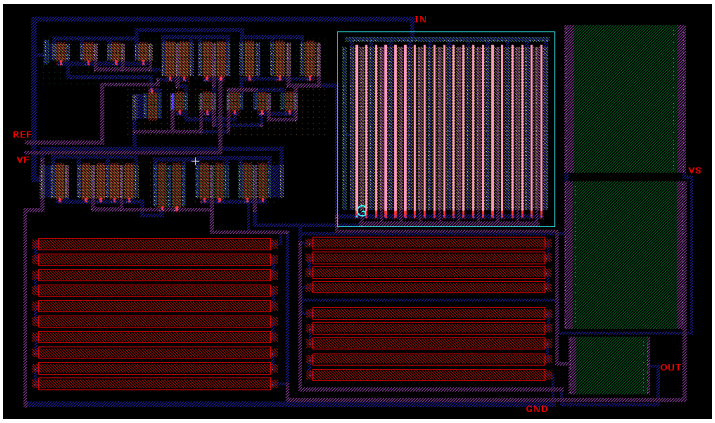

Fig. 20 Layout picture of the proposed LDO.

5 Conclusion

In this paper, a novel low dropout voltage regulator for hearing aid applications is presented. In the LDO design, only 4.5 pF on-chip capacitance is used and it does not require any off chip capacitor. Therefore, the area occupancy of the LDO is very less which is very much desired required feature in hearing aids. The new voltage suppressor block introduced in the LDO, helps to achieve a better transient response during abrupt load variations. All the major performance parameters of the proposed LDO are verified using post layout SPICE simulations. Also, the statistical analysis shows that the LDO is robust against process variations and local mismatch.

Intellectual Property

The authors confirm that they have given due consideration to the protection of intellectual property associated with this work and that there are no impediments to publication, including the timing to publication, with respect to intellectual property.

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Declaration of Competing Interest

The authors hereby confirm that the submitted manuscript is an original work and has not been published so far, is not under consideration for publication by any other journal and will not be submitted to any other journal until the decision will be made by this journal. All authors have approved the manuscript and agree with its submission to "Iranian Journal of Electrical and Electronic Engineering".

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