Integration of Quadrature Oscillator and Floating Inductor in FinFET Transistor Design: Innovations and Applications

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Abstract: In the past twenty years, low-voltage and power design have gained attention in analog VLSI design, particularly for high-performance and portable integrated circuits (ICs). Because of the increasing density of large-scale integration, a single silicon A.S.I. chip could have thousands or even millions of transistors on it. A rise in integration levels led to the development of Fin-type Field Effect Transistor (FinFETs) technology. In this research, an improved circuit design for a floating active inductor (FAI) and quadrature sinusoidal oscillator (QSO) is implemented employing only two active filters, the Z-copy-Voltage Differential Transimpedance Amplifier (Zc-VDTA). The purpose of the FAI is to contain two Zc-VDTA and one resistor with a ground capacitor, and it is easy to integrate the parameters of the Zc-VDTA bias current (IB) through the adjustment of the circuit. To verify the dependability of the circuits designed using floating active inductance circuits, a Butterworth fourth-order low-pass filter was created via component replacement. All the simulations have been carried out on 7 nm using linear technology SPICE, and cadence virtuoso tool.

1 Introduction

IN recent years, various application circuits have been centered on the construction of advanced analog circuit blocks. Quadrature sinusoidal oscillators (QSO) and floating active inductor (FAI) have been widely used in communication engineering, electronic instrumentation, and control systems. A Z-copy-voltage differential transconductance amplifier (Zc-VDTA) is a commonly used multi-function circuit block in analog signal processing circuits and analog waveform generation applications. Zc-VDTA is popular among applications due to its strong ability to adjust output current gain [1]. Zc-VDTA is an active building block

that may be used to electronically control transconductance gain and transmit voltage and current to their appropriate terminals. It can also be used to develop various kinds of active inductance simulators and through the usage of minimums [2-4]. General analog signal processing circuits and analog waveform generation circuits have the following shortcomings: lack of electronic adaptability; excessive use of passive components, especially external resistors; use of adjustable capacitors, which is not convenient for further integrated circuit manufacturing; oscillation frequency and oscillation conditions cannot be controlled independently [5]. Currently, various filter and QSO designs use circuit-building modules (such as Zc-CFTA, CCCDTA, M-VDTA CFA, CCC-II, etc.). This paper uses two VDTAs and two ground capacitors and ground resistors to design a new voltage-mode QSO. The design circuit uses Linear technology SPICE and Cadence simulation to verify the viability of the circuit. The simulation results show that the circuit has low power consumption and can achieve independent control of the oscillation frequency and oscillation conditions [6]. The Zc-VDTA modules used in the design circuit have oscillators, active floating inductors, that can present

different transconductance values. This is an advantage of the Zc-VDTA Filter. Another important feature of the Zc-VDTA Filter is that the voltage and current output terminals at the input end of the circuit can easily enter the transconduction application mode. The circuit designed in this paper uses a minimum number of passive and active components, and the circuit uses an additional VDTA filter, which can effectively control ω0[8-10].

2 Active Building Block (Zc-VDTA) Description

Much attention has been paid to Zc-VDTA as a VM active component because it is a flexible analogue active building block (AABB). In Figure 1, the schematic symbol for multioutput Zc-VDTA is displayed. The Zc-VDTA is composed of two transconductance amplifier subsections that operate independently of one another. content six terminals are divided into four output terminals, two input terminals DGNMOS(N) and DGPMOS(P), and all but the X terminal have a high input impedance. This means that the differential input voltage is converted by the first transconductance gain into a current at the terminals Z and Zc, and by the second transconductance gain into currents at the terminals ±Io.

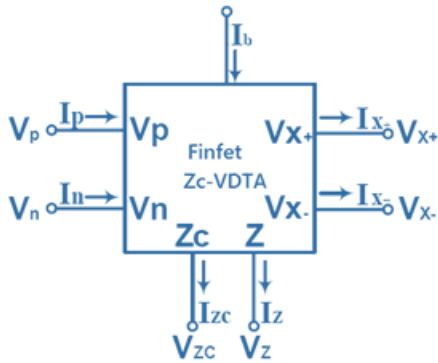**Fig. 1** The schematic symbol for Zc-VDTA.

Following is an illustration of the optimal Zc-VDTA matrix for port:

$$\begin{bmatrix} \mathbf{Ip} \\ \mathbf{In} \\ \mathbf{Iz} \\ \mathbf{Izc-} \\ \mathbf{Io+} \\ \mathbf{Io-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ gmx & -gmx & 0 & 0 & 0 & 0 \\ -gmx & gmx & gmy & 0 & 0 & 0 \\ 0 & 0 & -gmy & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \mathbf{Vp} \\ \mathbf{Vn} \\ \mathbf{Vz} \\ \mathbf{Vzc-} \\ \mathbf{Vo+} \\ \mathbf{V0-} \end{bmatrix} \tag{1}$$

The internal analog structure of Zc-VDTA is shown in Figure 2. The circuit uses two operation transconductance amplifiers. The input and output transconductance parameters of the Zc-VDTA circuit are determined by the transconductance of the output transistor, and can be expressed approximately as:

$$g_{m1} = \frac{g_1 g_2}{g_1 + g_2} + \frac{g_3 g_4}{g_3 + g_4} \cong (g_{1,2} + g_{3,4})/2 \tag{2}$$

$$g_{m2} = \frac{g_9 g_{10}}{g_9 + g_{10}} + \frac{g_{11} g_{12}}{g_{11} + g_{12}} \cong (g_{9,10} + g_{11,12})/2 \tag{3}$$
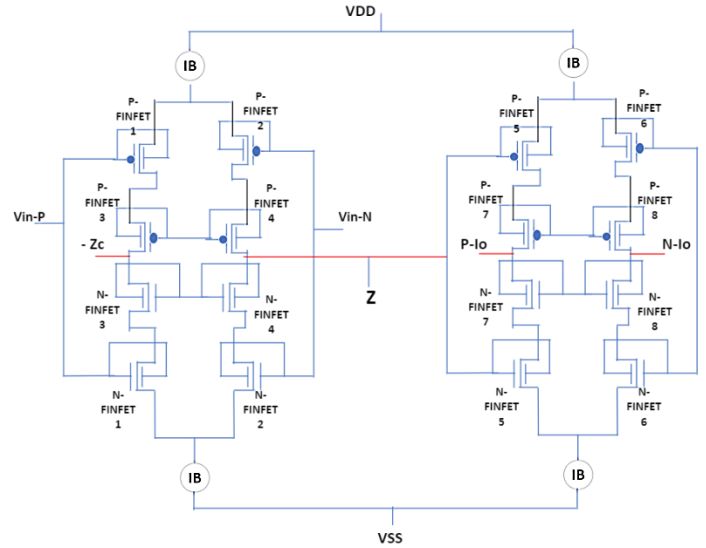

Fig. 2 Zc-VDTA internal simulation structure.

3 Voltage Mode Circuit Implementation

3.1 Quadrature Sinusoidal Oscillator (QSO) Circuit Design

VMSQO is designed by cascading an inverting second-order low-pass filter and a non-destructive integrator [5]. The purpose design circuit is shown in Figure 3. The characteristic equation of a QSO is obtained from the design circuit as shown in the equation.

$$s3 + a.s2 + b.s + c.k = 0 \tag{4}$$

and we have

$$c.k = a.b$$

then

$$w_0 = \sqrt{g_{m1}(g_{m2} + g_{m3})} \tag{5}$$

oscillation conditions are:

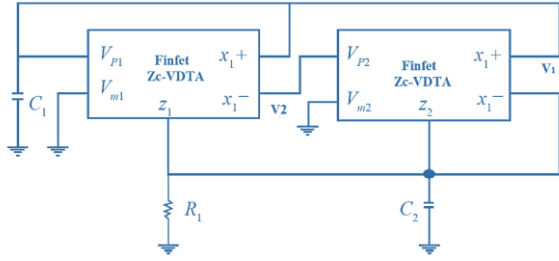$$\frac{(g_{m4} + g_{m2}) - 1}{R} \leq 0 \tag{6}$$

Fig. 3 VMSQO circuit designed using Zc-VDTA.

The oscillation frequency is regulated by gm1, which is independent of the oscillation circumstances, whereas R1, gm2, and gm4 can establish the oscillation conditions, as shown by Equations (5) and (6). The voltage transfer function is determined from Figure 3 as:

$$Av(s) = \frac{-(g_{m2} + g_{m4})}{s.C} \qquad (7)$$

3.2 Zc-VDTA Construction of Floating Inductance Simulator

Fig. 1 shows a floating inductance simulator that is based on Zc-VDTA in order to calculate inductance values. As shown in Figure 4, it uses two Zc-VDTA structures with one grounded capacitor and one grounded resistor in each. According to the drawing, the Zc-VDTA's P and -X terminals are grounded, as shown in the figure below, and the equation of active floating inductance is.

$$Lequ = \frac{C.R}{gm} \qquad (8)$$

The equation (8) is achieved by employing electrical tuning techniques. Practically, achieving gm1 = gm2 = gm can be readily done without the need to match the external passive components of Zc-VDTA. This can be accomplished by setting the two bias currents (I_B) equal.
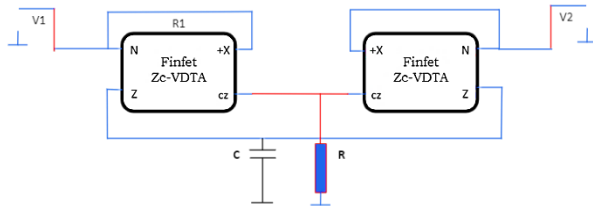

Fig. 4 Schematic for Zc-VDTA-based floating active inductance simulation.

3.3 Butterworth Filter Ladder, Fourth-Order Low Pass

A passive prototype of the fourth-order Low Pass Butterworth ladder filter is seen in Figure 5. This circuit uses a floating inductor, which can be swapped out for a simulated active inductance. The simulated active floating inductance based on Zc-VDTA is displayed in

Fig. 6, which is utilized in the fourth-order LPF design. The fourth-order low pass Butterworth filter's transfer function is provided by

$$\frac{Vo}{Vin} = \cfrac{\cfrac{1}{L_1.L_2.C_1.C_2}}{\begin{aligned} & S^4 + S^3.(\frac{R_S}{L_1} + \frac{1}{R_L.C_4}) + \\ & S^2.(\frac{1}{L_1.C_3} + \frac{1}{L_1.C_3} + \frac{1}{L_1.C_3} + \frac{R_S}{R_L.C_4.L_1}) + \\ & S(\frac{1}{L_1.R_L.C_4.C_3} + \frac{R_S}{L_1.L_2.C_4} + \frac{1}{L_2.R_L.C_4.C_3} + \frac{R_S}{L_2.C_3.L_1}) + \\ & (\frac{1}{L_1.L_2.C_1.C_2} + \frac{R_S}{L_1.L_2.C_3.C_4.R_L}) \end{aligned}} \qquad (9)$$

assume that the $L_1 = R_1 C_1 / g_{m1}$ with $L_2 = R_2 C_2 / g_{m2}$ and the g_{m1}, g_{m2} are the transconductance of the active elements.
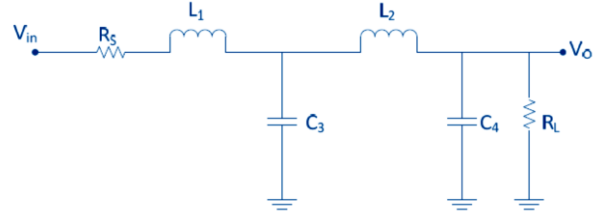

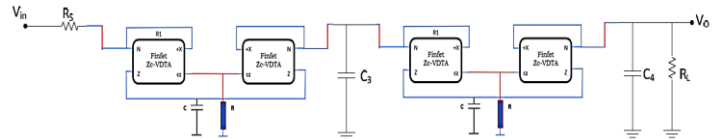**Fig. 5** Passive prototype of a fourth-order Butterworth low-pass filter.

Fig. 6 Zc-VDTA-based floating active inductor simulator.

4 Analyzing Zc-VDTA's Sensitivities.

In a perfect Zc-VDTA in Figure 7, all input and output ports (P, N, Z +, Z-, X+, X-) have an infinitely high resistance. In practice, the resistors for VDTA have specific finite values that vary according on the device characteristics. Additionally, it is necessary to consider high-frequency effects, while assuming the existence of parasitic capacitances in these ports. Thus, a functional Voltage-Mode Z Copy-Differential Transconductance Amplifier (Zc-VDTA), depicted in Figure 5.5, demonstrates the diverse range of parasitic ports. The port interferences occur in the form of Rp//Cp at port P, RN//CN at point N, RZ//CZ at port Z, RZ-//CZ- at port Z, RX±//CX± at port X±. These interferences are frequency dependent and are particularly prominent at high operating frequencies. They can significantly degrade desirable performances. To minimize the impact of port interference on circuit performance, it is advisable to employ a well-designed Zc-VDTA topology that includes matched transistor arrays, matching current mirrors, and an adequate number of external passive components for circuit synthesis.

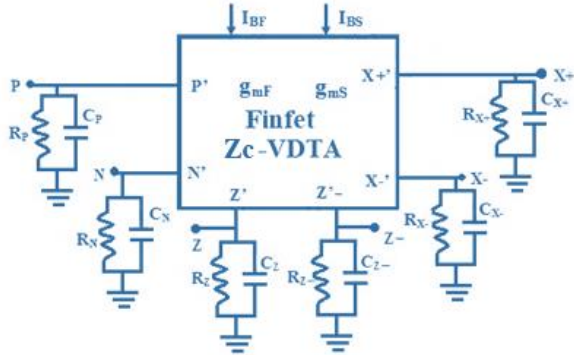$$S_{gm1,gm2}^{wo} = 0, S_R^{wo} = 0, S_{C1,C2}^{wo} = 0.5 \qquad (10)$$

Fig. 7 The non-ideal equivalent circuit of the Zc-VDTA.

As can be seen from the various sensitivity coefficients, all active and passive components in the system have low sensitivity and have little effect on ω_0.

5 Simulation Results of the Proposed Quadrature Sinusoidal Oscillator (QSO) and Floating Active Inductance(FAI) Configurations

To evaluate the performance of the quadrature sinusoidal oscillator (QSO) oscillator, developed as depicted in Figure 3, it was simulated using the Cadence Virtuoso tool and Linear Technology SPICE. The DGPMOS and DGNMOS transistors were simulated utilizing the specific specifications of the 7 nm Finfet technology. The circuit operates with a power supply voltage and a bias voltage of Vss=VDD = ± 0.1 V. The transconductance value of Zc-VDTA is gm1=gm2= 11nA/V. The current flowing into the base is 172 nanoamperes. Furthermore, the circuit employs a capacitance value of C1=0.1nF and a resistance value of R1=1kΩ. Figure 8 illustrates the time domain response of the circuit utilizing the Zc-VDTA. The circuit demonstrates stable functioning, with an oscillation frequency of f0 = 16.23 M.

In order to verify the theoretical predictions, the suggested floating active inductance circuits are simulated using Cadence tools and LT-SPICE. The schematic of Zc-VDTA, as shown in Figure 2, is utilized for this purpose. A DC supply voltage of 0.1 V is utilized. The bias current values for all simulations are consistently IB = 172 nA. The obtained transient responses from the simulated floating active inductors. The circuit's impedances, relative to frequency, are displayed in Figure 9 and compared to those of an ideal floating inductor. It is evident that the circuit is capable of functioning at frequencies of many megahertz.

The proposed floating active inductor was utilized to simulate several applications, such as a fourth-order Butterworth low-pass filter. The circuits have undergone simulation using Cadence tools and LT-spice. Figure 6 depicts a fourth-order Butterworth low-pass filter with passive RLC components.

After the process of scaling, the values of the individual components are C1=C3=0.01 microfarads and C2 = 0.05 microfarads, Rs=R_L=10K and the value of floating passive inductance 0.41Henry. The capacitance needed for the floating active inductance block is 3 nanofarads. The magnitude response of the circuit under consideration is illustrated in Figure 10.
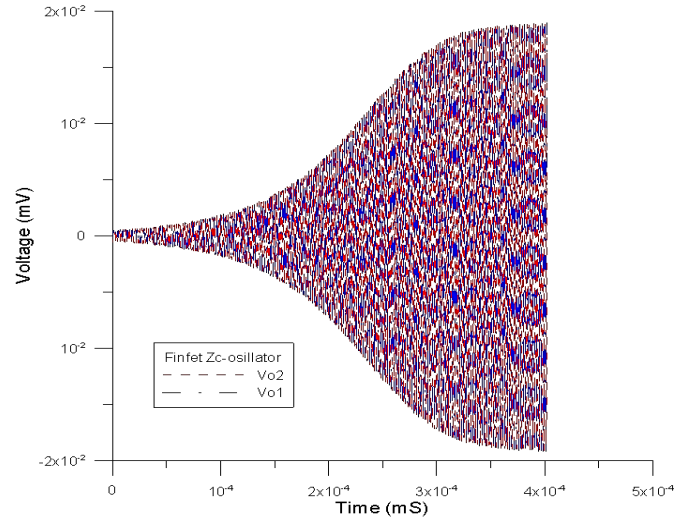

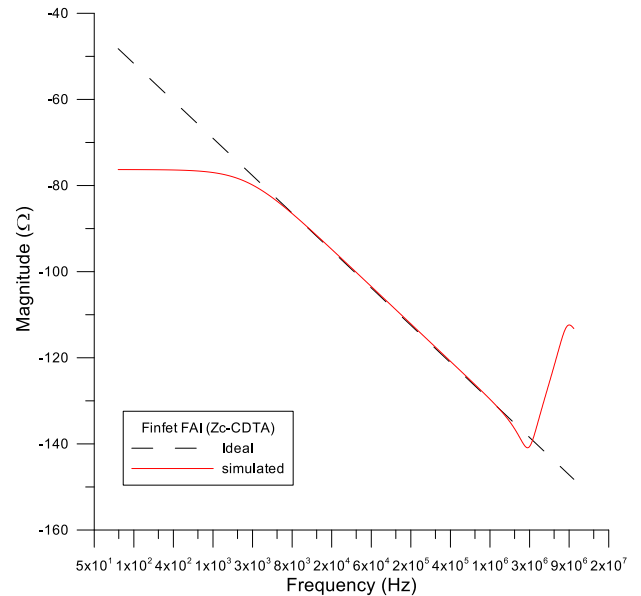**Fig. 8** illustrates the time domain response of the circuit utilizing the Zc-VDTA.

Fig. 9 Zc-VDTA simulation of the ideal and experimental floating active inductor frequency response.
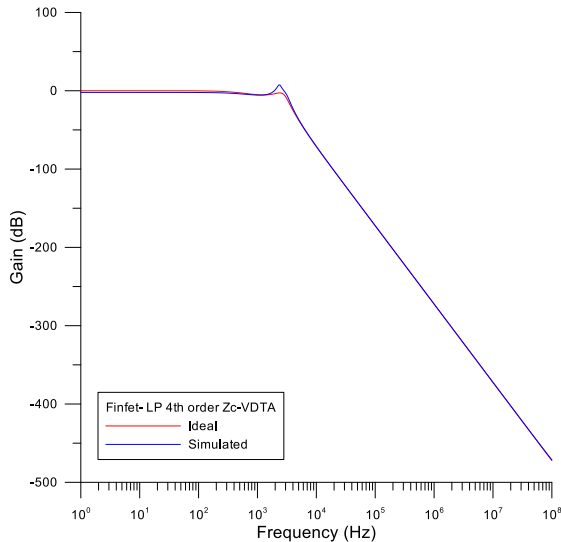
Fig. 10 The fourth-order low-pass filter's ideal and simulated gain responses are shown in Fig. 6.

6 Conclusion

This study introduces the unique quadrature sinusoidal oscillator and floating active inductors with electronic controlled using two Zc-VDTA designed with a Finfet transistor. Bias current (IB) values provide a simple and broad tuning mechanism for the proposed quadrature sinusoidal oscillator and active inductors.

Both active and passive circuit simulation findings correspond to a broad spectrum of operation. The 4th order Butterworth low-pass filter was built using the suggested inductors. In this study, a novel voltage mode quadrature sinusoidal oscillator is designed by using a Zc-VDTA. Two voltages differential transconduction amplifiers, two ground capacitors, and two ground resistors are all part of the design circuit. Cadence virtuoso tools and LT-PSPICE with a 7 nm transistor parameter are utilized for Finfet transistor simulation to validate its fundamental performance. The simulation results demonstrate that the circuit has strong electrical controllability, high bandwidth, low power supply voltage, low design cost, and stable operation. It also performs well.

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