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Design and Performance Optimization of a Bi-Channel Ge-GaAs Vertical Tunnel Field Effect Transistor with High Switching Speed and Improved Tunneling Rate

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Abstract: In this paper, an innovative vertical bi-channel tunnel field effect transistor is presented that exploits line tunneling mechanism to achieve improved electrical performance. In this device, the source contains germanium, while the channel and drain regions consist of GaAs., which results in a type-II heterostructure with low resistance tunneling barrier. The source region is situated in a vertical position, enclosed by two sidewall channels that encompass a broad area of tunneling. Our proposed design effectively blocks the electric field that is originated from the drain at the tunneling junction, thereby conferring high immunity to drain induced barrier thinning effect. The device that has been suggested offers a significantly greater on-state current, a factor of 144, when compared to the traditional TFET and provides a subthreshold swing of 3mV/dec and an on/off current ratio of 9.76×10^{10}. According to statistical analysis, the design parameters of metal gate workfunction value and source doping concentration are crucial and have the potential to impact device performance. Therefore, selecting the appropriate combination of these parameters is essential. The proposed device serves as a foundation for the development of computing systems that are low in power and high in speed.

Keywords: Band to Band Tunneling, Gate Workfunction, Heterojnction, Line Tunneling, Tunnel Field Effect Transistor.

1 Introduction

THE dimensions of traditional metal-oxide-semiconductor field-effect transistor (MOSFET) are continuously being reduced in order to fulfill the ever-increasing demands of low cost, low power, efficient integrated circuits with versatile functionality. However, the reduction in size of the device below 100nm is an arduous task due to the emergence of short channel effects, which ultimately impairs the device performance. According to the Boltzmann limit, a minimum subthreshold swing of 60 mV/dec can be attained at room temperature, but this capability can be significantly diminished in the nanoscale regime [1-2]. The tunnel field effect transistor (TFET) is a promising option for low supply voltage digital logic circuits due to its ability to achieve subthreshold swing values lower than 60 mV/dec over a given gate voltage swing compared to MOSFETs, thanks to the band to band tunneling current mechanism [3-6]. However, conventional TFETs rely on a limited point tunneling mechanism located at the boundary between the source and channel regions, resulting in low tunneling current. To enhance device performance, various techniques such as material engineering, geometry engineering, and doping engineering are being employed. The utilization of a line tunneling mechanism has been proposed as an effective technique for

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amplifying the tunneling window in different structures such as F-shaped [7-8], L-shaped [9-12], and electron hole bilayer TFET [13-16], vertical TFET [17] where a broader tunneling junction is provided at the source and channel region interface.

This paper introduces a new TFET structure that implements line tunneling in two side wall parallel channels. The proposed bi-channel vertical tunnel field effect transistor features an improved tunneling rate and high drive current, making it a promising candidate for future devices. Furthermore, the utilization of Ge-GaAs as a material combination at the source and channel region interface results in a substantial enhancement of device performance with regards to on/off current ratio, subthreshold, and ambipolarity. A comprehensive investigation into the influence of critical parameters on device performance has been conducted, and statistical analysis has been employed to determine the sensitivity of the device primary electrical measures to variations in fundamental design parameters.

2 Operation Principle and Simulation Methodology of the Device

The illustration in Fig.1 depicts the 2D schematics of the Bi-Channel Vertical Tunnel Field Effect Transistor (BCVTFET). The material combination utilized at the tunneling junction comprises of low band gap germanium in the source region and wide band gap GaAs in the sidewall channels as well as the drain regions. The proposed heterojunction structure offers a solution to the issues associated with TFET, particularly the low on-state current, by providing a narrower tunneling barrier width. Additionally, the use of wide band gap channel and drain material significantly mitigates the ambipolar behavior. The creation of two parallel channels at the source sidewalls results in a wide tunneling junction based on line tunneling phenomena, leading to substantial improvement of the on-state current when compared to the point tunneling conventional TFET. The interposed oxide region, situated amidst the upper facade of the source and drain, confers notable resistance to abbreviated channel effects, namely the drain-induced source tunneling effect. The primary design parameters are expounded upon in Table 1. The numerical simulations are executed through employment of the ATLAS device simulator [18], whereby the ensuing models are enabled to facilitate proficient appraisal of the device: (a) Nonlocal Band to Band Tunneling: The fundamental process that governs the operation in the BCVTFET is band to band tunneling, where carriers tunnel through a gate modulated tunneling barrier. A significant band bending occurs as the gate bias increases, resulting in an increase in the electric field at the interface of the source and channel junction. Therefore, the conduction band within the channel intersects with the valence band located in the source, allowing tunneling transitions between these two bands to become available. (b) Trap Assisted Tunneling: Trap-assisted tunneling is characterized as the generation of band to band tunneling current through the contribution of phonons. Essentially, trap assisted tunneling causes a leakage current prior to the onset of band to band tunneling, which significantly degrades the subthreshold swing in BCVTFET. In order to effectively evaluate the device's performance, the activation of Shockley-Read-Hall (SRH) generation/recombination models and trap-assisted tunneling models is essential. (c) The carrier mobility in response to the lateral and vertical electric field as well as the carrier concentration is analyzed within the framework of mobility models. (d) The Band Gap Narrowing Model, which is based on the Wentzel-Kramers-Brillouin (WKB) approximation [19,20], modifies the tunneling rate based on the band gap energy. Experimental observations reveal that a shrinkage of the bandgap occurs at high impurity concentrations, a phenomenon attributed to the inclusion of a heavily doped regions [21-23]. Given the heavily doped nature of the source region and the application of the WKB approximation, the band gap assumes a crucial role as a fundamental design parameter in determining the tunneling probability. Consequently, the band gap narrowing model is activated within the simulator to account for this phenomenon. (e) The Quantum Confinement Models account for the energy band formation and the reduction in density of states in thin film channels due to the quantum confinement effects. The drain current computation incorporates this effect. The manufacturing procedure for the device that is compatible with the proposed Si-based device in [24] can be summarized as follows: initially, the substrate material is coated with the source electrode using sputtering. Subsequently, a Ge layer is grown using an epitaxial process to establish the vertical structure. This is followed by the creation of a p^+ Ge layer through ion implantation. Then, an insulating SiO_2 region is formed using epitaxial growth to insulate the source and drain regions. After the epitaxial layer has been grown, the vertical GaAs active layers and drain region are patterned using i-line photolithography. The vertical structure is then formed through selective epitaxial growth. Next, the doping process is carried out via ion implantation to generate the n+ drain region. Once the gate dielectric, HfO_2, is created using atomic layer deposition, NH_3 plasma treatment is performed to generate an HfON interfacial layer. The HfON interfacial layer exhibits excellent interface properties and a higher permittivity. Finally, the sidewall gate electrodes and drain electrodes are fabricated using sputtering.

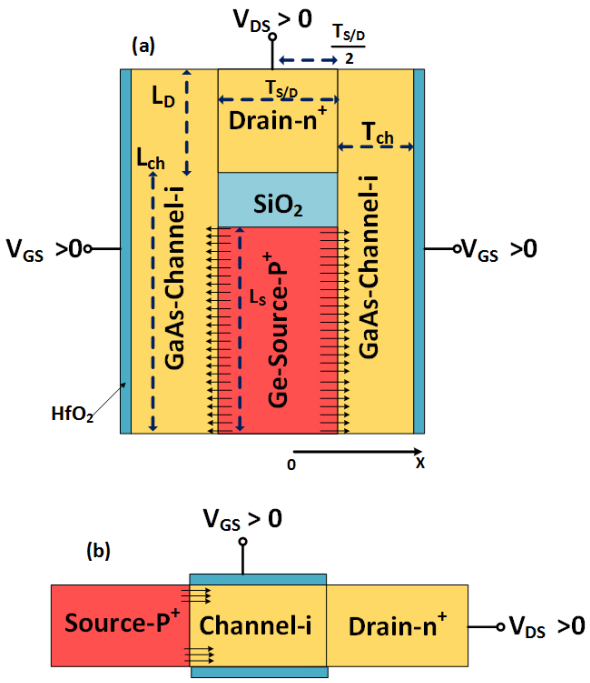

Fig. 1 2D schematics of (a) BCVTFET with two sidewall channels exploiting line tunneling mechanism, and (b) conventional heterojunction double gate lateral TFET.

Table 1 Initial design parameters for the BCVTFET and conventional TFET.

Parameters	BCVTFET	Conventional TFET
Channel Length (Lch)	60 nm	60 nm
Source vertical length(L_s)	30 nm	-
Channel thickness (T_{ch})	5 nm	5nm
Gate insulator thickness-HfO_2	2 nm	2 nm
Source and Drain doping density	5×10^{19} (cm^{-3})	5×10^{19} (cm^{-3})
Channel doping density	intrinsic	intrinsic
Gate Work Function (WF)	4.2eV	4.2eV
Source and Drain thickness	5 nm	5 nm
Vertical length of SiO_2	10 nm	-

3 Results and discussions

The energy band diagram of the proposed BCVTFET is depicted in Fig. 2, for both the off-state and on-state conditions. The operation of the BCVTFET primarily revolves around the control of the rate at which electrons tunnel from one energy band to another, specifically between the source and channel regions. This control is achieved by utilizing gate electrodes positioned along the sidewalls. Under off-state conditions (V_{GS}=0V, V_{DS}=1V), the width of the potential barrier between the peak of the valence band in the source and the lowest point of the conduction band in the channel is not narrow enough to produce a window of energy suitable for tunneling. As a result, the process of tunneling from one band to another is precluded, thereby limiting the occurrence of band to band tunneling. Consequently, the reverse leakage current of the p-i-n structure is solely influenced by the minority carriers, specifically trap assisted tunneling and the generation/recombination mechanism known as Shockley-Read-Hall (SRH). In the on-state (V_{GS}=1V, V_{DS}=1V), an increase in the gate bias towards highly positive values leads to a reduction in the width of the potential barrier between the region where the source is located and the channel region. As a result, a substantial band to band tunneling current is permitted. The application of gate bias induces a downward shift in the energy bands of the channel, leading to the synchronization of the conduction band in the channel region with the valence band of the source. This synchronization promotes the occurrence of direct tunneling carrier transition. The findings reveal that the energy band profile of the tunneling junction exhibit type-II heterojunction features, which can potentially serve as a low resistance tunneling barrier.

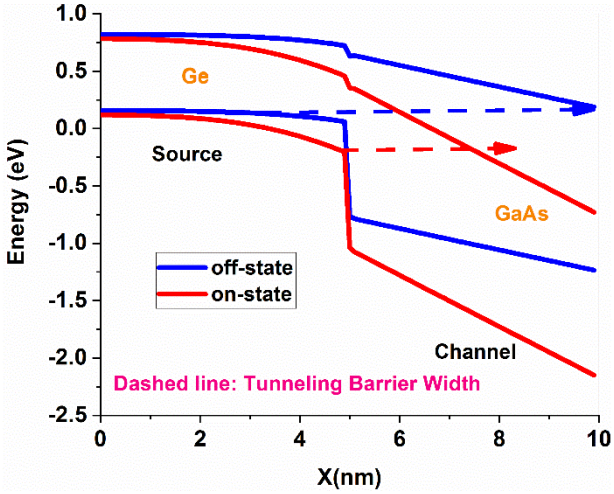

Fig. 2 Energy band profile of a BCVTFET in the off-state and on-state from source to channel.

The electron and hole density of BCVTFET, corresponding to the off-mode and on-mode, are depicted in Fig.3, with a lateral direction extending from the source to the channel. A prominent feature of this device is an abrupt p^+n^+ doping profile at the tunneling junction, which is critical. To reduce the width of the electrostatic potential barrier, the intrinsic channel region must be converted electrically into a heavily doped region. In the

off-state, the electron density in the channel is insufficient to minimize the space charge region at the source and channel interface. However, in the on-state, the electron density in the channel increases, causing the energy of subbands for holes and electrons to align.

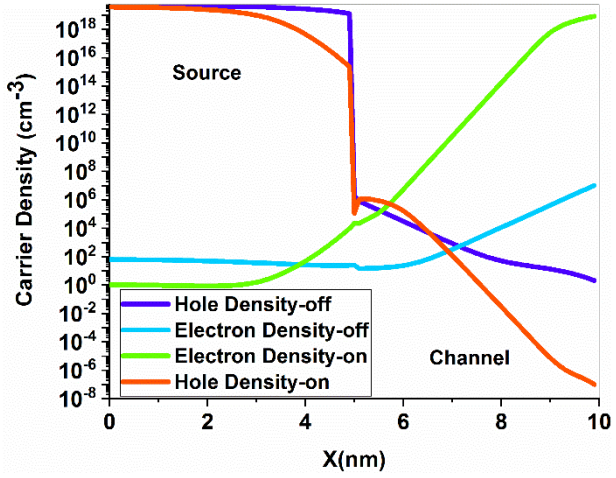

Fig. 3 Electron and hole density in the off-mode and on-mode as they traverse along the lateral direction starting from the source and moving towards the channel.

Figure. 4 presents a comparison between the simulated transfer characteristics of conventional lateral heterojunction TFET and BCVTFET. One of the primary limitations of the conventional TFET is that tunneling only occurs in a restricted region at the interface between the source and channel regions near the top and bottom gate oxide. To address this limitation and enhance the tunneling rate, a proposed vertical structure extends the interface between the source and channel regions. This extension increases the tunneling area. Additionally, the inclusion of two side wall gates enables tunneling along the vertical length of the source region on both the right and left sides. Furthermore, since the gate electrode completely covers the vertical length of the source, the required gate bias for the onset of tunneling decreases. The analysis indicates that BCVTFET exhibits a step-like behavior in its drain current profile. The threshold voltage of the device is specifically determined as the required gate voltage for the bands overlap, or in other words, the voltage necessary for the device to transition from a low off-state drain current to high conductance. Essentially, a 2D quantum well structure is established between the sidewall gate insulators and the source region. In this particular case, a significant number of states are aligned to contribute to band-to-band tunneling when a positive gate bias is applied, leading to a steep switching behavior that is highly satisfactory. The electrical properties of the devices being examined are condensed and presented in Table 2. The results demonstrate that the BCVTFET device has been able to achieve a higher on-state drive current (144 times higher than the conventional TFET) and improved switching speed due to the presence of sidewall parallel channels and a large source and channel overlap area for tunneling transmission, as compared to conventional lateral TFET. It is important to mention that the calculation of subthreshold swing is based on the maximum slope of the transfer characteristic. In the alternative method, the average subthreshold swing is determined by measuring the voltage variation required for a 1×10^{6} increment in the drain current from the minimum off-state current. As a result, the BCVTFET achieves an average subthreshold swing of 12 mV/dec, compared to 40 mV/dec for the conventional TFET.

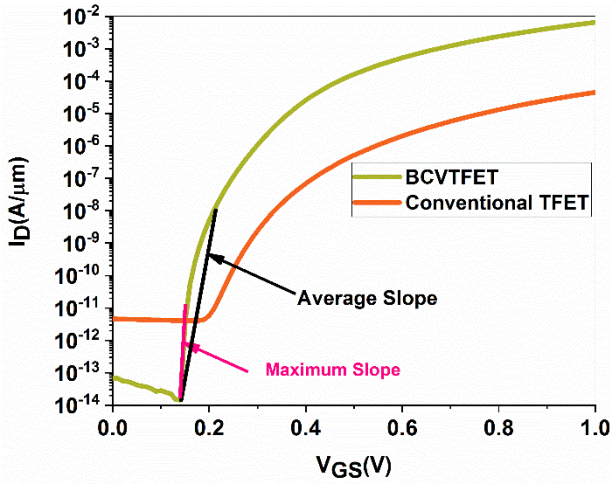

Fig. 4 I_D-V_{GS} curves of BCVTFET and conventional lateral TFET.

Table 1 Main electrical parameters of BCVTFET and conventional TFET.

Electrical Parameter	BCVTFET	Conventional TFET
I_{on} (A/μm)	6.53×10^{-3}	4.52×10^{-5}
I_{off} (A/μm)	6.69×10^{-14}	4.62×10^{-12}
V_{th} (V)	0.15	0.22
SS-Maximum Slope (mV/dec)	3	15
SS-Average Slope (mV/dec)	12	40
I_{on}/I_{off}	9.76×10^{10}	9.78×10^{6}

The impact of gate workfunction on the transfer characteristics of BCVTFET is illustrated in Fig.5. The role of the gate workfunction in controlling the charge density within the channel and its ability to modify the rate of tunneling is clearly evident. As the gate workfunction increases, the threshold voltage, which is the minimum gate bias required for tunneling onset, shifts

to higher positive values. Essentially, the optimal value can be identified as the lowest attainable positive bias for the current transition from the off-state to the on-state. label axes only with units. Source doping is a crucial factor in designing devices that can effectively control the tunneling rate.

The impact of source doping on the transfer characteristics of the device is depicted in Fig.6. The width of the depletion region at the source and channel p^+-n^+ junction is inversely proportional to the doping concentration of the n and p sides, which can be observed qualitatively. A source region that has been doped to a significant extent significantly reduces the tunneling barrier width, leading to an amplified electric field at the tunneling interface. This, in turn, results in an increasing band bending at the source and channel junction, thereby improving the tunneling current.

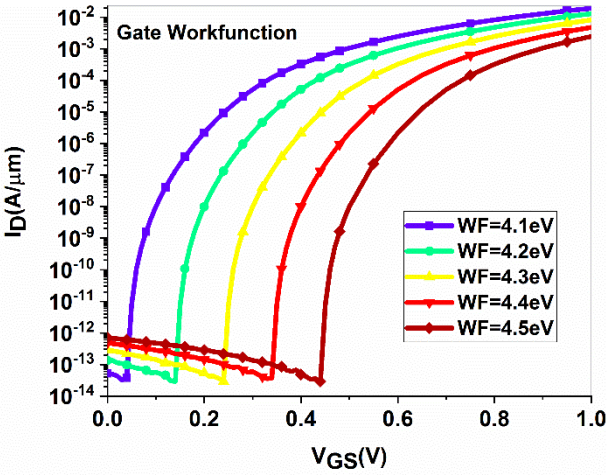

Fig. 5 Transfer characteristics of BCVTFET as the gate workfunction value is changed.

The predominant characteristic of the proposed BCVTFET is its improved line tunneling window, which effectively enhances the on-state current. Figure.7 illustrates the on-mode and off-mode current of the proposed device concerning the vertical length of the source region. It is noteworthy that the on-mode current increases as the source length increases. Furthermore, minimal fluctuations in the off-mode current are discernible. Figure.8 displays the effect of drain bias fluctuations on the main electrical characteristics of the BCVTFET. The key attribute of the suggested device is the lack of sensitivity of the threshold voltage and the negligible variation of the off-state current to the drain bias fluctuations, which proves the device practicality for nanoscale applications. It is apparent that an increase in drain bias leads to an elevation in carrier velocity and, therefore, an improvement in the on-state current. Basically, the embedded insulator between the drain region and top side of the source region blocks the effect of the drain electric field on the tunneling junction, which eventually diminish DIST effect.

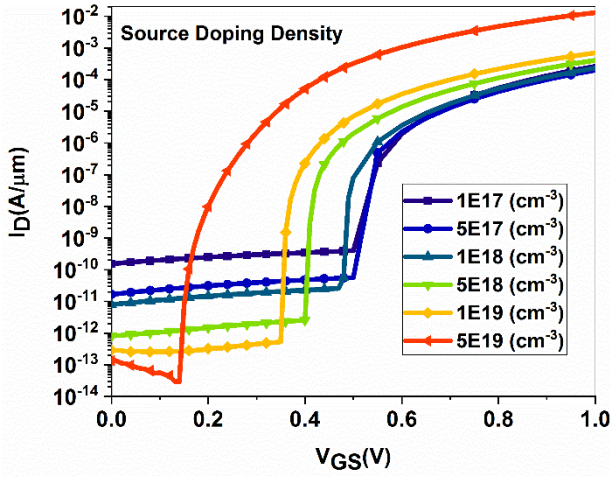

Fig. 6 The effect of source doping density on the transfer characteristics of the BCVTFET.

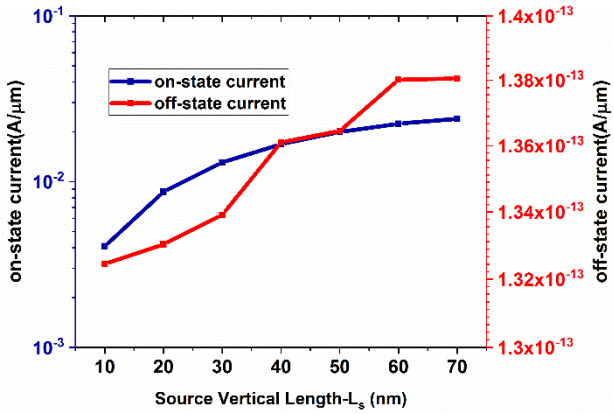

Fig. 7 On-state current and off-state current of the BCVTFET as the source vertical length is parametrized.

Temperature is an essential factor in the physical design of devices as it can significantly impact their performance. In Fig.9, the on-state and off-state variation of the BCVTFET is illustrated as the temperature changes. The findings reveal that the off-state current is greatly influenced by temperature fluctuations, primarily due to the minority carrier originating from the source region. Specifically, the density of minority electrons in the source region increases particularly at elevated temperatures, leading to a notable degradation in the average subthreshold swing. However, due to the dominant role of lateral gate electric field, the maximum on-state current remains largely unaffected by temperature changes.

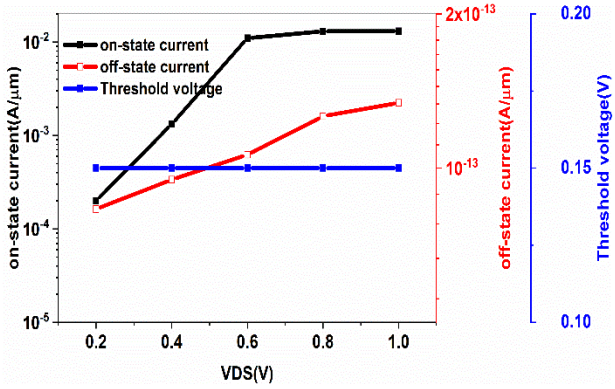

Fig. 8 On-state current, off-state current and threshold voltage of the BCVTFET as the drain bias is varied.

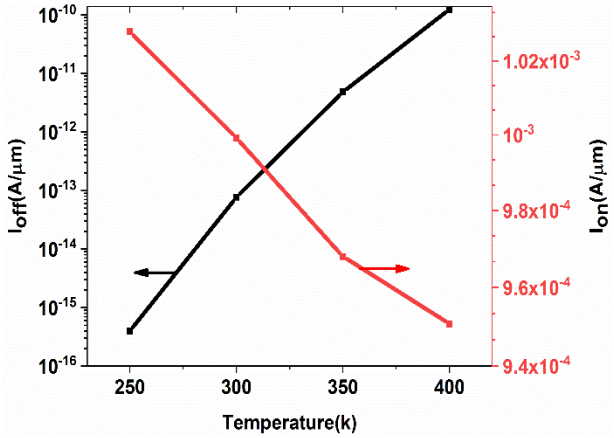

Fig. 9 Impact of temperature on the off-state and on-state current of the DCVTFET.

Figure.10 depicts the sensitivity of the primary electrical parameters of BCVTFET concerning the alterations in vital physical and structural design factors. Sensitivity, expressed as the coefficient of variation (CV) in percentile, is a statistical metric that represents the ratio of the standard deviation (σ) to the mean value (μ). A higher sensitivity suggests a greater vulnerability of the device's electrical parameters to the specific design measure

$$CV=\sigma/\mu\times100\% \quad (1)$$

The study reveals that source doping is a crucial element in the design process that can effectively manipulate the width of the tunneling barrier, thus affecting the electrical properties of the device. Essentially, the density of holes in the source region is responsible for the steepness of the bands at the source/channel junction. A heavily doped source region can facilitate a higher tunneling generation rate of charge carriers at this interface, thereby overcoming the issue of low on-state current. However, a lower doped source region can lead to an increase in the parasitic series resistance and off-state current related to the minority carriers, which can eventually compromise the device performance. Furthermore, the workfunction of the gate serves as yet another crucial parameter in the design process that can influence the channel charge density and play a major role in the device's primary electrical properties.

The determination of optimal values for both source doping density and gate workfunction is essential. The source vertical length serves as a crucial parameter in the device design process, as it impacts the tunneling area. The proposed device exploits a line tunneling mechanism that effectively improves the tunneling rate. Notably, the device exhibits insensitivity of threshold voltage and subthreshold swing to drain bias variation, making it applicable in the nanoscale regime. Temperature is a physical parameter of great importance, as it can affect the energy gap of the semiconductor and subsequently the tunneling mechanism of the BCVTFET. Additionally, temperature can impact the SRH generation/recombination mechanism and the density of source minority carriers. A comprehensive spectrum of temperature ranging from 200K to 400K has been employed to scrutinize the electrical properties of the apparatus. The investigation revealed that the tunneling rate can be substantially altered by trap assisted tunneling, which in turn plays a pivotal role in the occurrence of significant leakage current pathway prior to the initiation of band to band tunneling.

4 Conclusion

The study comprehensively investigates the electrical characteristics of a heterojunction vertical TFET utilizing line tunneling mechanism. The device displays superior tunneling rate compared to conventional TFET, making it a potential candidate for digital circuits that operate at high speeds and consume low amounts of power. The findings indicate that the on-state performance of the suggested dual channel structure surpasses that of the conventional TFET by a factor of 144. Furthermore, it is evident that an average subthreshold swing of 12 mV/dec is attained, resulting in enhanced switching speed. Statistical analysis evaluates the sensitivity of the device important electrical measures to critical design parameters variation. Results reveal the fundamental role of source doping density and gate workfunction in device performance. The findings indicate that a gate workfunction of 4.1 eV and a source doping density exceeding 1×10^{19} cm^{-3} result in a high tunneling rate while necessitating a low gate bias. Hence, an appropriate combination of optimized metal gate workfunction and source doping density can facilitate this device operation as an efficient high-speed switch in the nanoscale regime.

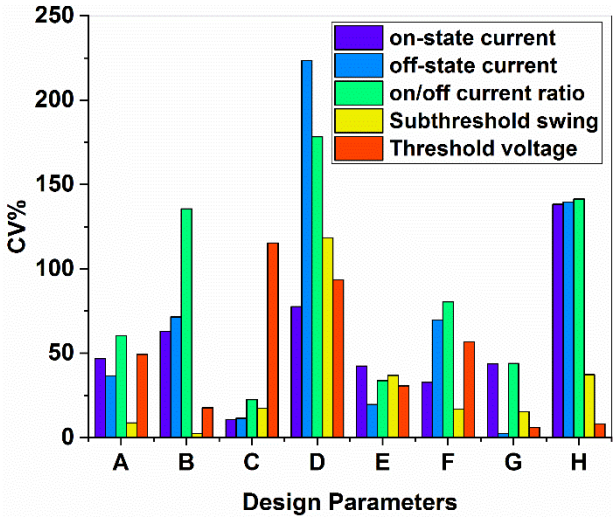

Fig. 10 Sensitivity of the BCVTFET primary electrical metrics change according to the fluctuation of numerous essential design factors.: A: Drain bias, B: Gate workfunction, C: Channel doping density, D: Source doping density, E: Channel thickness, F: Gate insulator thickness, G: Source vertical length, H: Temperature.

Conflict of Interest

The author declares no conflict of interest.

Author Contributions

Zahra Ahangari performed the simulation, assessed the outcomes, and composed the ultimate draft of the paper.

Informed Consent Statement

Not applicable.

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