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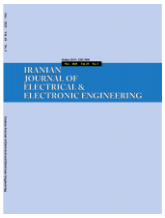

NCFET based, Non-Volatile and Radiation-Hardened Flip Flop with Simultaneous Backup Capability for Non-volatile/ Normally-Off Computing

V. Jamshidi *(C.A.) and M. M. Bordbar *

Abstract: Nonvolatile computing have been shown to be effective in the face of the sudden power outage for wireless sensor networks, Internet-of-Things applications, data converters, and emerging energy-harvesting circuits. It also plays a significant role in power-gating to minimize the leakage power for improving the energy efficiency. However, using on-chip backup module for D flip–flop has a bottleneck, and result in an increase in total power consumption, occupied area, and reduced calculation speed. Furthermore, the backup module needs external control signals, which increases the complexity of the circuit. This paper proposes a novel nonvolatile flip-flop with simultaneous data backup capability, which uses NCFET ferroelectric transistor to fundamentally advance the non-volatile computing paradigm. Proposed NVFF exhibits 0.8% faster and 5.0% smaller energy than previous works, while uniquely providing Radiation-Hardened feature.

Keywords: Data backup, ferroelectric transistor, hysteresis, non-volatility, non-volatile flip-flop, data restore.

1 Introduction

THE Future computing systems face three fundamental challenges which are: a) Data loss: A computing system loses its computing data when the power supply voltage is unexpectedly interrupted. b) Delay and energy consumption: unexpected supply voltage interruption, due to redoing the calculation have a drastic impact on the calculation time and total energy consumption. c) Implementing the power-gating technique: Implementing the power-gating technique in these systems to remove the leakage power incurs significant energy overhead costs and delay, as the data must be stored in an external non-volatile memory.

Power consumption is a parameter that has become a critical issue in many electronic circuits, especially in very large-scale integrated circuits (VLSI). One of the ways to reduce power consumption is to use the power gating technique. The power-gating technique on VLSI computing systems (e.g., high-performance cloud server centers and low-power portable devices) zeroes out the static leakage power. In the pipeline system, the states of registers and flip-flops must be backed up so that the stored data is not lost in the event of a voltage source outage. Similarly, battery-free portable devices with energy-harvesting techniques can profit from restore and backup operation, because ambient energy sources like vibrations, piezoelectric, photovoltaic, and radio frequency are reliable [1]–[8]. The outages of the voltage source have a drastic impact on the calculation time and energy consumption of the entire Internet of Things network [4]–[8]. On the one hand, in a computing system, if the data is not successfully backed up before the outage of power supply voltage, the system will lose its computing data. On the other hand, even if check-pointing and Rollback-Restore techniques are used significant energy overheads and delays will be incurred for each backup and restore operation. If backup data is stored in external non-volatile memory, it causes a lot of energy and delays to transfer data from

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that memory to the desired circuit. Non-volatile/Normally-off computing (NoC) is one of the promising power-saving techniques which can decrease power consumption more than low-power techniques like clock gating, power gating, dynamic voltage, and frequency scaling. The NoC provides zero standby leakage power consumption and instant-on properties [9], which are commonly utilized in many long-term sleep applications, such as wearable biosensors for healthcare, wireless sensor nodes for IoT, and energy harvesting embedded systems.

Fig. 1 shows the structure of conventional power gating (Fig. 1(a)) and normally-off computing (Fig. 1(b)). Implementing conventional power gating in digital systems faces many challenges. The first challenge is how to mitigate the delay, energy, and high peak power of a restore and backup operation. The second challenge is how to perform restore and backup control for distributed NV-devices, and how to organize backup and restore policy [1]. Providing this control action results in more area, wiring, and power consumption.

Recently, non-volatile flip-flops have been proposed to overcome these challenges for non-volatile computing systems [10]–[13]. In these circuits, components are used that retain their data when the supply voltage is shut down. Therefore, by connecting the power supply, you can perform data restoration. With this solution, the decrease in calculation speed and the increase in total energy consumption are prevented. Also, when the circuit is in a static state, its supply voltage can be shut down so that the leakage power becomes almost zero. In addition, the implementation of the power-gating technique will be inexpensive because there is no need for external nonvolatile memory. The use of non-volatile elements has made them very attractive to designers for normally off applications (e.g. [14], [15]). Among these elements, we can mention NCFET, FEFET, MTJ, etc.

Among the non-volatile elements, NCFET transistors have many desirable features such as small dimensions, static power consumption close to zero, high speed, nonvolatile, resistance to energetic particles, and compatibility with semiconductor devices [16]. The above advantages make it possible to achieve low-power non-volatile flip-flop designs. However existing NCFET based on non-volatile flip-flops has several important drawbacks. This paper proposes a new non-volatile flip-flop that not only provides high-speed data transfer but also reduces the area and power consumption compared to previous non-volatile flip-flops. In addition, the proposed flip-flop performs the backup operation simultaneously. Proposed NVFF exhibits 0.8% faster and 5.0% smaller energy than previous works, while uniquely providing Radiation-Hardened feature.

The rest of the paper is organized as follows: Section II reviews previous research in this area. Sections III and IV present the proposed non-volatile flip-flop and describes it in detail, Section V briefly explains how the Non-Volatile/Normally-Off computing can be implemented by using the proposed flip flop, Section VI shows the simulation results and comparison of the proposed nonvolatile flip-flop with previous works. Section VII gives the final conclusion.

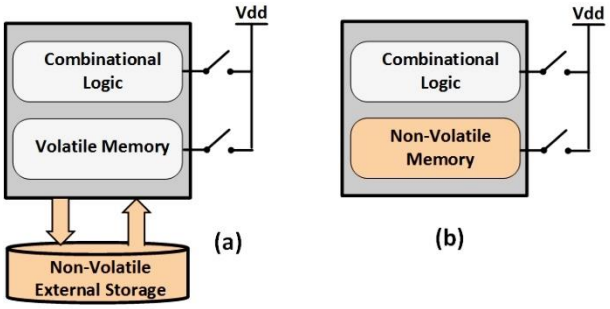

Fig. 1 Power managements: (a) Conventional power gating with data backup/restore (b) Normally-off computing.

2 Previous works

As mentioned earlier, delay, energy consumption, and data loss are the fundamental challenges for computing circuits [12]. Many non-volatile flip-flops have been proposed to address these issues [12], [17]–[29]. For review, we have divided these FFs into two basic categories: a) Flip-flops with the synchronous backup operation and b) Flip-flops with the asynchronous backup operation. In the following, we introduce the available works of each category.

2.1 Flip-flops with synchronous backup capability

In flip-flops with synchronous backup capability, designers try to perform the backup operation synchronously with the normal operation of the flip-flop [19]–[24]. They have low area and power consumption, but a high delay due to the high delay of write/read operations in non-volatile elements.

As shown in Fig. 2(a), Non-volatile elements (e.g., NCFET) are placed inside the flip-flop circuit. Flip-flops with synchronous backup are used in systems with sensitive data.

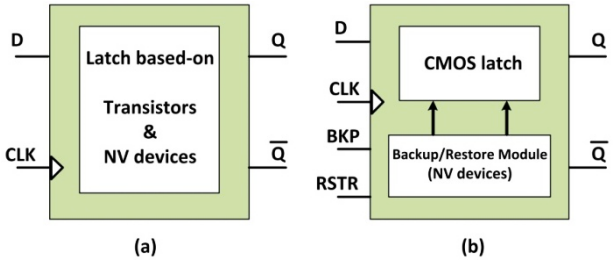

Fig. 2 Non-Volatile Flip-Flop structure: (a) Flip-flops with synchronous backup capability (b) Flip-flop with asynchronous backup capability

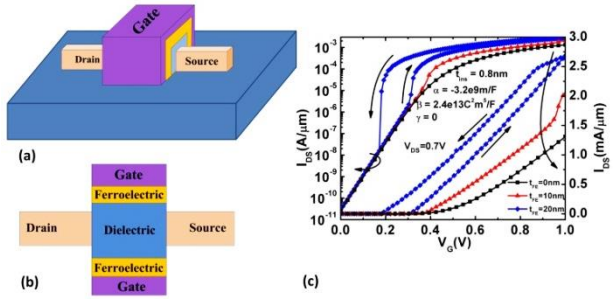

Fig. 3 Structure of the NCFET: (a) 3-D view (b) Cross section view (c) I_{DS}-V_G curves of the NCFET model

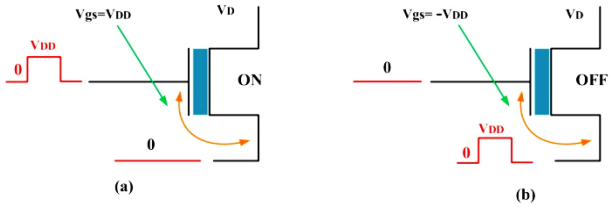

Fig. 4 Operation mode of NCFET transistor a) Write logic "1" (Vs= 0, Vg=VDD), b) Write logic "0" (Vs=VDD, Vg=0).

2.2 Flip-flop with asynchronous backup capability

In flip-flops with asynchronous backup capability, the backup operation and the normal operation of the flip are performed in two different time periods [18], [25]– [29].

In normal operation, data is stored in a volatile latch, and backup operations can be performed at regular intervals (For example, daily, hourly, etc.), or the existence of a request from a system or application. Although Flip flops with asynchronous backup capability offer high speed data transfer rates, they suffer from the high area and power consumption issues. As shown in Fig. 2(b), Non-volatile elements (for example, NCFETs) are placed outside the latch circuit, in a backup/restore module. Flip-flops with asynchronous backup are used in high-speed data computing systems.

This paper proposes a new non-volatile FF that not only provides high-speed data transfer rates but also reduces the area and energy consumption compared to the previous non-volatile flip-flops. In addition, the proposed flip-flop is a type of flip-flop with synchronous backup capability and is also used in systems with sensitive data.

2.3 An overview of the NCFET transistor

Fig. 3, shows the structure of NCFET transistors. As shown in Fig. 3(a), In the NCFET transistor, the channel is highlighted and a ferroelectric layer (e.g., Hafnium Oxide: HfO_2), surrounds on three sides.

The structure of the NCFET transistor is almost similar to the FinFET transistor, except that the existence of a ferroelectric layer in the gate makes the transistor a non-volatile element. The NCFET transistor has two states, ON and OFF, and in any state, changing its state is possible only by giving input; if the power supply of the circuit is also shut down, it will maintain its state. The operation mode of the NCFET transistor is shown in Fig. 4. The NCFET transistor works with voltages in the form of pulses, with the appropriate amplitude and width. When Vgs = +VDD (Vg=VDD, Vs=0) the transistor is on; and when Vgs=-VDD (Vg=0, Vs=VDD) the transistor is Off. When Vgs=0 or the circuit power supply is Off, the transistor maintains its state. In this paper, for NCFET simulation, a model based on the Landau-khalatnikov (LK) equation is used in the Hspice software environment [25], [29]. The LK equation (Eq. 1) shows the behaviour of the ferroelectric layer in terms of polarization and electric field, where α, β and γ are constant coefficients and ρ is the kinetic coefficient of the ferroelectric material. Table 1 shows the values of NCFET transistor parameters.

$$E = \alpha P + \beta P^3 + \gamma P^5 + \rho \frac{dP}{dt} \quad (1)$$

Table 1 The NCFET specifications used in the proposed flip-flop [30].

Technology node $[nm]$	32
Width of the transistors $[nm]$	45
α $[m/F]$	-7×10^9
β $[m^5/F/coul^2]$	3.3×10^{10}
γ $[m^9/F/coul^4]$	-2×10^9
ρ $[\Omega - m]$	0.25
Metal Capacitance $[fF/um]$	0.2
Write Voltage $[V]$	0.3

NCFET transistors have many desirable features such as small dimensions, near-zero static power consumption, high speed, non-volatile, noise resistance, resistant to high-energy particles, and compatibility with semiconductor devices [16]. Therefore, in this paper, NCFET transistors are used to design a non-volatile flip-flop with simultaneous backup capability.

3 Structure of Proposed Non-Volatile Pulse-Triggered Flip-Flop with Simultaneous Backup Capability

Fig. 5 shows the proposed non-volatile pulse-triggered flip-flop with simultaneous backup capability (called NVSB-pt). As illustrated in the figure, only one NCFET transistor has been used in the circuit. Table 2 summarizes the Operation of NVSB-FF. When (VDD='1' and RSTR='0'), the circuit is in normal operation. In this case, if CLK='1', Q will be equal to D, and if CLK='0', Q will preserve the last value of D. When VDD = '0' or in other words the voltage source is shut down, Q becomes equal to '0'.

When (VDD='0' → '1', CLK='0', and RSTR='1') or in other words the voltage source is connected, Q restores the state stored in the latch. Next, the details of the signalling circuit will be explained. Therefore, Vgs = +0.9V, which makes the ferroelectric layer with positive polarization (NCFET connected), and D/Q = 1 is stored in the ferroelectric layer as a state with positive polarization.

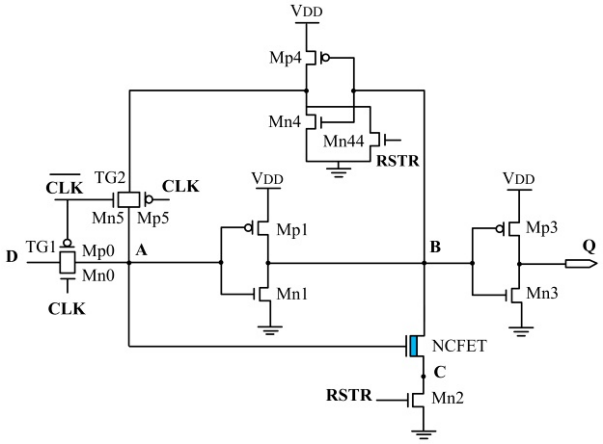

Fig. 5 Structure of the proposed flip-flop.

Table 2 Operation of the proposed flip-flop (NVSB-FF).

Conditions		Operations
RSTR='0'	VDD='1'; CLK='1'	Q takes the value of D.
	VDD='1'; CLK='0'	Q retains its previous value.
	VDD='0'; CLK='1'	Q becomes equal to 0.
RSTR='1'	VDD='0' → '1'; CLK='0'	Q is restored to the stored value.

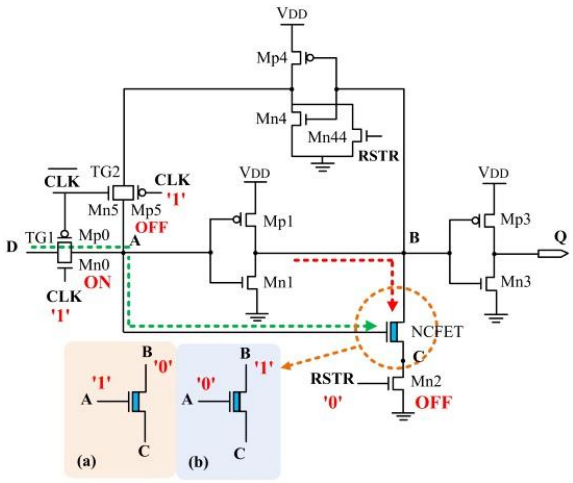

Fig. 6 Operation of the proposed flip-flop in normal and backup operation: a) NCFET is ON, b) NCFET is OFF.

3.1 Operation of the proposed flip-flop in restore mode

During the restore operation, the NCFET is either in the state with positive polarization or in the state with negative polarization (OFF/ON). In any of these states, the flip-flop must be able to correctly restore the value of Q during restore. If the ferroelectric layer is polarized with positive polarization (NCFET is connected), should be Q='1', and if the ferroelectric layer is polarized with negative polarization (NCFET is off), Q=should be Q='0'.

To start the restore operation, the RSTR signal is set to '1' and CLK is set to '0'.

The value of node A through path-1 takes the value '0' and the transistors Mn1 and TG1 are OFF; And Mp1, Mn2, and TG2 are ON (Fig. 7). The transistors Mp1 and NCFET form a Pseudo-NMOS inverter whose output logic (node B) depends on the state of the NCFET.

Case-1 (Restoring Q = 1): If the ferroelectric layer is polarized with positive polarization, the stored data is logic '1' (NCFET turned ON in Fig. 7(a)), the NCFET brings node B to 0V and the Q value becomes logic '1'. Now, if RSTR is equal to '0', the data is stored (D='1'), restored and transferred through TG2, and latched.

Case-2 (Restoring Q = 0): If the ferroelectric layer has a negative polarization, the stored data is logic '0' (NCFET turned OFF in Fig. 7(b)), Mp1 drives node B to 0.9V and the Q value becomes logic '0'. Now, if RSTR becomes equal to '0', the data is stored (D='0'), restored and transferred through TG2, and latched. Fig. 8 and Fig. 9 show the behaviour of the proposed flip-flop in different restored states. The simulation was performed in HSPICE using the 10nm-PTM technology and a supply voltage of 0.9V.

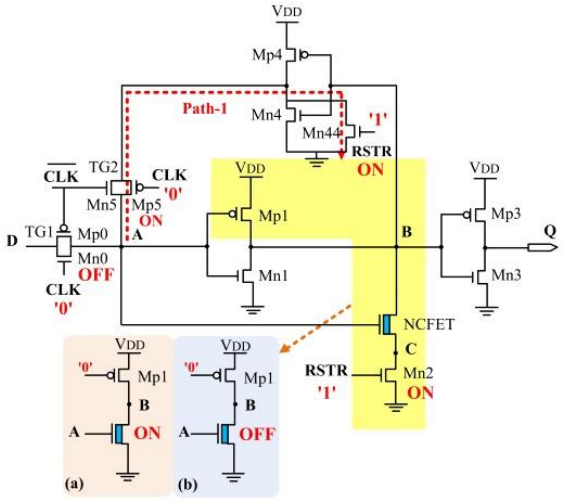

Fig. 7 Operation of the proposed flip-flop in the restore operation a) Pseudo-NMOS inverter: V(B) is equal to logical '0' b) Pseudo-NMOS inverter: V(B) is equal to logical '1'.

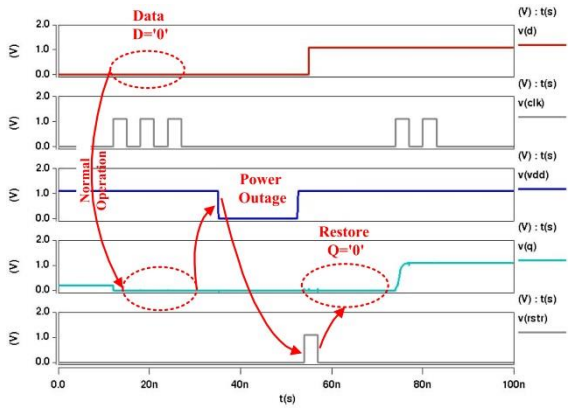

Fig. 8 Data restore '0' (Q='0').

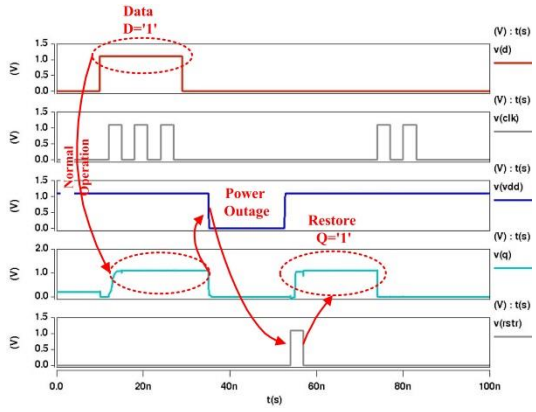

Fig. 9 Data restore '1' (Q='1').

4 The proposed edge-triggered and radiation-hardened flip-flop

Fig. 10 shows the proposed non-volatile edge triggered flip-flop with simultaneous backup capability (called NVSB-et). The NVSB-et contains a master latch that accepts the D input signal when CLK is low (CLK = '0') and holds it when CLK is high (CLK = '1'); and a slave latch that works the opposite way, the signal is transmitted from the master latch to the slave latch while CLK='1' and held until CLK='0'. Therefore, the signal must be transmitted through the master latch during CLK is equal to '0', and through the slave latch during CLK is equal to '1'. Which means that the D input signal is pass to the output Q only when the CLK changes from low to high (rising edge of CLK signal).

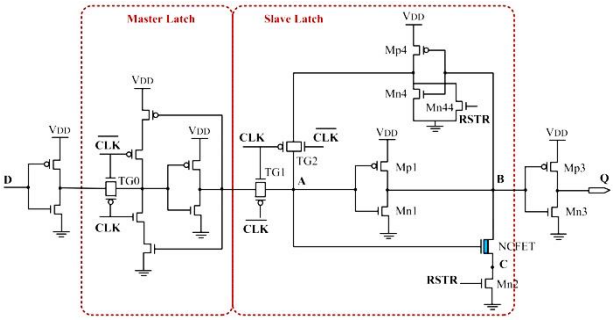

Fig. 10 Proposed Edge-Triggered Flip-Flop.

NVSB-et has a nearly low area overhead and is one of the most power-efficient structures compared to other master-slave latch-based designs. However, it is weaker against soft errors. A soft error or SEU occurs when an energetic particle strikes a FF of a processor logic block and changes the state of a data-FF.

The master latch of NVSB-et can easily be upset by soft errors that occur when CLK='1' (master latch-in-hold state) while the slave latch can be upset when CLK='0' (slave latch-in-hold state) as shown in Fig. 11. In Addition, soft errors can affect NVSB-et during the transparent mode, if the error is propagated and kept by the subsequent latch.

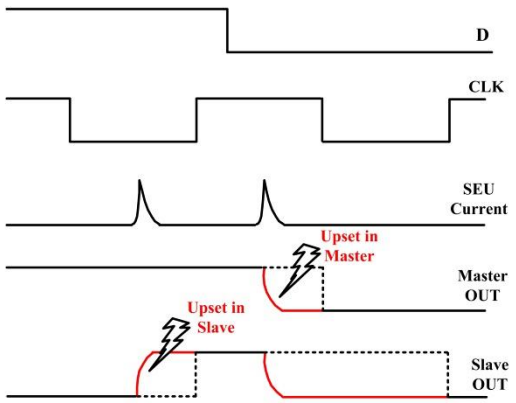

Fig. 11 Impact of Single Event Upset (SEU) on the NVSB-et master and slave latches.

In order to solve the problem of a Single Event Upset (SEU), we proposed an SEU-tolerance inverter (called STI). As shown in Fig. 12, the STI consists of two parts;

In STI1 (in Fig. 12), two separate paths from the input are applied to {Mp1-Mn1 and Mp2-Mn2}. One is a direct path from n1 to n2 and the other is a delayed one from n1 to n4. The STI1 is an inverter that inverts its input (IN) only if both nodes n2 and n4 are identical logic values. If the two voltage nodes of n2 and n4 have different values, the previous output value will be retained by STI2.

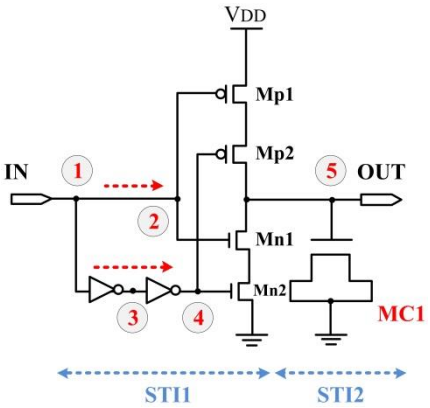

Fig. 12 Proposed SEU-tolerance inverter (STI).

STI2 is a MOS capacitor (MOSCAP). Connecting the MOSFET drain and source together creates a MOSCAP [31]. Due to the fact that the capacitor is resistant to sudden changes in voltage, it has the ability to act somewhat like a secondary-cell battery to maintain a stable output. Therefore, an SET pulse in nodes of n1, n2, n3 or n4 will be filtered through STI2; and an SET pulse in the node of n5 will be filtered through STI1.

In the design of Fig. 10, we use STI instead of a conventional inverter. Fig. 13 shows the proposed radiation resistant flip-flop.

To investigate the soft error tolerant capability of the proposed NVSB-pt, a number of SEUs are injected into various nodes of NVRH-SB and their effect on the output node (Q) is observed. Fig. 14 shows the related simulation results.

As shown in the figure, any particle strike to nodes A and B that occurred with the SEU injections was recovered after a short period of time. This recovery is the resultant of the STI1 and STI2 parts that restore the corrupted data. Simulation results showed that, depending on the supply voltage, NVRH-SB is capable of tolerating SET pulse duration of up to 630ps.

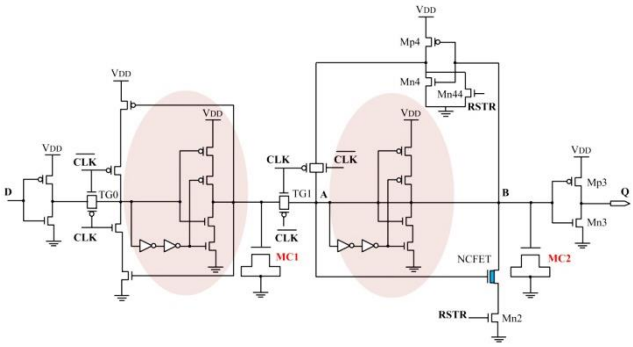

Fig. 13 Proposed Radiation-Hardened and Edge-Triggered Flip-Flop.

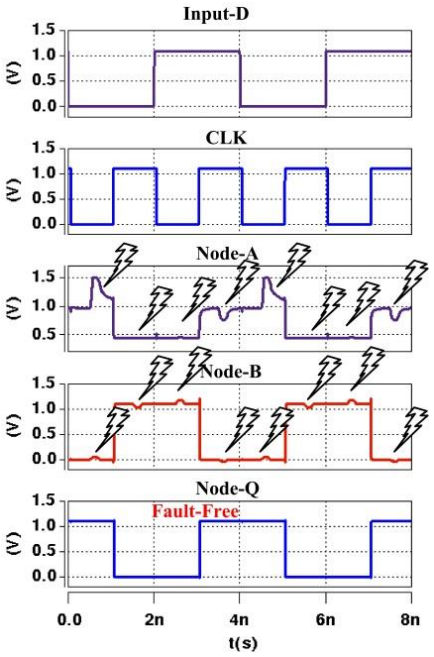

Fig. 14 SET filtering capability of NVSB-RH

5 Non-volatile/normally-off computing by using proposed NVRH-SB

In conventional power gating, when a processor is in the standby state, the data is stored in the non-volatile memories made of emerging nano devices. When the system is reset, the data stored in non-volatile memories can be automatically returned in the registers or flip flops in a very short time.

However, conventional power gating in digital systems still faces many challenges. The first challenge is how to mitigate the energy, delay and possibly high peak power of a backup or restore operation. The second challenge is how to perform backup and restore control for distributed NV-devices, and how to organize the policy of backup and restore [1]. Providing this control action results in additional wiring, more area and energy consumption.

To overcome the above challenges, the entire structure of a normally-off computing system can be designed by using NVRH-SB flip-flops as shown in Fig. 15.

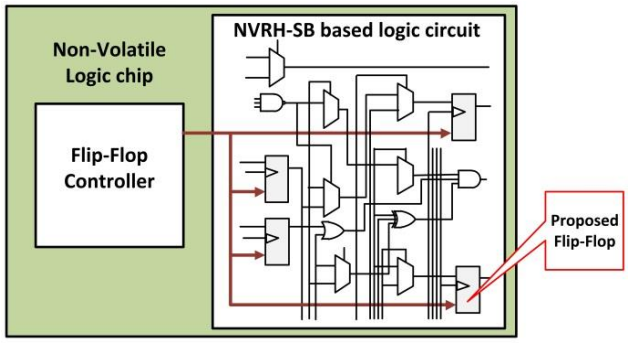

Fig. 15 Non-volatile logic chip based on NVRH-SB.

In this section, we present a non-volatile 1-bit ALU (nvALU) which integrated with proposed NVRH-SB and CMOS 3-state gates for realizing normally-off computing technology.

5.1 Non-Volatile Serial ALU (nvsALU) by using NVRH-SB

A serial arithmetic-logic unit (sALU) is a fundamental component of the soft processor used in FPGA based designs to perform various useful arithmetic and logic operations [32]. The design of the sALU is a very critical part of the soft processor and many researches are going on for speeding up instruction execution and reducing power consumption by improving the sALU structure.

On the other hand, the nonvolatile ALU is an emerging approach to nonvolatile computing [33]. Nonvolatile computing has been proven to be effective solution to prevent computation progress loss due to either an unexpected or scheduled power outage in energy-harvesting Internet-of-Things applications.

To achieve the above purposes, a non-volatile serial ALU (nvsALU) is presented in Fig. 16. In nvsALU, three shift registers are used for the inputs A and B and the output R.

When the circuit is reset, the shift registers A and B are loaded with parallel data. Positive edge triggered flip flops are used in which all changes take place soon after the positive edge of the clock. At this time, the contents of all three-shift registers are shifted to the right. This causes the X-FF output to be transferred to the accumulator register and the next pair of input bits Ai and Bi to be transferred to the ALU.

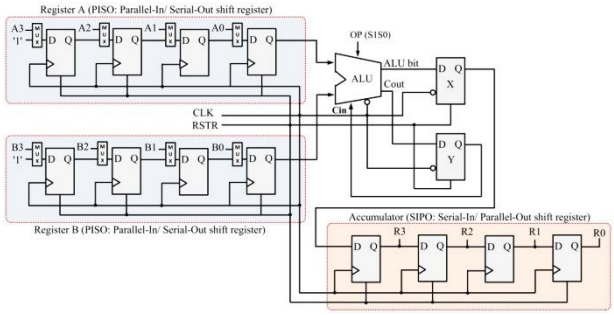

Fig. 16 Non-volatile Serial ALU by using proposed Flip-Flop.

The internal structure of the proposed 1-bit ALU is shown in Fig. 17. According to Fig. 17, when CLK =′0′ , transistors MpCLK and MnCLK are turned ON. The power supply is connected to the circuit and the ALU operates based on the selected lines S1 and S0. The results are stored in X and Y flip-flops.

When CLK =′1′, transistors MpCLK and MnCLK are turned OFF. The power supply is disconnected from the circuit. This power gating reduces power consumption by cutting off the idle ALU.

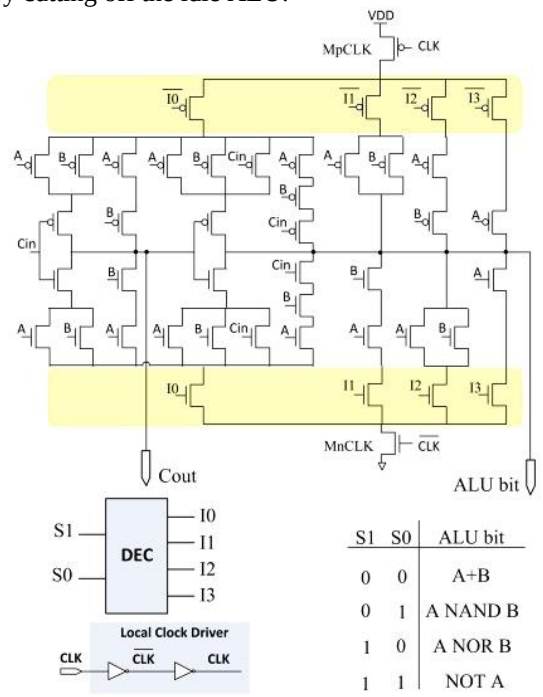

Fig. 17 Power gating 1-bit ALU.

If a sudden power supply failure occurs, the data of the three registers are restored by activating the signal RSTR.

The proposed ALU uses 3-state gates. 3-state gates are the types of logic gates having three states of output: high (H), low (L) and high-impedance (Z). High impedance is equivalent to not being connected. As shown in Fig. 17, the outputs of the 3-state gates are connected directly together to form a common output

Table 3 Comparison of the proposed flip-flop with previous works.

Parameters/References	Ref. [17]	Ref. [18]	Ref. [37]	Ref. [38]	Ref. [39].(a)	Ref. [39].(b)	Ref. [40]	Ref. [1]	NVRH-SB
Technology	10nm	10nm	10nm	10nm	10nm	10nm	10nm	10nm	10nm
Year	2017	2018	2019	2021	2021	2021	2022	2024	2024
Non-volatile element	PZT cap.	PZT cap.	MTJ	RRAM	NCFET	FEFET	FEFET	FEFET	NCFET
Supply voltage (VDD)	1.5V	1.5V	1.1V	1.8V	0.4V-0.8V	0.4V-1.0V	0.2V-0.8V	0.7V	0.9V
# Voltage sources	1	2	1	2	1	1	1	1	1
# Transistors (area)	30-Tr. 2-PZT cap.	21-Tr. 2-PZT cap.	25-Tr. 2-MTJ	23-Tr. 2-FEFET	24-Tr. 2-NCFET	22-Tr. 2-FEFET	23-Tr. 2-FEFET	24-Tr. 2-FEFET	36-Tr. 1-NCFET
Backup time	1.64s	2.22s	909ps	10ns at 2.4V	1.4ns at 2V	1.0ns	1.0ns	0	0
Restore time	1.25s	2.2s	177ps	1.3s at 0.4V	75ps at 0.5V	56ps at 0.8V	0	261ps	~39ps
Backup energy	2.4pJ	3.44pJ	82.2J	735fJ	7.0fJ at 0.5V	1.3fJ	1.2fJ	0	0
Restore energy	2.34pJ	0	0	735fJ	9.0fJ at 0.5V	1.1fJ at 0.8V	1.4fJ	1.36fJ	1.3fJ
Requires additional control signals	Yes	Yes	Yes	Yes	Yes	NO	Only Restore	Only Restore	Only Restore
Supports sudden power outage	NO	NO	NO	NO	NO	Yes	NO	Yes	Yes
SEU immune	NO	NO	NO	NO	NO	NO	NO	NO	Yes

line, provided that the circuit guarantees that all but one will be in a high-impedance state at any given time. Using a decoder to control 3-state gates guarantees this. The proposed ALU performs the following operations:

Logical Operations: These functions include NAND, NOR, and NOT. The NAND and NOR gates are universal gates. These gates are functionally complete, i.e. they are sufficient to implement any complex digital circuits.

Universal gates are utilized because they are cost effective and easier to fabricate. In addition, when the realization of a complex Boolean function, the goal is usually to reduce the number of operators and thus reduce gate count. Using these gates actually facilitates this goal, as it helps reduce the Boolean equation as quickly as possible when using De Morgan's law.

Arithmetic Operations: This refers to bit addition. It should be noted that subtraction A − B is calculated as addition with the negative number, i.e. A + (−B). The addition A + (−B) is equal to A + B + 1.

There are sometimes multiplication and division required. These operations are complex and expensive to implement. In soft processors, multiplication and division can be realized as repeated addition and subtraction, respectively.

5.2 Evaluation at the circuit level

The simulation of the proposed circuit has been done by HSPICE software in 10 nm PTM technology [34]. For NCFET simulation, the model presented in [35] was used, and CosmosScope software was used for data analysis.

Table 3 shows the parameters of non-volatile flip flops that are designed based on non-volatile elements such as PTZ cap, MTJ, ReRAM, etc. Based on Table 3, one of the most significant issues with previous designs is the high delay and energy consumption in data backup and restoration. The lowest supply voltage in previous works belongs to reference [36], which uses a non-volatile FEFET element, but the area in reference [18] has the lowest value, and the lowest restore and backup times belong to references [17] and [29], respectively. Meanwhile the lowest amount of energy consumption and backup belongs to the reference [17]. But One of the challenges associated with the DFF element is that sudden interruption of the voltage source can cause data loss, which in previous works only reference [18] without the need for additional signals provides the possibility to preserve information when the voltage source is shut down. In reference [18], a non-volatile FEFET element has been used.

Now, if the proposed NVSB-FF flip-flop is compared to other flip-flops; It can be observed that except for the supply voltage, NVSB-FF has improved all parameters. The first reason is that in this flip-flop, backup/restore is done without any external module, and another reason is the use of a non-volatile, low-power, and fast NCFET element.

We utilized the model presented in [41] to inject the SEU fault into the simulated flip flops, in which an SE hit could be applied to the flip-flop nodes using a double exponential current source with the treatment of Eq. 2:

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_a - \tau_b}\left(e^{-t/\tau_a} - e^{-t/\tau_b}\right) \quad (2)$$

where Q_{inj} is the total amount of collected charge at the affected node. τ_a and τ_b are two time constants, dependent on material [41]. τ_a is the charge-collection time constant of the junction and τ_b is the time constant for the initial creation of the ion track.

Table 3 shows all flip-flops, except NVRH-SB are vulnerable to SEU.

Fig. 18 shows the proposed flip-flop layout. This

configuration is achieved by optimizing the backup and restore functions. The occupied area of the proposed flip flop is equal to *26.34um*^{2}. The proposed flip-flop has small area overhead. This is due to the absence of a separate backup unit in its structure.

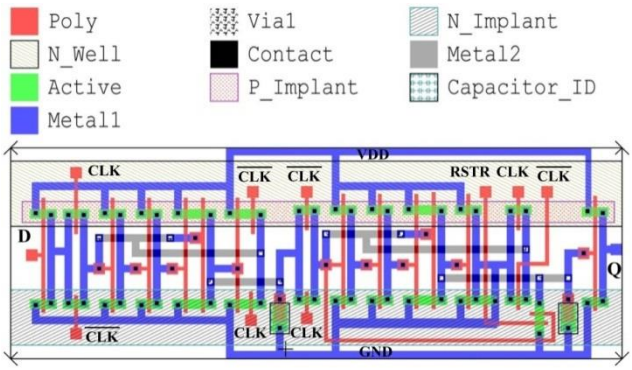

Fig. 18 The proposed flip-flop layout.

6 Evaluation at the system level

Simulation method at the system level, to compare the energy consumption of non-volatile flip-flops, a TI MSP430 MCU with a frequency of 24 MHz is simulated as described in [42]. All MCU registers are designed based on NVFFs (Fig. 19).

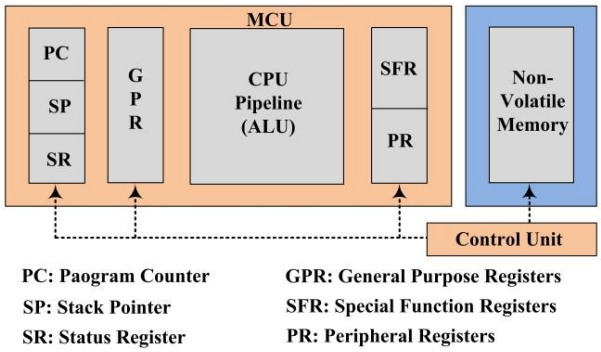

Fig. 19 Structure of MCU to compare energy consumption at the system level.

The energy consumption of the system with a different number of checkpoints is shown in Fig. 20. The amount of energy consumed in flip-flops depends significantly on the number of checkpoints during program execution. Therefore, by changing the number of checkpoints, energy consumption has been calculated.

As seen in Fig. 20, with the increase in the number of checkpoints, NVSB-FF consumes less energy than [17] and [18].

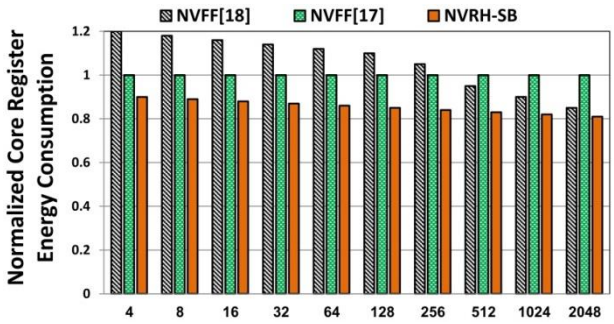

Fig. 20 Comparison of system energy consumption by changing the number of checkpoints.

According to Fig. 21, in practical applications, NVSBFF consumes less energy. It can be seen that NVSB-FF provides an average energy consumption reduction of 23%.

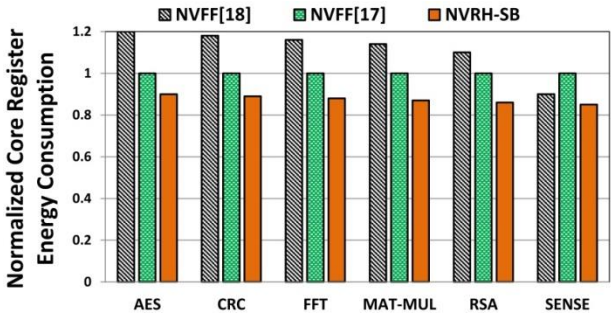

Fig. 21 Comparison of system energy consumption in different applications.

The most important features of NVSB-FF compared to previous flip-flops are:

- In the proposed flip-flop, by adding a minimum number of devices to the traditional CMOS structure, data non-volatile capability is provided. Considering that NCFET transistors are non-volatile, they do not require any voltage or current to maintain data. Therefore, if the supply voltage is shut down, it will not affect the NCFET mode.
- The proposed flip-flop does not need a separate circuit for backup and restore operations because these operations are performed at the same time, which makes the backup time zero.
- Although the restore time depends on the supply voltage, with a supply voltage of 0.9V, the NVSBFF has a very short restore time and the power consumption during the restore time is also significantly less than other flip-flops.
- The use of NCFET in the proposed flip-flop increases immunity to noise because NCFET has a hysteresis feature. To change the state of NCFET from OFF to ON, a voltage equivalent to Vgs=+VDD is required, and to change the state of NCFET from ON to OFF, a voltage equivalent to Vgs=-VDD is required.

7 Conclusion

In this paper, a flip-flop with low power, high speed, non-volatile and radiation-hardened based on NCFET was presented. In the proposed circuit, power and energy consumption has been significantly reduced. In this design, there is no time and energy consumption for backup because the backup operation is performed simultaneously. In addition, the area has been reduced due to the absence of a separate backup circuit. The restored energy consumed is 1.3fJ, which is the lowest amount of restored energy compared to previous works. The hysteresis feature in NCFET makes the proposed flip-flop very resistant to noise. In addition, another advantage of the proposed design is that the information does not lose with sudden voltage source failure. The mentioned items and the results show the superiority of the proposed design compared to previous works.

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