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Design and Implementation of a 31-level Inverter Based on FPGA for Sustainable Energy Applications

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Abstract: Artificial intelligence-based optimization algorithm was used to compute the switching angle values. In order to run the inverter with the lowest possible Total Harmonic Distortion (THD) value, it is suggested in this study to use an algorithm such as the Practical Swarm Algorithm (PSA). The multilevel inverter and optimization algorithm were created and simulated in this study using a MATLAB software. A frequency spectrum analysis was also conducted and found to be consistent with the theoretical analysis of the system. To provide practical results, the FPGA generates PWM signals that are appropriate for the inverter switches. On the Spartan-3E Starter set, the suggested control schemes were developed and put it into practice. Xilinx-ISE 12.1i design software and VHDL hardware description language were used to create the FPGA software. The suggested approaches have a number of benefits over conventional digital PWM techniques, including straightforward hardware implementation, minimum scaling of digital circuits, easy digital design, reconfigurable, and flexibility in adaptability. The outcomes of the experiment and the simulation agreed rather well.

Keywords: FPGA, Selective harmonic elimination (SHE), Harmonics, Particle Swarm Optimization (PSO).

1 Introduction

MULTILEVEL inverters (MLIs) are now employed at various voltage and power levels in a wide range of industrial, utility, and power applications. The early 1980s saw the introduction of the multilayer inverter idea. A voltage waveform with three or more stages in the output is referred to as multilevel [1]. Due to its ability to generate low harmonic components at low switching frequencies, multilevel inverters have grown in popularity. Additionally, they produce reduced losses, low electromagnetic interference (EMI), and low blocking voltage of switching devices [2], [3]. To achieve the high-power rating and high-quality output voltage waveforms, multiple voltage-source inverters are a suitable way [4], [5]. Better waveforms with a wider range of harmonics may be produced by these inverters than by a basic square wave inverter. The number of fuel cells and solar cells that use them is growing [6].

Many control strategies have been put forth and used in the context of multilevel inverter applications. The control approaches may be categorized into two groups: low switching frequency techniques, which are fundamental, and high switching frequency techniques, which are complex. The active power switch is only commutated once or twice in a single cycle when using low switching approaches like Space Vector Control (SVC) and Selective Harmonic Elimination (SHE). Nevertheless, the SHE is a commonly utilized control method for multilevel inverters, particularly in situations requiring high power and medium voltage. Because of its low switching in comparison to other control approaches, the SHE technique has reduced switching losses and less EMI [7]. Furthermore, it can reduce the size of the necessary filter at the inverter output by eliminating the dominating low order harmonic. In the SHE method, a series of nonlinear equations is solved to determine the switching angles in advance. Numerous strategies and mathematical methodologies have been put up and examined in literature to address the SHE

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issues in multilevel inverters [8]. The basic categories into which all suggested solution approaches can be divided are: a) Iterative approaches; b) Resultant Theory; and c) Evolutionary Algorithms. One of the most used iterative methods is Newton Raphson (NR). NR has been used in to address the SHE issues in multilevel inverts [9]. The technique is simple to use and effectively removes the harmonics. It does, however, require an accurate beginning estimate and may not converge at certain amounts.

In 2017, a Hybrid An ant colony optimization-based hybrid algorithm was utilized to determine the ideal switching angles in a three-phase, seven-level inverter. An optimization algorithm was applied to eliminate low order harmonics in the reduced switches multilevel inverter, and the resultant THD of the load voltage was 4.66% at M=0.8 index of Modulation [10]. In 2018, provides the hybrid asynchronous PSO (APSO) method for selective harmonic elimination (SHE) in MLI and the SHE-PWM approach. The best THD for phase output voltage was 12.52% while using the based hybrid (APSO) Newton-Raphson (APSO-NR) method for removing unwanted harmonics in cascaded H-bridges (MLI) [11]. In 2015, the recently developed evolutionary optimization method named BAT algorithm is used to solve the nonlinear transcendental equations of SHE problem. To verify the presented method accuracy, simulation and experimental results are provided for a 7-level cascaded multi-level inverter. The feasibility and effectiveness of the proposed algorithm is evaluated with intensive simulation [12]. In 2020, the E-Type RSMLI is successfully designed and simulated in MATLAB for R and R-L load. The topology is simulated using Selective Harmonic Elimination method, for the suppression of lower order harmonics and the THD-V value obtain equal 3.46% of 13-level [13]. In 2020, using the OMTHD technique by applying the NR, GA, and PSO methods, the best THD value reduction results were obtained with the PSO algorithm. In contrast, using the classical NR optimization method, it presented higher THD values for all cases. Finally, analysing the results obtained with the SHE method eliminating the low order harmonics according to the case, a greater reduction of the THD value was achieved in most of the analysed cases, using the PSO algorithm [14]. In 2021, the SHE method assisted with GA in order to generate switching signals for MLIs fed from adjustable DC sources is investigated. The proposed method’s validity has been demonstrated by simulations performed with MATLAB software. As a result, the designed system is recommended for high power applications that may be affected by low order harmonics and high THD [15]. In 2022, the best switching angles for cascading multilevel inverters to provide minimal total harmonic distortion (THD) in output voltage were found using the Genetic Algorithm (GA), Particle Swarm Optimization (PSO), and Bee Algorithm (BA) in this study. PSO, GA, and BA have THD values of 12.56%, 13.03%, and 12%, respectively, according to calculations [16].

This study examines the most popular method for resolving the SHE issue, which is PSO. This study's objective is to provide a thorough solution to the SHE problem. This work made use of a 31-level inverter, which is simulated by MATLAB-SIMULINK and implemented practically using the FBGA card.

2 Theoretical Analysis of the Proposed MLI

The power electronic component utilized in electrical power conversion systems is called a multilevel inverter. To create the desired waveform, a multilevel inverter employs a number of stages. Several benefits come with this technique: reduced voltage stress, increased efficiency, and improved output waveform and power system quality. Motor drives, renewable energy systems, and utility applications are just a few examples of the high-power applications that often employ MLIs [17]. This research uses 16 switches and 4 DC input sources (Vdc) to modify an MLI circuit to generate a 31-level output AC voltage. Fig. 1 shown a Four asymmetrical isolated DC sources are used as the input DC voltage sources, and they are organized in a (1:2:4:8)*Vdc ratio. The DC voltage is provided by a group of solar PV systems that include boost converters. Table 1 displays the necessary switching patterns to attain a 31-level output voltage. Only the patterns of the positive part are mentioned, and to get the patterns of the negative part we reverse the state of switches S1 to S8 of the positive part. The present route diagram is shown in Fig. 2 under different operating modes according to Table 1 switching statuses. Fig. 5 show the current paths taken to produce different output voltage values: Fig. 5(a) shows the output voltage path to produce +12Vdc, Fig. 5(c) shows the output voltage path to produce -3Vdc, and Fig. 5(d) depicts the current path to obtain an output voltage of -7Vdc.

Table 1 Switches states of the 31-level output voltage

Conducting switches: 1 =ON; 0= OFF												
S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Q_1	Q_2	Q_3	Q_4	V_{out}
1	1	0	0	1	1	0	0	1	1	1	1	$15V_{dc}$
1	1	0	0	1	1	0	0	0	1	1	1	$14V_{dc}$
1	1	0	0	1	1	0	0	1	0	1	1	$13V_{dc}$
0	1	0	1	1	1	0	0	0	0	1	1	$12V_{dc}$
1	1	0	0	1	1	0	0	1	1	0	1	$11V_{dc}$
1	1	0	0	1	1	0	0	0	1	0	1	$10V_{dc}$
1	1	0	0	1	1	0	0	1	0	0	1	$9V_{dc}$
0	1	0	1	1	1	0	0	0	0	0	1	$8V_{dc}$

1	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**7V_{dc}**
1	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**6V_{dc}**
1	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**5V_{dc}**
0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**4V_{dc}**
1	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**3V_{dc}**
1	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**2V_{dc}**
1	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**1V_{dc}**
1	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0V_{dc}**

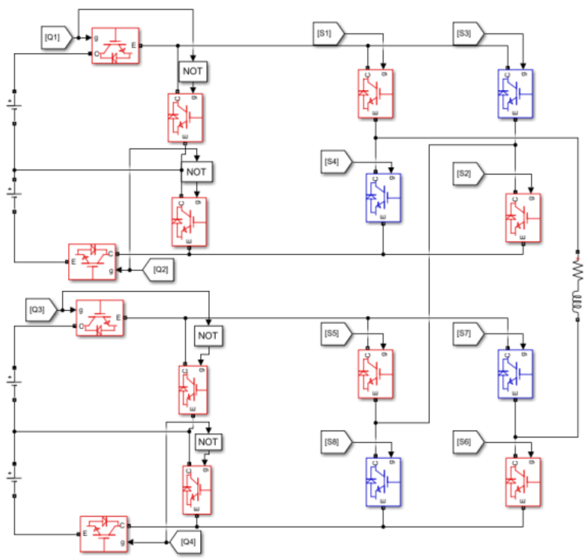


Fig. 1 The proposed of the 31-level inverter circuit.

3 Selective Harmonic Elimination

Selective harmonic elimination, or SHE, is the procedure used in the power electronics sector to remove or reduce certain harmonics from the output waveform of inverters or converters. Unwanted frequency components called harmonics may be present in the output voltage or current of power electronic equipment. They may result in a number of issues, including increased losses, electromagnetic interference, and waveform distortion. Selective Harmonic Elimination involves the removal of some harmonics and the retention of others. Typically, this is achieved by controlling the switching patterns of power electronic devices, such as the MOSFET or IGBT switching in an inverter [18]. By meticulously choosing the switching angles and pulse-width modulation (PWM) patterns, you may exclude specific harmonics from the output waveform. A set of nonlinear equations have to be solved in order to determine the optimal switching angles that result in the elimination of the desired harmonics. The goal is to achieve the intended harmonic profile while meeting the system's criteria, which include keeping the fundamental frequency constant and reaching the required output voltage. Selective harmonic elimination is often used in power systems that provide sensitive loads or in settings where strict adherence to harmonic standards is required, two contexts in which low harmonic distortion is essential [19]. Artificial intelligence (AI) techniques are now mostly applied to optimization techniques to address engineering challenges. These optimization algorithms' main advantages are their modest complexity and absence of complete reliance on expert assumptions [20]. Furthermore, low-cost digital signal processors may be used to quickly build this AI. Several optimization techniques are employed in different contexts, including Differential Evolution, Particle Swarm Optimization (PSO), Genetic Algorithm, and Bee Algorithm [21]. The objective functions used by these algorithms take nonlinearity in low-order harmonic equations into account. Most researches use different goal functions to lower the harmonic elimination [22]. A number of approaches have been put out over time to deal with the harmonic elimination issue. The pulse width modulation technique of selective harmonic removal allows for the expression of the output waveform by Fourier expansion [23].

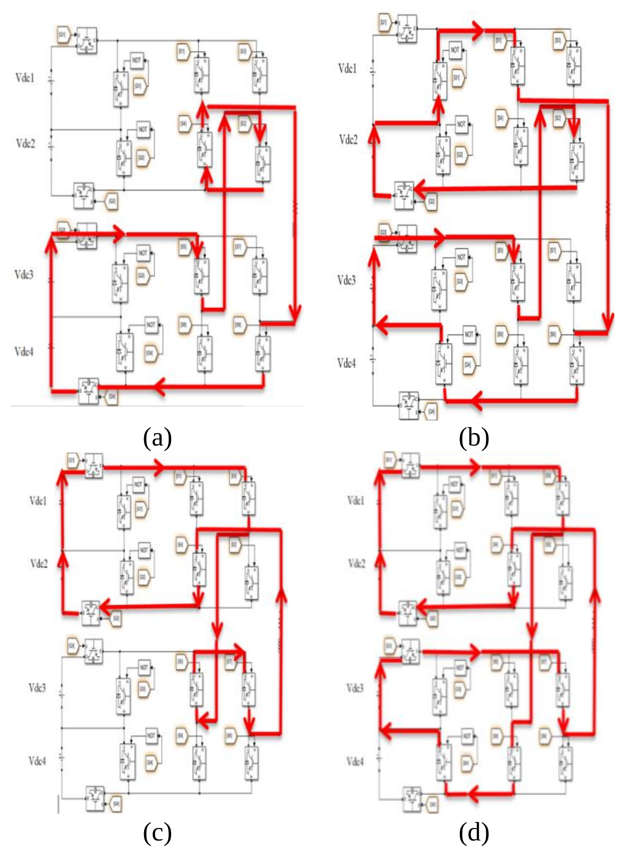


Fig. 2 Current path with output voltage of (a) +12V_{dc}, (b) +6Vdc, (c) -3Vdc, and (d) -7Vdc.

$$\mathrm{Vm}(t) = \frac{Ao}{2} + \sum(An\cos(nw) + Bn\,sin(nw)) \quad (1)$$

Where A_o is dc component, *An* is amplitude of the even harmonics, and Bn represents odd harmonics. Multilevel inverter produces quarter symmetric output in which the dc component and even harmonic component gets 0. Equation (2) becomes:

$$\mathrm{Vm}(t) = Vn\,sin(n\alpha i) \quad (2)$$

The equation of Fourier expansion can be expressed in the form of Eq. (2) which becomes

$$Vn = \frac{4Vdc}{\mathrm{n}\pi}\sum_{i=1}^{m} Ki\cos(n\alpha i) \quad (3)$$

Ki is the ratio of dc voltage source of i^{th} voltage and dc source which can be expressed in the form of

$$Kn = \frac{Vdci}{Vdc} \quad (4)$$

The only harmonics present in quarter-wave symmetric multi-level inverter are odd which need to be eliminated. The switching angles should be selected in such a way to reduce the total harmonic distortion [24]. It is feasible to remove all of the low-order harmonics by solving the following system of non-linear equations

$$\begin{Bmatrix} V1 = \frac{4Vdc}{\pi}[cos\alpha_1 + cos\alpha_2 + +cos\alpha_k] = Mi \\ V3 = \frac{4Vdc}{3\pi}[cos3\alpha_1 + cos3\alpha_2 + +cos3\alpha_k] = 0 \\ \vdots \\ Vn = \frac{4Vdc}{n\pi}[cosn\alpha_1 + cosn\alpha_2 + cosn\alpha_k] = 0 \end{Bmatrix} \quad (5)$$

Where $\mathrm{Mi} = \frac{\mathrm{V1}}{\mathrm{S} * \mathrm{V}_{dc}}$

Mi the modulation index, V1 is the fundamental voltage value, S is the DC sources number, and V_{dc} = DC source value. In single-phase n = 1, 3, 5, 7 … ∞, α_k is the switching angle, and V_n is the output voltage for the n^{th} harmonic.

The following condition must be met by the switching angles [25].

$0 < \alpha_1 < \alpha_2 < \alpha_3 < \cdots \alpha_{12} < 90°$.

4 Particle Swarm Algorithm

By choosing the ideal switching angle values, the objective function of optimization approaches is to reduce the THD of any power circuit. Particle swarm optimization (PSO) was used in this study to analyse and simulate the data in order to solve the selective harmonics elimination (SHE) methodology problem by selecting the best firing angles to reduce the THD value of the inverter output voltage waveform [26]. Based on the mobility and intelligence of swarms, PSO is a strong stochastic optimization method. With the aim of finding the optimal answer, a swarm of agents, or particles, moves throughout the search area in this approach. According to the PSO approach, each swarm agent is characterized by its position and velocity and provides a solution. A swarm of random particles is initialized in the PSO technique, and it then uses updated generation to look for the best solution. Every iteration updates each particle by the two best values [27], [28]. The PSO algorithm consists of a relatively basic notion, with paradigms implemented in a few lines of code. with an explanation of each step provided below:

The following steps for formulating a solution using PSO is taken into account to determine switching angles for harmonic elimination [20]:

1. Floating-point strings or select binary.
2. Determine how many particular variables there are in the problem, and put them within several searching points and the searching points gradually get close to the optimal point using their local best (p-best) and the global best (g-best). The number of variables in this application corresponds to the number of switching angles for the MLI. Twelve switching angles are needed for a 31-level inverter.
3. Initialize the population after determining its size. The execution time may increase along with the convergence rate as the population grows, some experience in PSO is needed to choose a population that is the optimal size. A random angle between 0 and 90 degrees is used to initialize the population while taking into account the output voltage waveform's quarter-wave symmetry.
4. For PSO to find the optimal answers within a wide search space, the fitness function is essential. Eliminating lower order harmonics (h3, h5 up to h31) for (31-level) and reducing THD for are the goals of this work. The formulated fitness Value according to the formulated (FV) is according to eq. (6).

$$\mathrm{FV}(\alpha 1, \alpha 2, \dots, \alpha k) = \sqrt{\left[\frac{(h3)^\wedge 2 + (h5)^\wedge 2 + (hn)^\wedge 2}{\mathrm{abs(h1)}}\right]} \quad (6)$$

Where h_1: fundamental component, and h_n: is the amplitude of the n-th harmonic, with n odd, (h3, h5 up to h31) are the harmonics magnitudes of (5, 7 up to 31).

5. For calculating a certain number of modulation indexes, modified step is applied to the fitness equation and repeats the previous steps. In this study, modulation index (Mi) is changed from 0.5 to 1. Fig. 3 shows the flowchart of the optimizing proses for Particle Swarm algorithm optimization.

5 Simulation results

Fig. 4 and Fig. 5 show the block diagram of the single and three-phase 31-level inverters, respectively. Fig. 6 describes the switching angels in degree with respect to different modulation index for a single-phase 31-level inverter using PSO algorithm. Fig. 7 demonstrates the value of THD at different modulation indexes for a single phase 31-level inverter using PSO algorithm. Fig.

8 describes the switching angels in degree with respect to different modulation index for a three-phase 31-level inverter using PSO algorithm. Fig. 9 demonstrates the value of THD at different modulation indexes for a three- phase 31-level inverter using PSO algorithm. Fig. 10 show the waveform of Output current 31-level single-phase inverter and FFT analysis at Modulation Index = 0.95 and switching angels in degree are (α1=1.60, α2=6.20, α3=16.81, α4=21.40, α5=22.81, α6=30.05, α7=35.84, α8=44.17, α9=48.34, α10=57.32, α11=59.68, α12=66.59, α13=70.70, α14=79.93, α15=84.87) at load (R=100Ω, L=200mH). While Fig. 11 show the waveform of Output current 31-level three-phase inverter and FFT analysis at Modulation Index = 0.95 and switching angles in degree are (α1=1.24, α2=7.55, α3=11.46, α4=21.04, α5=23.28, α6=29.86, α7=39.95, α8=77.28, α9=46.62, α10=56.38, α11=61.38, α12=69.10, α13=75.20, α14=70.44, α15=88.23) at load (R=100Ω, L=200mH).

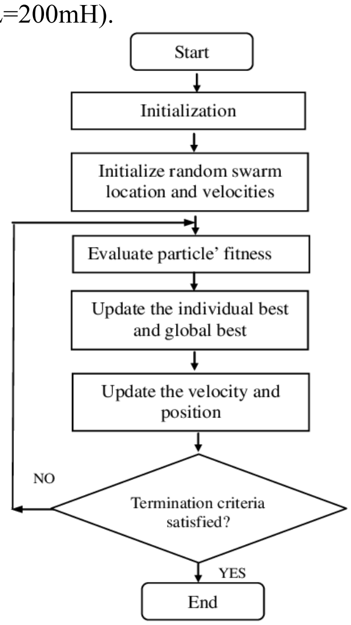


Fig. 3 General PSO algorithm flowchart.

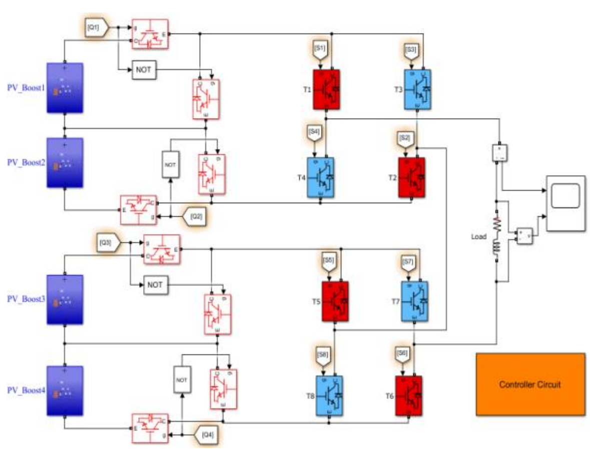


Fig. 4 Model circuit of the 31-level inverter.

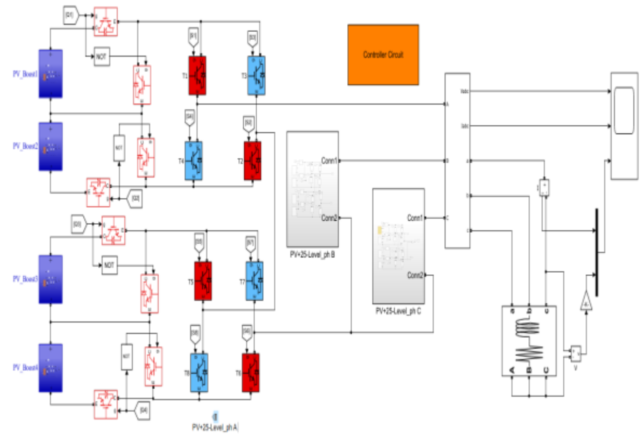


Fig. 5 Three-phase circuit of the 31-level inverter.

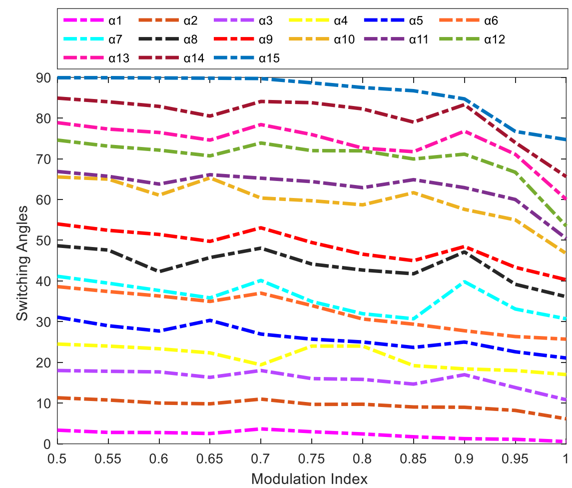


Fig. 6 Switching angles at different modulation index for the single-phase 31-level inverter using PSO algorithm.

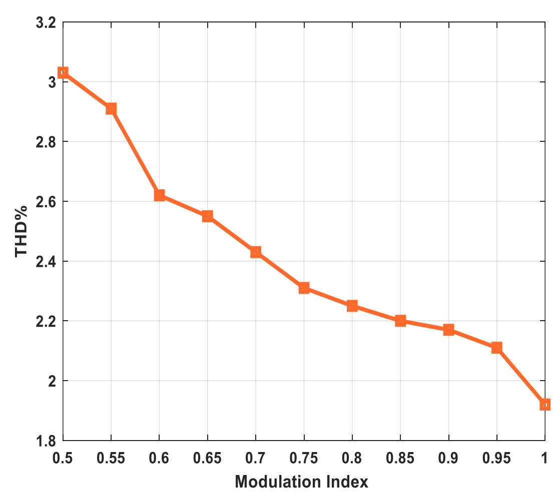


Fig. 7 THD-V values at different modulation index for the single-phase 31-level invert using PSO algorithm.

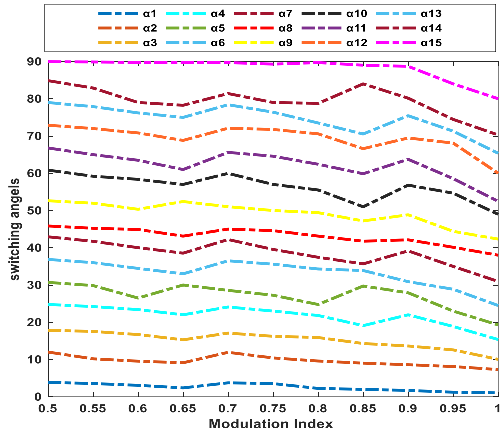


Fig. 8 Switching angles at different modulation index for the three-phase 31-level inverter using PSO algorithm.

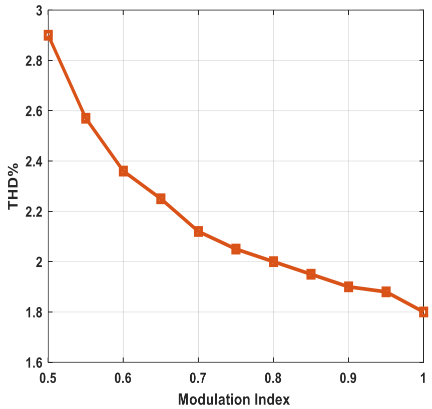
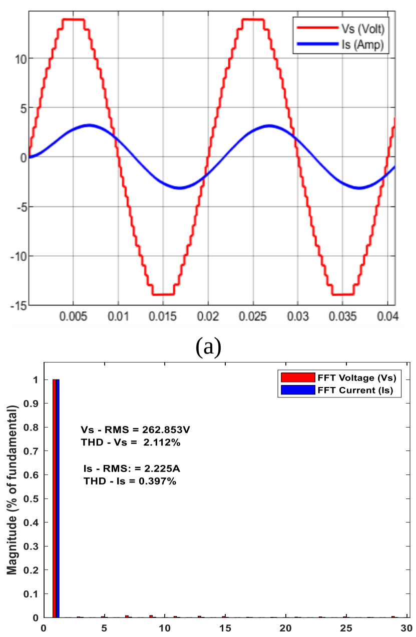


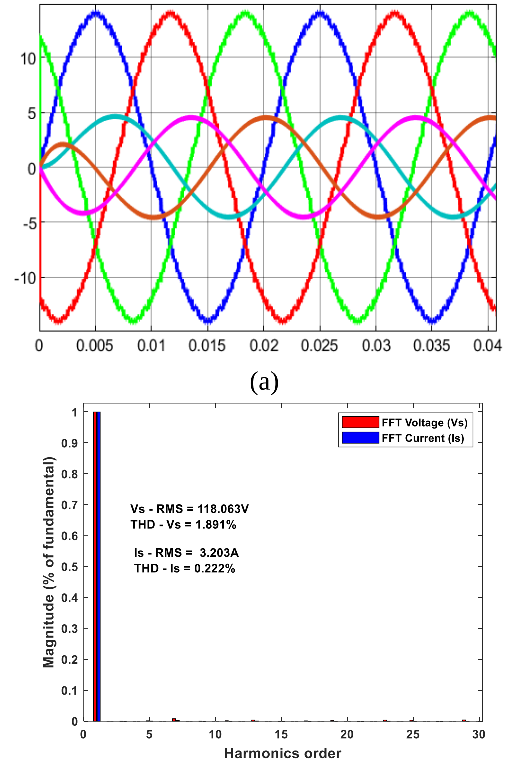
Fig. 9 THD-V values at different modulation index for the three -phase 31-level invert using PSO algorithm.



(a)

(b)

Fig.10 Voltage and current waveform and their FFT of the single-phase 31-level inverter at modulation index (0.95).



(a)

(b)

Fig. 11 Line voltage and current waveform and their FFT of the three-phase 31-level inverter at modulation index (0.95).

6 Practical Configuration

The practical circuit consists of a PV system, multilevel inverter circuit, R-L load, isolator circuit IC TLP (250), FPGA programmed by the Integrated Software Environment (ISE), and Xilinx software package that enables the implementation of the concept project to the FPGA as shown in Fig. 12.

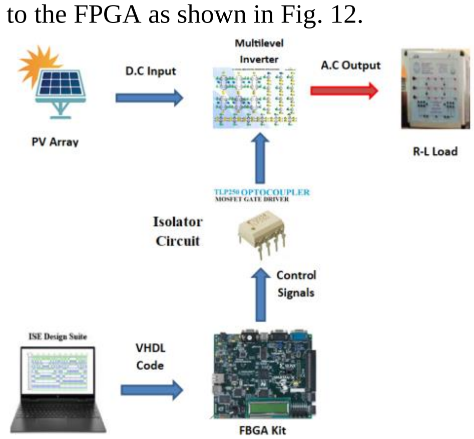


Fig. 12 Schematic diagram of a practical MLI circuit.

7 FPGA Design Flow

The ISE Project Navigator manages and processes the design idea through the following stages as illustrated in Fig. 13 that depicts the flowchart of the FPGA design

flow:
1. Design Entry
Using a Verilog Hardware Description Language (VHDL), the source files are created at this step is built based on the proposed project requirements.
2. Synthesis
After design items and any optional simulation, the synthesis stage should be carried out. Currently, it is being checked.
3. Implementation
During design the implementation circuit, the logical design is converted into a physically formatted file and transferred to the preferred device.
4. Verification
Verifying a design assessing with its performance and utility.
5. Configuration
Creating and downloading the configuration file at the FPGA kit from a host computer is the last step.
6. Programming via ISE/iMPACT

The success that the ISE/iMPACT software presented after testing the program at the FPGA.

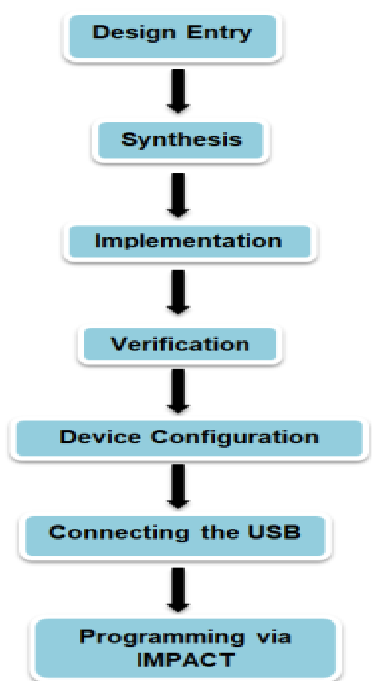


Fig. 13 Flowchart of the FPGA design flow.

8 Design Single Phase 31-Level (VS-MLI)

In this part, the 31-level inverter circuit shown in Fig. 14 is designed and built practically. The simulation and practical outcome results are compared. A prototype circuit shown in Fig. 14 was built using the experimented power board shown in Fig. 12 by employing sixteen power MOSFET switches. The input DC voltage sources are arranged with the structure of (1:2:4:8)*Vdc and values of 3V, 6V, 12V, and 24V to realize the circuit as planned in the proposed topology. The prototype power circuit requires sixteen opto-couplers IC TLP (250). The system is tested practically at different inductive loads with values of (R =100 Ω, 50Ω, 100 Ω, 150 Ω) and (L= 75mH, 150mH, 250mH).

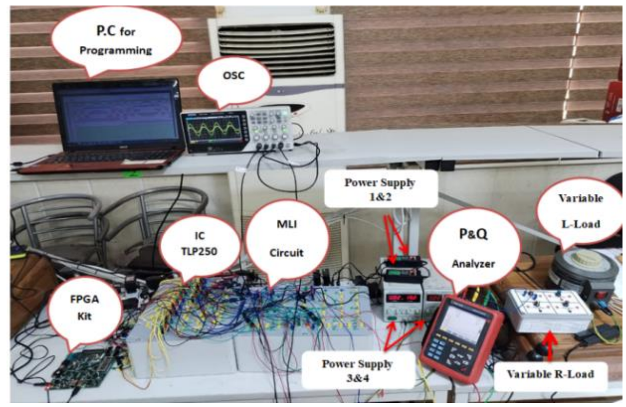


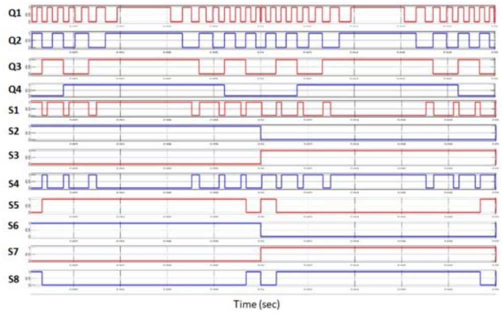
Fig. 14 Prototype of 31-Level.

9 Experimental results

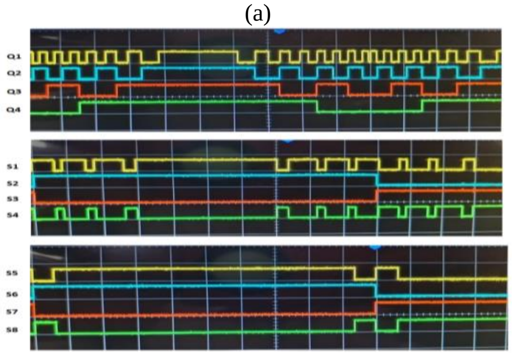
Fig. 15 illustrates the output pulses outcomes from MATLAB simulation and OSC output from FPGA that used to drive the inverter switches. Figs. 16 to 19 show the simulation and practical results of the output voltage and current waveforms at different loads as shown in Table 2. While Figs. 20 to 23 illustrate the FFT spectrum analysis waveforms with their THD values by comparing the simulation and practical results at different loads. The power quality analyzer shows that the THD-V and THD-I are equal to 2.9% at load 1, 2.6% and 2.3% at load 2, 2.5% and 2.1% at load 3, and 2.4% and 1.98% at load 4, respectively. These results are nearly closed to the simulation results which THD values are 2.1054% at resistive load 1, 2.106% and 1.8426% at load 2, 2.085% and 1.8183% at load 3, and 2.105% and 1.8891% at load 4, respectively. If we make a comparison, the THD values are almost matches and all these results are within the IEEE standards. As a results, the proposed and designed power circuits and controllers of the 31-level inverters are effective and efficient to be built and implemented practically in industrial systems. Table 3 shows the comparisons between the proposed circuit and different topologies.

Table 2 Types of used loads

Loads	values
Load 1	100Ω
Load 2	50Ω+75mH
Load 3	100Ω+150mH
Load 4	150Ω+250mH

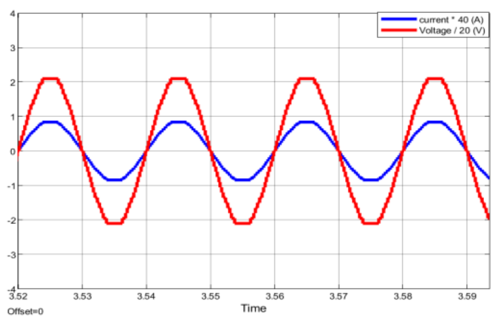


(a)

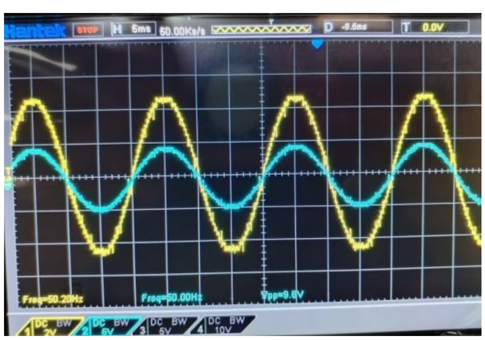


(b)

Fig. 15 The switching pulses of the 31-level inverter (a) MATLAB simulation, (b) OSC output by FPGA Kit.

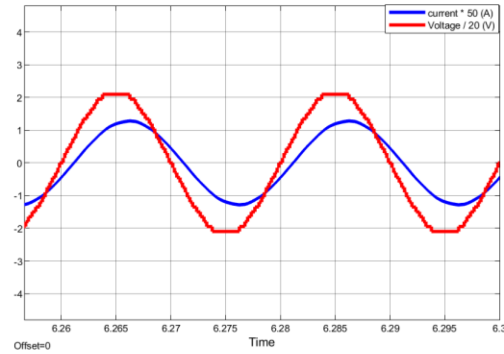


(a)

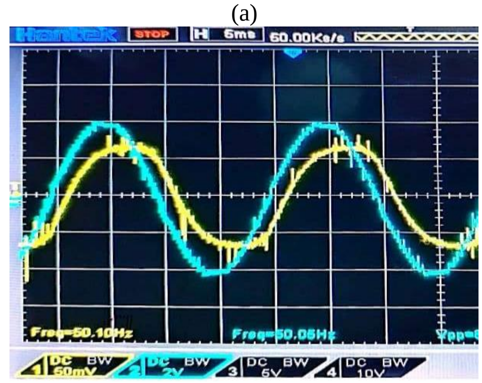


(b)

Fig. 16 Comparison results of the output voltage and current waveforms of the 31-level inverter (a) simulation, and (b) practical results at Load of R=100Ω.

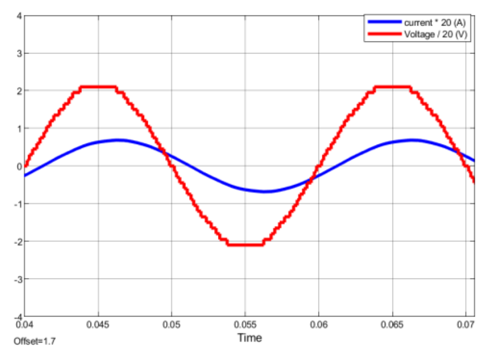


(a)



(b)

Fig. 17 Comparison results of the output voltage and current waveforms of the 31-level inverter (a) simulation, and (b) practical results at Load of R=50Ω and L=75mH.



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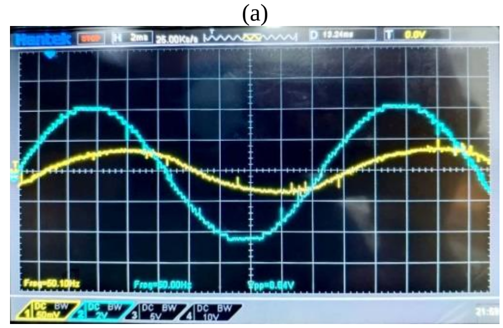
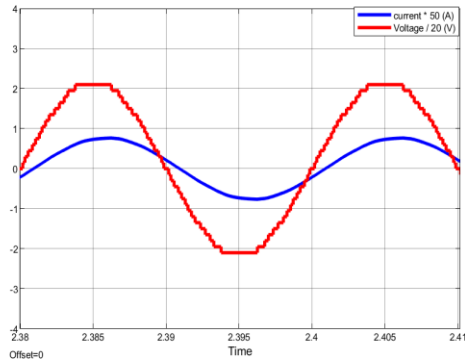


(b)

Fig. 18 Comparison results of the output voltage and current waveforms of the 31-level inverter (a) simulation, and (b) practical results at Load of R=100Ω and L=150mH.



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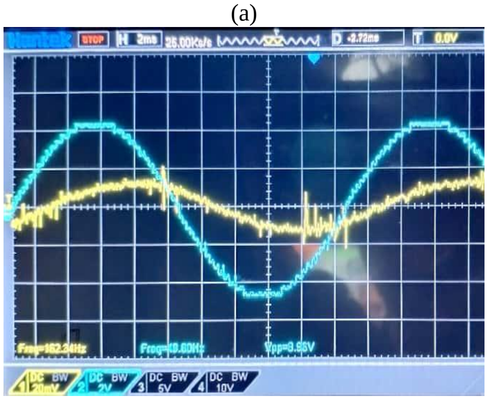
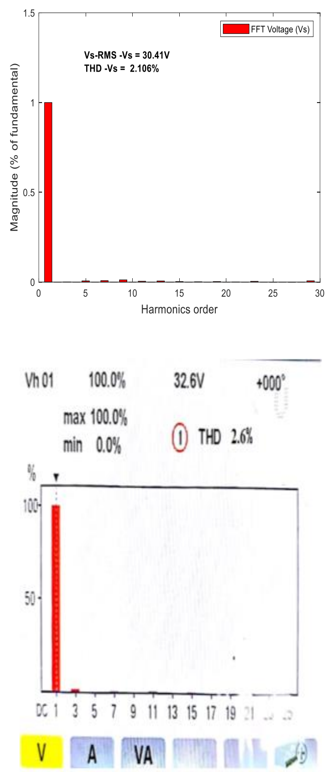
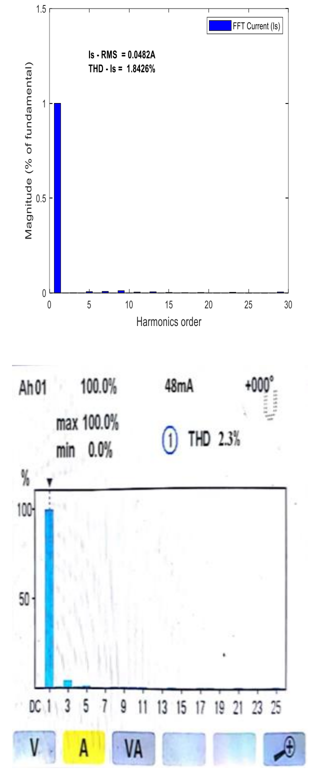


(b)

Fig. 19 Comparison results of the output voltage and current waveforms of the 31-level inverter (a) simulation, and (b) practical results at Load of R=150Ω and L=250mH.

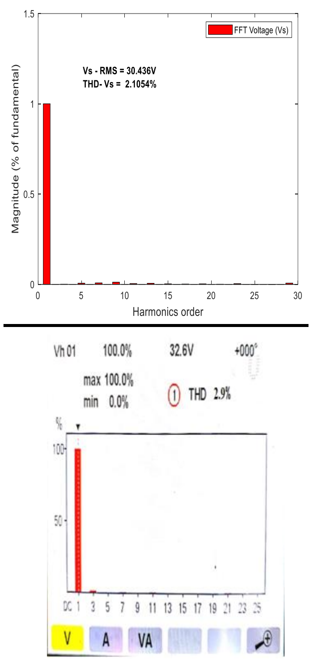


(a)

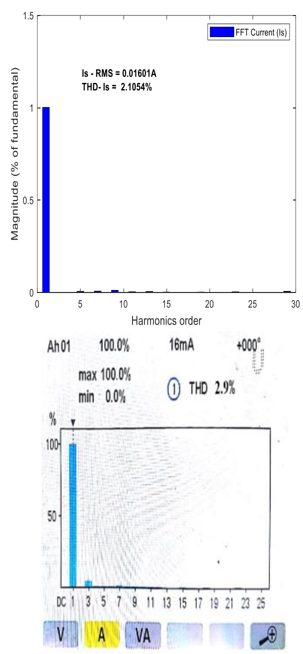


(b)

Fig. 21 The simulation and practical FFT spectrum analysis with the THD values of (a) the output voltage and (b) current at load R=50Ω and L=75mH.

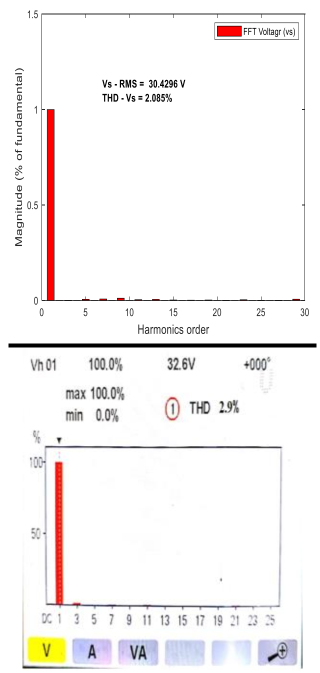


(a)

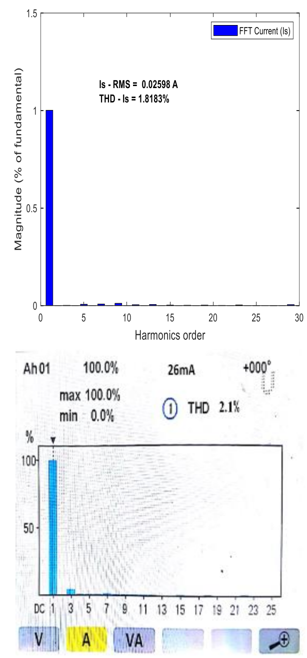


(b)

Fig. 20 The simulation and practical FFT spectrum analysis results with the THD values of (a) the output voltage and (b) current at load R=100Ω.

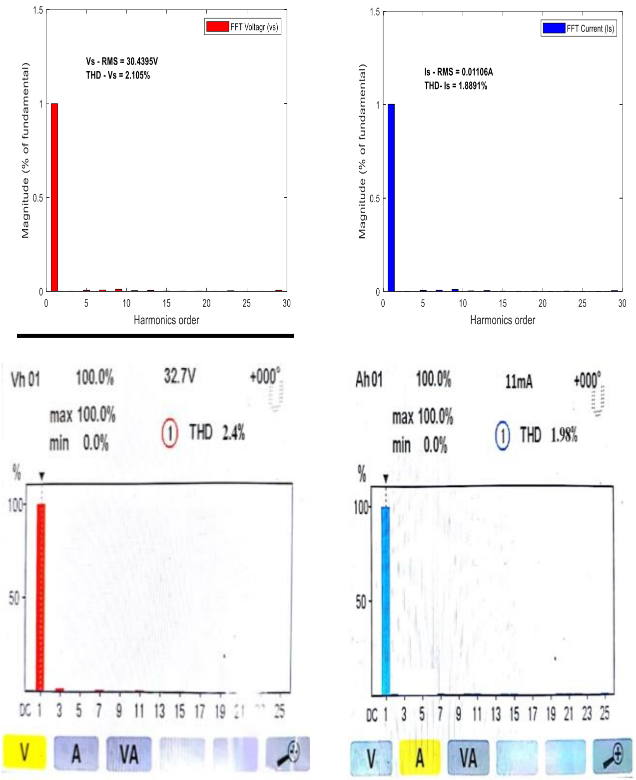


(a)



(b)

Fig. 22 The simulation and practical FFT spectrum analysis with the THD values of (a) the output voltage and (b) current at load R=100Ω and L=150mH.



(a) (b)

Fig. 23 The simulation and practical FFT spectrum analysis with the THD values of (a) the output voltage and (b) current at load R=150Ω and L=250mH.

Table 3 Comparison the proposed circuit components and results with related topologies

Ref.	No. of levels	No. of switches	No. of Sources	THDV
[29]	31-level	10	6	3.2%
[30]	31-level	12	4	4.66%
[31]	31-level	16	4	3.32%
[32]	31-level	12	7	2.52%
Proposed circuit	31-level	16	4	2.4%

10 Conclusion

The acquired angle values demonstrate that while the PSO approach was effective in solving the nonlinear SHE equations, it required many attempts to provide the best outcome. PSO approach may be used with any type of level inverter and minimizes THD for uneven DC sources. PSO technique achieves minimum THD for unequal DC sources, and can be applied for any kind of level inverter. For 31-Level and different loads conditions, the maximum and minimum THD-V values based on simulation data were 2.12% and 2.01%, while practically were 2.9% and 2.4%. At the same time, the maximum and minimum THD-I were 2.12% and 1.80%, and practically equal to 2.9% and 1.98%. Based on the overall results, the THD values of the voltages and currents are within the IEEE standards. The suggested power circuits and designed controllers demonstrate the effectiveness of the modelling systems. These systems can be used in industrial applications and they are applicable and easy to build practically. After verifying these circuits by MATLAB program, the practical and experimental prototype models are built to prove these results.

Conflict of Interest

The authors declare no conflict of interest.

Author contribution

Rakan proposed and designed the circuit, Ali developed the theory, performed the computations, verified the analytical method. **Rakan and Ali** investigated the idea by modeling the system under supervision of **Abdul Ghani**. All authors wrote the manuscript, discussed the results, commented on the manuscript, contributed with the designed system, implemented the research, and writing the final manuscript.

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