

Design and Analysis of Double Channel Organic Field Effect Transistor with Bottom Gate

Arun Pratap Singh Rathod*, Pawan Kumar Mishra**^(C.A.) and Abhilasha Mishra***

Abstract: In recent years, organic field effect transistors, also known as OFETs, have witnessed a substantial demand, mainly due to their expanding applications in the display and sensor industries, owing to simple fabrication techniques and cost-effective raw materials. But due to limited charge mobility, its applications are mostly focused on non-computing applications. Since OFETs are fundamental elements employed in an electronic circuit, the performance of the whole electronic device is correlated with its performance. The development of high performance OFET is particularly beneficial for establishing non-silicon-based chip manufacturing in developing countries worldwide. In an attempt to develop a high performance OTFT, double channel bottom gate organic field effect transistor (DCBG OFET) is proposed in this research article. DCBG OFET or OTFT is a single gate device comparable to a bottom gate bottom contact (BGBC) OTFT in structure, but it generates 4 times higher drain current in its conduction channel with identical material composition and structural dimensions compared to its analogous. A comprehensive comparative study has been presented here investigating performance parameters like transconductance, threshold voltage, subthreshold slope, linear and saturation mobility, etc., to determine the functional superiority of the DCBG OFET over other single gate OTFT structures like BGBC, top gate bottom contact (TGBC), and bottom gate top contact (BGTC) OTFTs. It has been observed that DCBG OTFT exhibits a four-fold improvement in the drain current with respect to conventional single gate OTFTs, and staggering 300% enhancements in parameters like transconductance, linear and saturation mobility are also observed in DCBG OFET over other OTFT architectures with matching material configuration and structural dimensions, operational under the identical voltage conditions.

Keywords: Double conduction channel; OTFT; BGBC; DCBG; OFET; Drain current.

1 Introduction

THE Remarkable growth has been achieved in the field of organic electronics predominantly in the

manufacturing of organic thin film transistors (OTFT) or organic field effect transistors (OFET) over the last two decades. This rise in demand for OFETs could be attributed to device flexibility, low-cost fabrication techniques, and development of new organic semiconductors with enhanced mobility [1]. Due to their inherent benefits organic devices are widely used in different application domains, like RFIDs [2], displays based on OLEDs (organic light-emitting diode), sensors [3] and logic circuits etc. Though recent developments in terms of mobility of organic semiconductors materials have improved significantly but compared to inorganic semiconductors like silicon, it is still quite low limiting its application in commercial computational circuits. Therefore, to overcome this problem, modification in structural parameters and alteration in electrode position

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to improve the output current characteristics could be the way forward. Over the years, various OTFT structures with different material combinations, electrodes positions and dimensions have been proposed and tested to enhance drain current primarily. Such OFET structures generally employ single gate architectures like top contact bottom gate, top gate bottom contact, top contact top gate etc. due to its ease of fabrication [4], [5]. One of these structures, bottom gate bottom contact (BGBC) OTFT is widely used by the virtue of its robust performance fabrication ease [6]. However, different approaches have been considered by several researchers to improve the drain current levels like double gate OTFT structures by incorporating an additional gate and dielectric layer in the structure of BGBC OTFT [7]. This structural modification improved the drain current level by facilitating greater accumulation charges in the channel region, thereby strengthening the conduction channel. However, DG OTFT also exhibited several limitations, like unwanted increment in the device size. Further it was also found that contamination occurs during the process of depositing additional dielectric layer above the organic semiconductor layer (OSC), affecting the device performance negatively [6], [8]. Consequently, numerous novel OFET architectures, such as cylindrical and vertical OTFTs, have also been considered. Such non-conventional structures may offer certain advantages but their limitations including complicated fabrication process, non-regular sizes, structural complexities, operational specificity restrict their application compared to a conventional BGBC OTFT [9].

Therefore, a novel organic field effect transistor has been proposed here, comprising a bottom gate configuration with dual conduction channel. The proposed double channel bottom gate organic field effect transistor (DCBG OFET) incorporates the architectural simplicity of BGBC OTFT but capable enough to generating four times higher drain current when equated to a BGBC OTFT of identical material composition, size and functional under matching operating voltages. A comprehensive investigative study is presented here to compare the performance parameters of DGBC OFET with other similar single gated devices like BCBG, TGBC, and BGTC OTFT to discuss their merits and limitations. Further the reasons for the disparity in performance of these structures have been identified and discussed in detail to achieve better understanding of the operational processes of such OFET architectures and discover new avenues for performance enhancements forging the path for the future developments in the organic transistors.

2 Methodology

A sequential research methodology was used to perform parametric analysis of the concerned OFET

architectures used in this study. The setup for in silico analysis of OFETs included ATLAS TCAD tool from Silvaco. The model used for the analysis of charge carrier mobility was Poole-Frenkel mobility [10]. This model explains the intricacies related to mobility of charges in the semiconductor materials due to the electric field effect within predefined boundary conditions [11]. Mathematically Poole-Frenkel mobility model is given by:

$$\mu(E) = \mu_0 \exp \left[-\frac{A}{kT} + \left(\frac{\beta}{kT} - \gamma \right) \right] \quad (1)$$

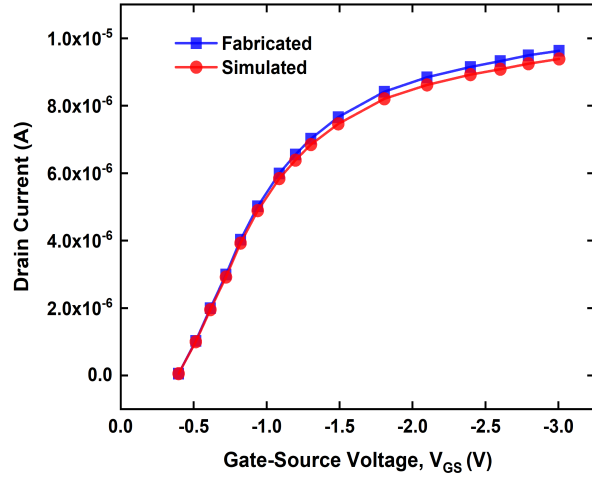
Here Boltzmann constant is denoted by k , T is temperature, $\mu(E)$ represents field assisted mobility, E is electric field, and μ_0 represents charge mobility at zero electric field respectively. Also, β indicates Pool-Frenkel factor for holes & Δ represent the activation energy at zero-field effect, and γ is fitting parameter. This model calculates the conduction parameters related to trapped charges induced by thermal excitation and applied electric field. These calculations are important as charge carriers get localized near the trap locations and start encircling them, as a consequence the drain current deteriorates in the regions without the presence significant electric field [12], [13].

Also, the parametric effects due to temperature, carrier generation and carrier trap mechanics are also considered while, modelling OTFTs precisely. The in-silico results generated by ATLAS TCAD provide important insights into the correlation between a OTFT architecture and its performance [14]. The comparative study includes different electrical parameters, like threshold voltage, subthreshold slope, mobility etc., to evaluate relative performance of different OTFT structures [15]. Data thus gathered is vital for developing optimized OTFT designs for numerous applications viz. sensors, flexible displays, and logic circuits.

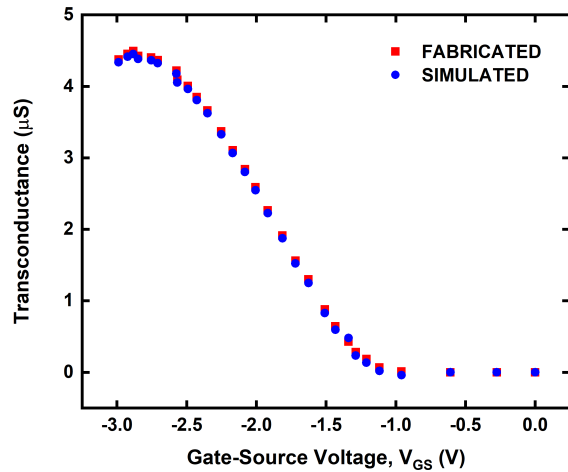
Table 1. Material composition & dimensions of OTFT models used in the validation process.

Physical Parameter	Simulated OTFT	Fabricated OTFT
Channel-Length (μm)	10	10
Channel-Width (μm)	100	100
OSC Layer (material & thickness)	Pentacene (30nm)	Pentacene (30nm)
D and S electrode (material & thickness)	Gold (30nm)	Gold (30nm)
Gate electrode (material & thickness)	Aluminum (20nm)	Aluminum (20nm)
Gate dielectric (material & thickness)	Al_2O_3 (5nm)	Al_2O_3 (5nm)

The in-silico analysis, begin with the validation of a OTFT device model based on fabricated and tested OTFT device to verify the material composition, device size, electrical properties of simulation model against a pretested OTFT developed by Klauk et al. [14], [15], [16]. This process is essential to establish a standard for the assessment of in-silico OTFT model, which will be employed further to develop proposed DCBG OFET.



(a)



(b)

Fig 1. (a) Comparative analysis of transfer characteristics in fabricated and simulated OTFT models; (b) Comparative analysis of transconductance in fabricated and simulated OTFT models.

It has been displayed in Table 1, that physical parameters of different thin films related to the simulated OTFT are identical to the parameters of the OTFT developed by Klauk et al. [16]. These parameters include thickness of the constituent thin films of the OTFT, and different material compositions used in the BGTC OTFT structure, all such parameters are kept same for both fabricated and simulated OTFT. During the in-silico

analysis, the application of suitable potential difference between source and gate electrode generates a conduction channel by facilitating the charge accumulation inside organic semiconductor (OSC) layer at dielectric-OSC interface between drain and source electrode. Thereafter, when required potential difference is applied between source and drain electrode, the accumulated charges proceed towards drain electrode from source electrode constituting drain current in simulated BGTC OTFT, equivalent to the channel formation in the OTFT fabricated by Klauk et al. As observed from the Fig. 1(a), there is no significant difference between the drain current trends associated with simulated and fabricated BGTC OTFT. Similarly, Fig. 1(b) demonstrates the transconductance characteristics of the simulated OTFT fabricated OTFT. It could be clearly observed from the Fig. 1(b) that the simulated device closely follows the trends of fabricated device. The different magnitudes of various performance parameters associated with simulated and fabricated OTFT are recorded in Table 2, indicating slight variations in the performance of the two OTFTs.

Table 2. Comparative analysis of different pperformance parameters associated with fabricated and simulated BGTC OTFT.

Physical Parameter	Fabricated OTFT	Simulated OTFT
Gate to Source potential, V_{GS} (V)	0 to -3	0 to -3
Drain to Source potential, V_{DS} (V)	0 to -3	0 to -3
Drain current, I_{DS} (μA)	5	4.93
Ratio of 'ON' and 'OFF' current	7.03×10^7	6.88×10^7
Transconductance, g_m (μS)	4	3.87
Saturation mobility, μ_{sat} ($cm^2/V \cdot s$)	0.40	0.38
Threshold voltage, V_{th} (V)	-1.20	-1.23
Sub-Threshold Slope, SS (V/dec)	0.074	0.078

Since it is evident from Table 2, that the performance of simulated and fabricated OTFT is nearly identical, the material composition, dimensions, operating voltages, and simulation model stands validated including the operating principal and internal device physics. Consequently, it safe to assume that validated thin films, device dimensions and operating voltages could be reliably used for further device development and analysis. It is vital to understand that all subsequent structures of OTFT produced in this research work are derived from the validated BGTC structure, employing the identical materials and dimensions with only change in the device architectures.

Table 3. Different physical dimensions & materials used in analysis of DCBG OTFT and other single gate OTFT structures.

Physical Dimensions and Materials	BGBC OTFT	TGBC OTFT	BGTC OTFT	DCBG OTFT
Length of Channel	18 μm	18 μm	18 μm	18 μm (9 μm +9 μm)
Width of Channel	100 μm	100 μm	100 μm	100 μm
Organic semiconductor (thickness and material)	80nm, Pentacene	80nm, Pentacene	80nm, Pentacene	80nm, Pentacene
D and S electrode (thickness and material)	60nm, Gold	60nm, Gold	60nm, Gold	60nm, Gold
Gate electrode (thickness and material)	20nm, Aluminium	20nm, Aluminium	20nm, Aluminium	20nm, Aluminium
Gate dielectric (thickness and material)	10nm, Al_2O_3	10nm, Al_2O_3	10nm, Al_2O_3	10nm, Al_2O_3

The physical parameters like dimensions of thin films and their material composition of the DCBG and other single gate OTFTs including BGBC OTFT, top gate bottom channel (TGBC) OTFT, bottom gate top channel (BGTC) OTFT devices have been recorded in Table 3. These parameters were used for the in-silico development of the concerned OTFT structures for further analysis and comparative study. The overall dimensions, including the material and thickness of individual layers are identical for all the OTFTs. The conventional BGBC, TGBC and BGTC OTFT furnish a 18 μm long single conduction channel whereas the DCBG OFET possess two conduction channels of 9 μm each. Hence the total channel length of DCBG becomes equivalent to the channel length of BGBC device. Two smaller channels provide higher current density and contribute significantly to the overall drain current enhancement in DCBG OFET. The OTFT structures presented here in Table 3 are discussed elaborately in the forthcoming sections elucidating the structural nuances, operational physics, functional variations and performance parameters in detail establishing the performance superiority of DCBG OFET over the conventional devices like BGBC, TGBC and BGTC OTFT.

3 Operational variations with respect to BGBC OTFT and novelty of DCBG OFET

A conventional BGBC OTFT is one of the elementary units of any organic electronics circuit. It is comprised of three different electrodes viz. the source, drain and the gate electrode [7]. The operating principal of a bottom gate bottom gate OTFT is comprised of two distinct processes that include accumulation of the charge carriers in the conduction region thereafter movement of accumulated of accumulated charge from source to drain electrode forming a conduction current. During these processes the source electrode provides the entrance to the charge carriers into the conduction region within organic semiconductor (OSC) layer or active layer. On applying suitable potential difference between the source

and drain electrode, positive or negative charges depending on the type of OSC material are injected at the OSC-dielectric through source electrode in accordance with the electrode-OSC energy gap [17]. Similarly, the modulation of conduction channel by altering the number of charge carriers in the conduction region is achieved through gate electrode affecting the overall conductivity of the device.

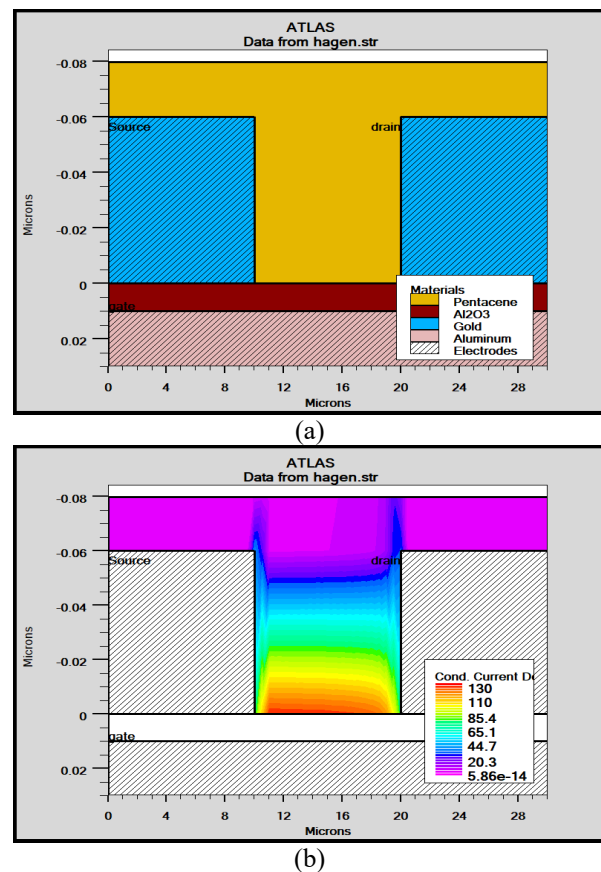


Fig 2. (a) 2-D simulated of an OTFT in BGBC configuration; (b) Visualization of drain current density in the conduction channel region.

The potential difference applied at the gate electrode defines the electrostatic force of attraction experienced by the charge carriers, thereby controlling movement of charges within the conduction region [18].

A thin insulation layer is used to block unwanted tunnelling of charges between the OSC and gate terminal. This insulation (dielectric) layer is sandwiched between the OSC layer and gate electrode. The selection of dielectric layer is important as high value of dielectric constant results in low leakage current and facilitates modulation in the conduction channel efficiently [19]. The potential difference between source and drain causes charge movement from source to drain electrode. Due to the potential gradient charges drift into the conduction channel, consequently generating conduction current. Modulation in gate potential results in charge modulation in conduction channel that led to increment and decrement in the drain current. This implies that higher gate voltage attracts large number of charge carriers, resulting in greater drain current, while lower drain current is obtained when lower voltage is applied at the gate terminal due to reduced number of charges carriers in the conduction channel [20].

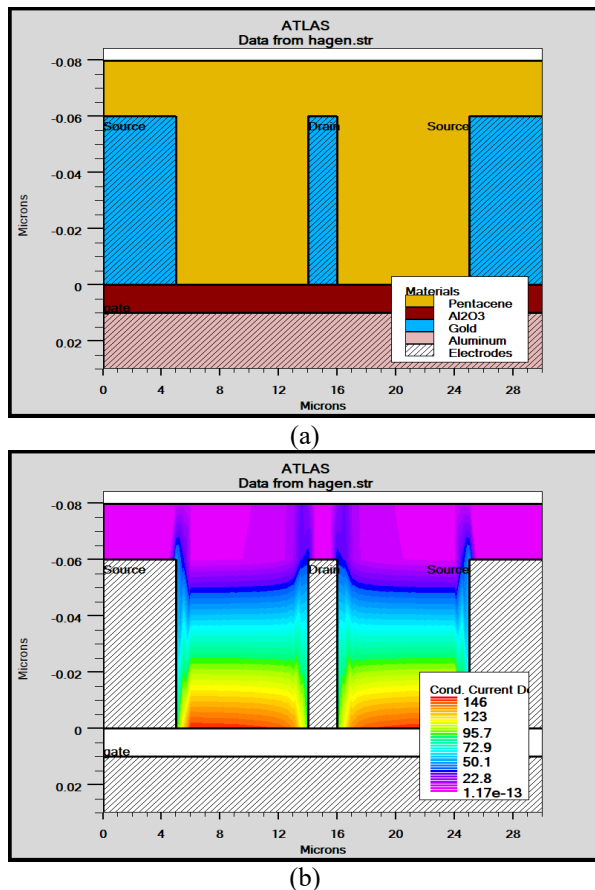


Fig 3. (a) 2-D structure of DCBG OFET; (b) Conduction current density in DCBG OFET under external voltage biasing.

To validate the principle of operation related to BGBC OTFT, the two-dimensional simulated structure of the device along with the highlighted conduction channel has been examined. As illustrated in Fig. 2(a) the BGBC structural layout is comprised of an aluminium gate electrode, source and drain electrodes of gold, an active (pentacene) layer and a thin layer of aluminium oxide as dielectric. Further in Fig. 2(b) the channel region within the active layer is highlighted, where the propagation charge carriers from source to drain electrode results in the formation of conduction current. The charges in the channel are moderated by gate potential and hence it controls the quantum of conduction current in the device [21]. Consequently, the BGBC device operations includes the injection of charge carriers in a controlled manner via source, which are moderated by the gate potential and collected at the drain terminal as discussed earlier. Therefore, the theoretical principle of BGBC OTFT has been validated with the operation of the simulated BGBC device. The passivation through the dielectric layer in the final step of fabrication ensures operational efficiency by preventing charge migration from adjacent devices in an integrated circuit setup and protecting device from environmental factors like humidity and external heat [22], [23]. To Understand the operational physics of the BGBC OTFT is crucial for exploring the factors responsible for performance enhancement and its possible applications.

The double channel bottom gate OFET is a variant of single gate BGBC structure. DCBG architecture is novel from other single gate architectures as it displays a unique central drain electrode flanked by source electrodes on either side splitting the single conduction path into two analogous conduction channels as shown in Fig. 3(b), effectively enhancing the current driving capability of the OTFT with constant footprint, leading to greater symmetry in charge transport and minimizing the contact resistance. Consequently, it reduces complexity in interconnections and finds suitability in the layouts of integrated circuit where routing line minimization is crucial. DCBG OFET integrates the aluminium gate electrode in the bottom position like BGBC OTFT configuration. Similarly, a dielectric layer comprising Aluminium oxide (Al_2O_3) is deposited above the gate electrode to limit the undesired movement of charges between the gate and active layer [24]. In a novel attempt instead of depositing a source and a drain electrode in a conventional setting, a central drain electrode composed of Gold (Au) is deposited followed by the deposition of source electrodes (Au) on either side of drain over the dielectric layer at the lateral margins, breaking the single channel into two smaller channels. Subsequently, an 80nm thick active layer comprised of pentacene is deposited over the dielectric layer embedding the electrodes, hence completing the device structure. The device architecture of the double

channel bottom gate organic field effect transistor is illustrated in Figure 3(a). The distinctive electrode configuration of the DCBG OFET facilitates the development of two independent conducting channels inside the organic semiconductor (OSC) or active layer. These channels arise from the application of an external electric field, as previously reported [25], [26]. As shown in Figure 3(b), Channel-1 is established between source1 and the central drain electrode, while Channel-2 is formed forms between source-2 and the central drain electrode.

Majority charge carriers (holes or electrons) within each conduction channel migrate from the respective source electrodes towards the common drain electrode, depending on the type of semiconductor material. Both channels exhibit identical length and comparable current density, resulting in similar charge carrier transport characteristics [27]. For operational simplicity, the two source electrodes are interconnected externally to form a combined source node, streamlining electrical interconnections and signal routing [28]. The electrical behaviour of each channel adheres to fundamental charge transport principles, significantly influencing device performance, particularly drain current [29]. The DCBG OFET's unique bottom-gate, central source, and paired drain electrode configuration enables the formation of two parallel conducting channels within the organic semiconductor layer. To further analyse the device's performance, a thorough investigation is done related to twin channel formation within the dual-channel architecture.

The interconnected drain electrodes effectively convert the DCBG OFET into a three-terminal device with distinct properties compared to conventional bottom-gate, bottom-contact (BGBC) OTFTs. The central drain and paired source electrodes in the DCBG OFET result in a Source-Drain-Source (SDS) configuration, leading to two equally sized conduction channels (L_1 and L_2). This configuration contrasts with the BGBC OTFT of same dimensions with single conduction channel. The DCBG OFET architecture features a 50% reduced channel length of individual channels ($L_1, L_2 = L/2$) relative to the conventional BGBC OTFT (L), while maintaining invariant channel width (W), carrier mobility (μ), gate-source voltage (V_{GS}), drain-source voltage (V_{DS}), and oxide capacitance (C_{ox}). To quantitatively measure the correlation between channel length moderation and output drain current. To achieve this a mathematical analysis of the current-voltage characteristics was conducted. The resulting equations, presented as Equations (2) to (8), provide a framework for understanding the performance implications of channel length reduction in the DCBG OFET.

For the BGBC OTFT, the drain current ($I_{DS(BGBC)}$) can be expressed as Equation (2):

$$I_{DS(BGBC)} = \frac{W\mu C_{ox}}{L} \left\{ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right\} \quad (2)$$

where V_T denotes the threshold voltage, a critical parameter defining the onset of channel conduction. The drain current is expressed as a function of key device parameters, including channel length, width, carrier mobility, V_{GS} , V_{DS} , and C_{ox} . The expression presented here is derived from the simplified model of charge carrier transport in the conduction channel, asserting a linear relationship between current and electric field (Ohm's law). The term $(V_{GS} - V_T)$ represents the voltage above the threshold voltage (overdrive voltage) required to generate a conducting channel.

For DCBG OFET, the drain current ($I_{DS(DC)}$) is given by:

$$I_{DS(DC)} = \frac{W\mu C_{ox}}{L_1} \left\{ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right\} + \frac{W\mu C_{ox}}{L_2} \left\{ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right\} \quad (3)$$

Here L_1 and L_2 are the lengths of twin channels formed in DCBG OFET. The existence of two parallel conduction channels present in the DCBG OFET is mathematically represented here. The total drain current in dual channel device is the sum of the currents flowing through each channel. On further simplifying equation (3) after rearrangement, we get:

$$I_{DS(DC)} = \frac{1}{L_1} + \frac{1}{L_2} \left[W\mu C_{ox} \left\{ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right\} \right] \quad (4)$$

Simplifying equation (4) while taking $L_1 = L_2 = L/2$, following expression is obtained:

$$I_{DS(DC)} = \frac{1}{L/2} + \frac{1}{L/2} \left[W\mu C_{ox} \left\{ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right\} \right] \quad (5)$$

Further simplification of equation (5) yielded:

$$I_{DS(DC)} = \frac{2}{L} + \frac{2}{L} \left[W\mu C_{ox} \left\{ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right\} \right] \quad (6)$$

On simplifying Equation (6) the obtained expression is represented as Equation (7)

$$I_{DS(DC)} = \frac{4}{L} \left[W\mu C_{ox} \left\{ (V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right\} \right] \quad (7)$$

The DCBG OTFT exhibits a substantial enhancement in drain current ($I_{DS(DC)}$), with a value four times greater than that of the BGBC OTFT ($I_{DS(BGBC)}$), as expressed in Equation (8):

$$I_{DS(DC)} = 4(I_{DS(BGBC)}) \quad (8)$$

This reveals that the generated drain current in DCBG OFET is four times that of a BGBC OTFT with the same dimensions and operating voltages. The increased drain current in the DCBG OFET could be primarily attributed to the presence of twin parallel conduction channels. This effectively doubles the channel width, leading to a corresponding increase in current. Mathematical derivation confirms this phenomenon. To further validate the device results with mathematical data an additional comparative study was undertaken. The mathematical validation process included calculating the output drain current I_{DS} for 30 different drain to source voltages between 0 to -3V at a constant gate to source voltage of -3V for DGBC OFET using Eq. 7 and comparing each outcome with corresponding drain current obtained after simulating DGBC architecture for same voltage ranges. The 30 outcomes of I_{DS} generated each through mathematical calculations and simulation process then plotted using graph generating tools to present a direct comparison between simulation results and the ideal current conditions produced through mathematical calculations.

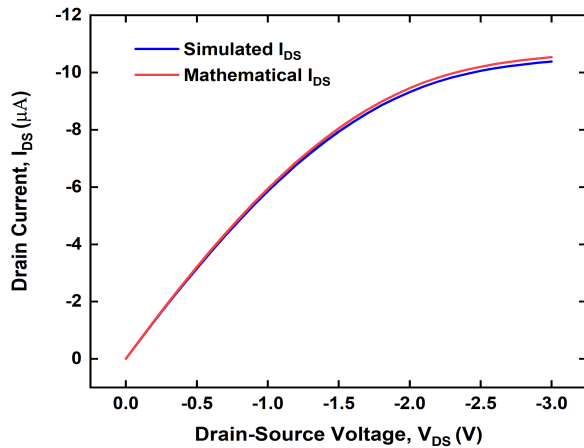


Fig 4. A comparative representation of output drain current response of DC BEBG device achieved through mathematical analysis and simulation of DCBG OFET at $V_{DS} = 0$ to -3V at constant V_{GS} of -3 V.

It is evidently illustrated in Figure 4 that both the simulated and mathematical drain current (I_{DS}) curves exhibit similar trend. As the drain to source voltage (V_{DS}) becomes more negative (from 0 to -3V), the I_{DS} improves. This indicates that the device is operating in the saturation region, and now current is primarily controlled by the gate-source voltage and is relatively independent of the drain voltage. The simulated I_{DS} values are consistently lower than the mathematically predicted values across the entire V_{DS} range. This inconsistency could be attributed to several factors, including parasitic effects, non-ideal channel behavior etc. In simulation parasitic resistances and capacitances have been incorporated and are accounted for but such

defects are not included in the mathematical model. Moreover, the mathematical model might assume an ideal channel, while the simulation considers real-world effects like carrier mobility variations and channel length modulation. In spite of these discrepancies there is only a divergence of only 1.43% in the final I_{DS} results. Hence the mathematically generated results validate the simulated device results.

The DCBG OFET, characterized by its distinctive electrode arrangement and bifurcated conduction channels, exhibits a quadrupled drain current relative to the conventional BGBC OTFT. This performance enhancement is attributed to channel length reduction while preserving charge carrier density within the channels. Notably, the cumulative channel length of the DCBG OFET equals that of the BGBC OTFT, ensuring identical device dimensions and material composition. The presented equations (2 to 8) quantitatively illustrate the correlation among the drain current, channel length, and other key factors, thus elucidating the performance advantages of DCBG OFET architecture over BGBC architecture.

4 Proposed Fabrication Flow of DCBG OFET

The DCBG OFET is a high-performance single gate OTFT, which can generate four times higher current in conduction channel than other single gate OTFTs like, BGBC, TGBC, BGTC etc. But due to its structural similarities with bottom gate bottom contact architecture, it is quite simple to fabricate just like a BGBC OTFT with exact same number of manufacturing steps employing identical raw materials. The step by step proposed fabrication process has been elucidated in Fig. 5 including the materials and fabrication techniques. The dimensions are given in a range rather than exact figures as user may modify the device size as per the requirement. It worth mentioning here that the performance enhancement achieved in DCBG OTFT is direct result of its novel architecture rather than its size or material composition. The fabrication of DCBG OFET may begin with the deposition of gate electrode (Aluminum) over a glass or flexible plastic substrate using thermal evaporation technique [30]. This technique supports electrode deposition up to a thickness of 100 nm approximately.

Thereafter, a 20 to 30nm thick layer of dielectric material (Al_2O_3) is deposited uniformly over the previously deposited gate electrode layer using Atomic Layer Deposition technique (ALD), followed by annealing of freshly deposited dielectric layer at $\sim 150^\circ C$ in an inert environment for better dielectric properties. In the next step the twin source and central gate electrodes are deposited using the thermal evaporation technique with the help of shadow masking [30]. Proper defining of source and drain electrode is crucial for efficient conduction channel. Good alignment of electrodes

results in well-defined channel region. After this a ~50–80 nm thick organic semiconductor layer (pentacene) is deposited over the dielectric layer encapsulating the source and drain electrodes [30].

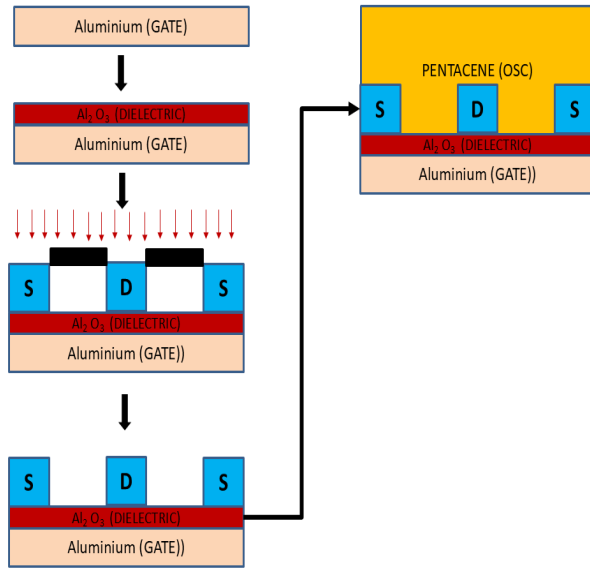


Fig 5. Fabrication flow of DCBG OFET.

The deposition of organic semiconductor layer is achieved through thermal deposition performed in high vacuum conditions ($\sim 10^{-6}$ Torr) inside an inert gas compartment to prevent any kind material degradation due to oxidation. Finally, to protect the device from environmental degradation due to humidity, air exposure etc., a passivation layer of materials like Poly (methyl methacrylate) (PMMA) could be deposited using spin coating. This completes the device fabrication of DCBG OTFT highlighting minimal fabrication steps and simple techniques employed in the process.

5 Results and Discussion

A relative evaluation of the double channel bottom gate organic field effect transistor operating under identical electrical conditions was conducted to elucidate the performance disparity with other device architectures. The experimental findings unequivocally demonstrate a fourfold enhancement in drain current for the DCBG OFET relative to its BGBC counterpart, and significant improvement over single gate OTFT structures like BGTC and BCTG OTFTs despite maintaining identical device dimensions and material composition. As illustrated in Figures 6(a), 6(b), 6(c) and 6(d), the DCBG OFET generates twin accumulation regions and conduction channels compared to single accumulation region and conduction channel developed in the BGBC, BGTC and TGBC OTFT architectures. These results have been achieved without altering the material composition of the devices underscoring the

potential of DCBG architecture to significantly improve the performance metrics of organic thin film devices.

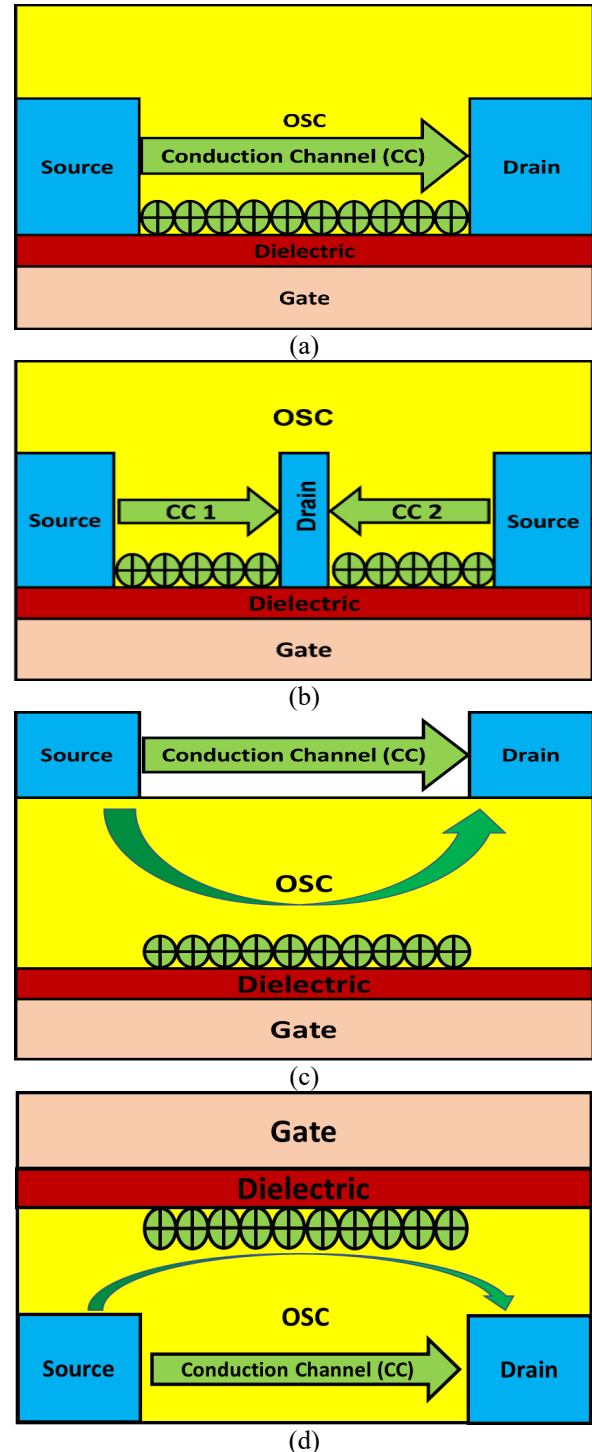


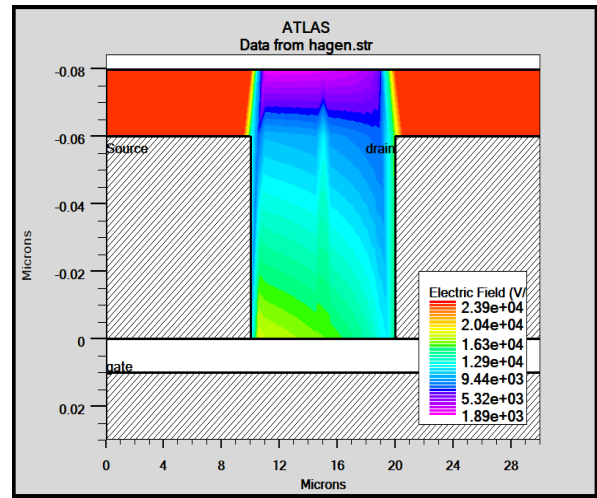
Fig 6. (a) Charge accumulation and conduction channel formation in BGBC OTFT; (b) Charge accumulation and twin conduction channel formation in DCBG OFET; (c) Charge accumulation and conduction channel formation in BGTC OTFT; (d) Charge accumulation and twin conduction channel formation in TGBC OFET.

Table 4. Performance factors comparison of between DCBG OFET and other single gate OTFTs with single channel.

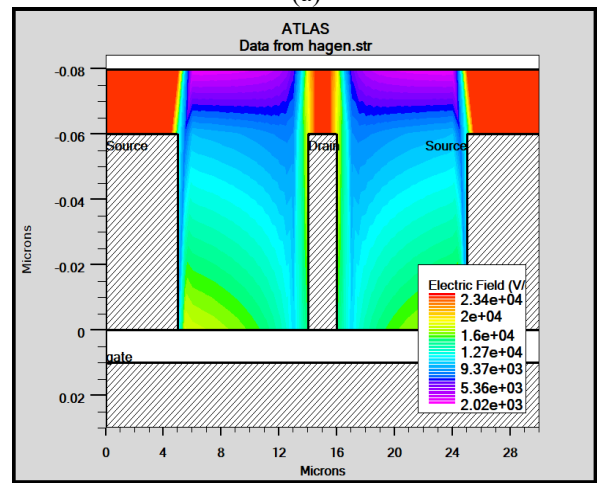
Performance factors	BGBC OTFT	TGBC OTFT	BGTC OTFT	DCBG OFET
Gate_Source_Voltage, V_{GS} (V)	0 to -3	0 to -3	0 to -3	0 to -3
Threshold_Voltage, V_{th} (V)	-1.30	-1.34	-1.39	-1.25
Drain_Source_Voltage, V_{DS} (V)	0 to -3	0 to -3	0 to -3	0 to -3
Mobility_Linear, μ_{linear} ($cm^2/V.s$)	1.68	1.86	1.84	6.56
Output_Drain_current, I_{ds} (μA)	2.02×10^{-6}	2.16×10^{-6}	2.12×10^{-6}	8.07×10^{-6}
I_{ON}/I_{OFF} ratio	110.58	96.19	115.83	378.69
Trans-conductance, g_m (μS)	1.16×10^{-6}	1.30×10^{-6}	1.29×10^{-6}	4.59×10^{-6}
Mobility_saturation, μ_{sat} ($cm^2/V.s$)	0.102	0.107	0.104	0.416
Sub-Threshold_Slope, SS (V/dec)	0.92	0.89	0.90	0.89

Table 4 presents a comprehensive comparative analysis of different performance parameters belonging to the Dual Channel Bottom Gate, BGTC, TGBC and BGBC Organic Thin-Film Transistor architectures. The table systematically compares key performance metrics, like threshold voltage, maximum drain current, mobility, transconductance, subthreshold slope etc., for each structure providing invaluable insights into the operational characteristics of each device configuration. The results presented here are recorded after successful insilico implementation of DGBC, BGBC, BGTC and TGBC OFETs operating at identical gate to source voltage (V_{GS}) and drain to source voltage (V_{DS}). Detailed examination of individual parameters is further done in the subsequent subsections to elucidate their respective contributions to the overall performance and efficiency of both the OTFT structures.

It has been illustrated in Figure 6 that the electric field distribution within an active layer of BGBC and DCBG OFET plays an influential role in the overall performance of the OTFT devices. As shown in Figures 7(a) and 7(b) the drain and source terminals are responsible for collection and injection of charge carriers. While gate electrode controls the formation and modulation of conduction channel within the organic semiconductor layer and organic semiconductor layer serves as the active layer where charge carriers transport occurs. The electric field intensity is represented by the color gradient in the diagram. It could be clearly observed in Figure 7 that the electric field pattern within the active layer of BGBC and DCBG OFET is completely different owing to the structural differences of the OTFT devices.



(a)



(b)

Fig 7. (a) 2-D structure of DCBG OFET; (b) Conduction current density in DCBG OFET under external voltage biasing.

Due to the central unique central position of the drain electrode the electric field distribution within the active layer of DCBG device has transformed significantly. As the consequence of this novel positioning electric field intensity is notably higher in the regions closer to the drain electrodes compared to the conventional configurations like BGBC. This enhanced electric field can potentially improve the charge carrier mobility and device performance. Moreover, due to the symmetrical arrangement of the twin source and central drain

electrodes, the electric field distribution in the active layer exhibits a symmetrical pattern, improving the transport of charge carriers and reducing the channel variability. Further, the enhancement in the carrier injection and extraction efficiency is also achieved because of the concentration of the intense electric field in the vicinity of the drain electrodes, creating regions of high field strength and significantly reducing the contact resistance.

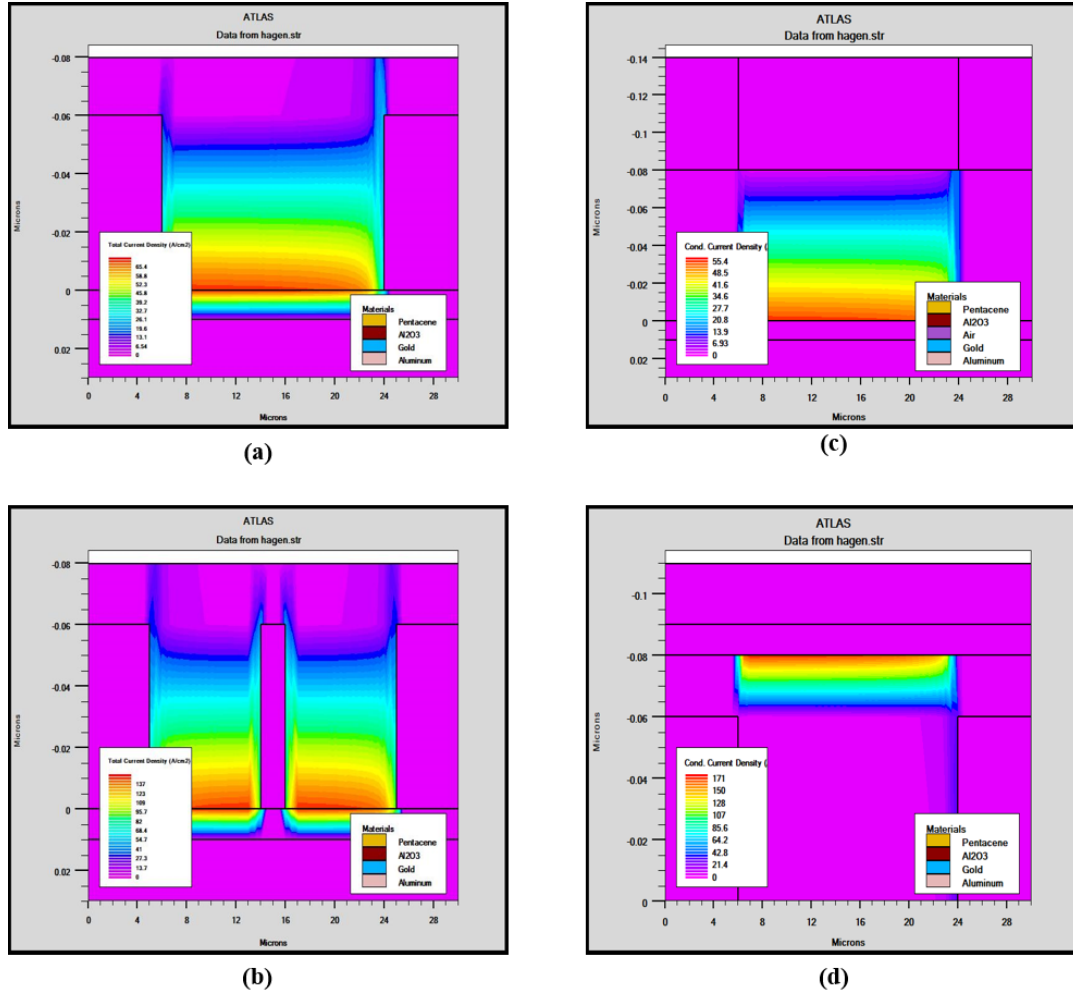


Fig 8. (a) Conduction channel formation in BGBC OTFT; (b) Twin conduction channel formation in DCBG OFET; (c) Conduction channel formation in BGTC OTFT; (d) Conduction channel formation in TGBC OTFT.

These changes in the electric field distribution directly impacts charge carrier mobility within the conduction channel of the device as higher electric field exerts a stronger force on charge carriers, increasing the drift velocity of the charges and consequently enhancing the carrier mobility. Meanwhile, the higher electric field can potentially reduce the probability of carrier trapping by providing sufficient energy for trapped carriers to

escape and generate more uniform and efficient twin conduction channels.

As shown in Fig. 8 owing to its unique electrode configuration the DCBG OFET is proficient in generating highly conductive twin conduction channels with high charge density in contrast to other single OTFT structures which are unable to achieve such a feat despite operating at identical voltages. In Fig 8(a), the BGBC OTFT structure is shown with a single

conduction channel generated between source and drain. Similarly in Fig 8(c) and 8(d), formation of single conduction channels could be seen in BGBC and TGBC OTFTs respectively. It is important to note that all these structures possess identical material composition and dimensions but due to the novel architecture of DCBG OFET, a twin channel geometry is produced inside its active layer unlike other structures. The performance enhancement is not limited only to the generation of twin channel geometry; in fact, it transcends across all the performance parameters recorded in Table 4. Henceforth a brief discussion on each performance parameter mentioned in Table 4 is presented in this section.

Gate to Source Voltage (V_{GS}): It is evident from Table 4 that all devices including DCBG OFET, BGBC, BGTC and TGBC OTFT operate within the identical range of V_{GS} , changing from 0V to -3V. The negative voltage regime here is indicative of positive charge carriers as majority type in the pentacene material. This voltage range induces and control the density of charge carrier in the channel region, altering the OTFT's overall performance [30], [31].

Drain to Source Voltage (V_{DS}): Similar to V_{GS} , the V_{DS} too is varied from 0 to -3V for all the OTFT structures uniformly. Here also the negative voltage here is indicative of positive charge carriers as majority type in the pentacene material. The application of this voltage facilitates the transistor's operation in saturation region, facilitating the movement of charge carriers from source towards drain terminal, increasing the output drain current and enabling OTFT functioning.

Mobility Linear (μ_{lin}): Carrier mobility in the linear region is a critical determinant of charge transport efficiency within the active layer of an organic thin film transistor. Enhanced mobility facilitates unrestricted charge carrier movement through the semiconductor active layer, resulting in increased drain current. The DCBG OFET demonstrated superior linear mobility, with a value of $6.56 \text{ cm}^2/\text{V}\cdot\text{s}$, compared to the $1.68 \text{ cm}^2/\text{V}\cdot\text{s}$, 1.30×10^{-6} , and 1.29×10^{-6} shown by the BGBC, TGBC and BGTC OTFTs respectively. This substantial mobility enhancement in the DCBG OFET enables more efficient charge carrier transport, leading to enhanced overall OTFT performance [32], [33], [34].

Output Drain Current, I_{DS} (Saturation): Drain current is responsible for driving the progressive connected nodes (transistors) in a combinational or sequential electronic circuit. The drain current in saturation is a pivotal performance parameter in organic thin-film transistors (or OFETs). It embodies the charge carrier flow from twin source electrodes to central drain electrode within the semiconductor active layer [33]. This current constitutes the driving force for subsequent circuit elements in both combinational and sequential logic configurations.

$$I_{DS} = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2 \quad (9)$$

Here μ is denoting mobility, while C_{ox} is representing gate oxide capacitance per unit area. The channel width in the equation is represented by W , L is length of conduction channel, gate source voltage V_{GS} , and threshold voltage is V_T [30]. The DCBG device provides significantly higher drain current, amounting to $8.07 \times 10^{-6} \text{ A}$, in contrast to the BGBC, TGBC and BGTC configurations, which provided minimal drain currents in order of $2.02 \times 10^{-6} \text{ A}$, $2.16 \times 10^{-6} \text{ A}$, and $2.12 \times 10^{-6} \text{ A}$ respectively. This significant upgrade in current flow signifies the superior performance of the DCBG OFET due to its central drain (CD) architecture compared to all other single gate architectures considered in this study.

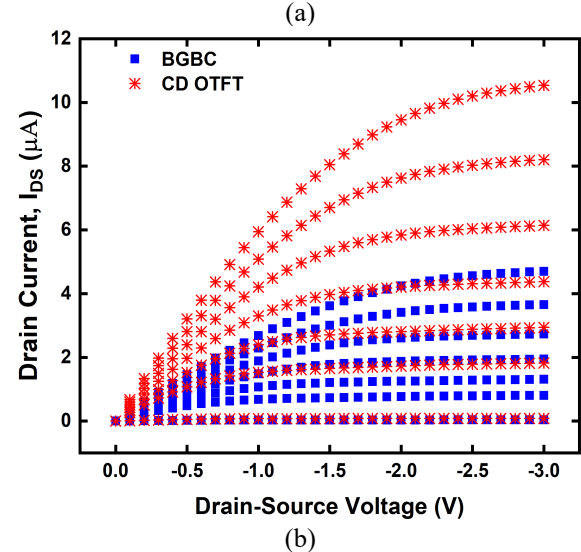
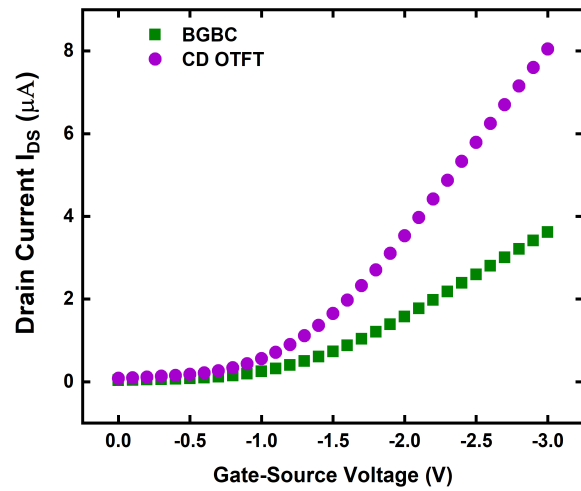


Fig 9. (a) Comparative transfer characteristics of BGBC and DCBG OFET with Central Drain (CD) for $V_{GS} = 0$ to -3V at constant V_{DS} of -3V ; (b) Comparative output drain current characteristics of BGBC and DCBG OFET with Central Drain (CD) for $V_{DS} = 0$ to -3V at constant V_{GS} of -3V .

The provided graph in Figure 7(a) illustrates a comparative analysis of the transfer characteristics between a conventional BGBC Organic Thin-Film Transistor and a DCBG OFET with a central drain (CD) configuration. The V_{GS} is presented on x-axis and the y-axis represents the I_{DS} in microamperes (μA). It is evident from the figure that the increase in drain current of CD configuration is significantly more with respect to BGBC design as the magnitude of V_{GS} becomes more negative. The negative voltage indicates a typical p-type OTFT operation, where a more negative gate voltage induces a higher hole concentration in the channel. The CD configuration not only demonstrates higher drain current across the entire range of V_{GS} but also exhibit a steeper slope than BGBC architecture. This enhancement in performance could be attributed to the enhanced charge carrier transport, higher field-effect mobility, reduced contact resistance between the drain electrode and the organic semiconductor, leading to improved current injection and extraction [32], [33], [34]. Also, the improved electric field distribution in the CD configuration may contribute to the formation of a more uniform and efficient conduction channel resulting in better transfer characteristics than BGBC OTFT.

Similarly, the graph provided in Figure 7(b) illustrates a comparative analysis output characteristics BGBC OTFT and DCBG OFET in CD configuration in terms of change in drain current (I_{DS}) with respect to V_{DS} . Here, x-axis represents V_{DS} , while the y-axis depicts the I_{DS} in microamperes (μA). As elucidated in Figure 7(b) across the entire range of V_{DS} the CD configuration consistently demonstrates higher I_{DS} values compared to the BGBC structure. Here also, the CD design exhibits a steeper slope in contrast to BGBC design, implying a higher field effect mobility and greater sensitivity towards V_{DS} in the linear region. In saturation region as the drain current becomes less dependent on the V_{DS} and is primarily determined by the V_{GS} , the CD architecture of DC BEBG exhibits higher drain currents and a steeper output characteristic, indicating improved charge carrier mobility, optimized field distribution, reduce contact resistance and development of a more uniform and efficient conduction channel compared to BGBC OTFT structure [34].

I_{ON}/I_{OFF} Ratio: It is the ratio of the current in the 'ON' state (I_{ON}) to the current in the 'OFF' state (I_{OFF}). It reflects on the capability of the transistor to switch between on state and state of operation very quickly. The higher I_{ON}/I_{OFF} ratio indicates that lower amount leakage current is produced in 'OFF' state by OTFT hence the reduction in unwanted power consumption is achieved while significantly increasing battery life of the portable electronic devices [30]. The single channel devices including BGBC, TGBC and BGTC OTFTs exhibiting ratios of 110.59, 96.19, and 115.83 respectively; while the DCBG OFET produces an enhanced I_{ON}/I_{OFF} ratio of

378.69, demonstrating its ability to provide a low 'OFF' state current while maintaining a significantly higher 'ON' state current.

Transconductance (g_m): Transconductance is the property of an OTFT that represents its ability to strengthen the input signal and propagate it to the output port with minimal delay [34].

$$\frac{dI_D}{dV_G} = \frac{\mu C_{ox} W}{L} (V_{GS} - V_T) \quad (10)$$

$$g_m = \frac{dI_D}{dV_G} \quad (11)$$

where, transconductance is denoted through g_m , drain current is I_{DS} , and gate voltage is V_{GS} [30]. As recorded in the Table 4 the DCBG OFET demonstrates superior transconductance of $4.59 \times 10^{-6} \mu S$ in comparison to the other single gated designs, providing significantly lower transconductance attributing to $1.16 \times 10^{-6} \mu S$ for BGBC, $1.30 \times 10^{-6} \mu S$ for TGBC and $1.29 \times 10^{-6} \mu S$ only for BGTC OTFT. This approximately 4 times increased transconductance in DCBG configuration is indicative of its enhanced capability to improve signal amplification and greater output level increment in multistage sequential and combinational circuits with numerous OTFTs as interconnected nodes.

Mobility at Saturation (μ_{sat}): Saturation mobility (μ_{sat}) is a crucial metric that quantifies the effectiveness of charge carrier movement within the organic semiconductor layer while the OTFT is operating in saturation regime. During this operational state, the channel is pinched off completely, and the drain current becomes nearly independent of the drain-source voltage and depends only on V_{GS} . μ_{sat} directly influences the maximum attainable drain current of OTFT and, consequently, its overall performance. A higher saturation mobility implies enhanced charge carrier mobility within the organic material, resulting in improved device speed and current conducting capabilities [31].

$$\mu_{sat} = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{|I_D|}}{\partial V_G} \right)^2 \quad (12)$$

Here W is channel width, L is length of channel, gate oxide capacitance per unit area is given by C_i , saturation drain current is I_D and V_G is gate-source voltage [30].

The DCBG device exhibited a superior saturation mobility of $0.416 \text{ cm}^2/\text{V}\cdot\text{s}$ compared to the $0.102 \text{ cm}^2/\text{V}\cdot\text{s}$, $0.107 \text{ cm}^2/\text{V}\cdot\text{s}$, and $0.104 \text{ cm}^2/\text{V}\cdot\text{s}$ measured for the BGBC, TGBC and BGTC OTFTs respectively. This substantial enhancement in charge carrier mobility within the saturation regime could be attributed to the central drain architecture and facilitates more efficient charge transport within the active layer of DCBG OFET.

Threshold Voltage (V_T): The threshold voltage (V_t) is a key parameter which indicates the start of transistor operation. It represents the minimum gate voltage

required to induce a conducting channel and initialize the flow of current [30], [31], [32], [33], [34]. A lower V_T facilitates the transistor operation at lower voltage levels, which is an advantageous for low power applications. V_T can be experimentally determined from the transfer characteristic curve using the following equation:

$$V_T = V_G - \frac{I_{DS}}{\frac{dI_{DS}}{dV_G}} \quad (13)$$

where, V_T is the threshold voltage, V_G represents gate voltage, drain current is I_{DS} , and dI_{DS}/dV_G is the slope of the drain current versus gate voltage curve [30]. All OTFT structures including BGBC, TGBC, BGTC and DCBG OFETs exhibited comparable threshold voltage values of -1.30 V, -1.34 V, -1.39 V and -1.25 V, respectively. This similarity suggests that both devices initiate conduction at lower gate voltage, implying comparable operational starting points but still the threshold voltage of DCBG is slightly lower than the other OTFT configurations implying rapid channel formation for lower voltage operations.

Sub-Threshold Slope (SS): The subthreshold slope (SS) serves as a critical metric for evaluating a transistor's sensitivity to gate voltage modulation within the subthreshold region, where the device operates in a weak inversion mode. It quantifies the rate at which drain current varies with changes in gate voltage. Mathematically expressed as the inverse of the logarithmic derivative of drain current with respect to gate voltage [30].

$$SS = \frac{1}{\frac{d(\log_{10} I_{DS})}{dV_{GS}}} \quad (14)$$

where SS represents the subthreshold slope, I_{DS} is the drain current, and V_{GS} is the gate-source voltage [30]. The SS provides valuable insights into the transistor's switching behaviour and operations below threshold voltage. Results show that the BGBC exhibited slightly higher SS (0.92 V/decade) compared to DCBG OFET (0.89 V/decade) making it slightly slower in terms of transitioning between the 'OFF' and 'ON' states with respect to dual channel device. While TGBC and BGTC OTFT structures exhibited comparable SS of 0.89 V/decade and 0.90 V/decade respectively implying equivalent switching speed comparable to DCBG OTFT.

The enhancement observed in the charge carrier mobility inside the active layer of DCBG OFET could be attributed to its unique architectural design. The dual channel configuration, incorporating novel central drain electrode, facilitates augmentation in the charge accumulation within the conduction channel region. The strengthening of charge density in the active region directly contributes to the substantial enhancement in output drain current. The results obtained in Table 4 explicitly support claim related to the superior performance of the DCBG OFET over the other single gate OTFT devices in terms of both carrier mobility

(μ_{sat}) and drain current (I_{DS}). The observed correlation between the charge carrier mobility and electric field distribution underscores the efficacy of the DC BEBG architecture in optimizing charge transport in the conduction channel and strengthening the drain current. These outcomes also provide valuable insights into the effect of electrode positioning and channel length modulation on the OTFT performance and explore new avenues for advancement in the field of organic transistor design. The results validate the theoretical predictions regarding the exceptional performance characteristics of DCBG OFET, including elevated drain current, transconductance, and charge carrier mobility making it more suitable for applications demanding higher drain current levels to support greater numbers of nodes (transistors) in an electronic circuit.

6 Conclusion

This investigation underscores the performance limitations of organic semiconductor based conventional OTFT architectures, primarily because of inferior carrier mobility and uneven electric field distribution. To address this, the double channel bottom gate organic field effect transistor (DCBG) with central drain architecture has been proposed in this study. Compared to the benchmark Bottom Gate Bottom Contact (BGBC) OTFT, the DCBG demonstrated a fourfold increase in drain current, viz. 8.05 μA for DC BEBG and 2.01 μA for BGBC architecture. It also outperformed other single-gated OTFT structures like TGBC ($2.16 \times 10^{-6} \mu A$) and BGTC OTFT ($2.12 \times 10^{-6} \mu A$). Moreover, the DCBG exhibited superior carrier mobility, with saturation and linear mobilities of 0.415 cm^2/Vs and 6.54 cm^2/Vs , respectively, compared to 0.103 cm^2/Vs and 1.67 cm^2/Vs for the BGBC OTFT. This translates to a remarkable 300% performance enhancement compared to other OTFT structures like TGBC (1.30×10^{-6}) and BGTC (1.29×10^{-6}) providing limited linear mobility. The substantial improvements in drain current and carrier mobility offered by the DCBG OFET significantly advance its capabilities compared to other organic transistors. Also, an approximate 300% improvement is also noticed in transconductance of DCBG OTFT ($4.59 \times 10^{-6} \mu S$) compared to BGBC ($1.16 \times 10^{-6} \mu S$), TGBC ($1.30 \times 10^{-6} \mu S$), BGTC ($1.29 \times 10^{-6} \mu S$) OTFTs. These findings emphasize that substantial performance enhancement is feasible in organic transistors with suitable improvement in the device structures. Continued research and development in this field are essential to fully realize the potential of organic electronics in advanced computing applications and electronic circuit optimizations.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

All authors have equal Contributions.

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Informed Consent Statement

Not applicable

Declaration of generative AI and AI-assisted technologies

Author(s) declared that no generative AI or AI-assisted technologies were used in the writing process of this manuscript.

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