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Iranian Journal of Electrical and Electronic Engineering

Journal Homepage: ijeee.iust.ac.ir

A Reduced Switch Seven Level Three phase UPQC for Voltage and Current Quality Enhancement in Distribution System

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Abstract: Power quality enhancement in modern distribution systems has become a critical challenge due to the proliferation of nonlinear loads and distributed generation. Unified Power Quality Conditioner (UPQC) systems offer a comprehensive solution by integrating series and shunt compensators to mitigate voltage and current disturbances. However, conventional UPQC topologies often involve a high number of switches, resulting in increased complexity, switching losses, and cost. This paper proposes a reduced switch seven-level three-phase UPQC configuration aimed at improving voltage regulation and current harmonic suppression while minimizing component count and system complexity. The proposed topology employs a control strategy such as Instantaneous Reactive power Theory (IRP) and Synchronous Reference Frame (SRF) theory to enhance dynamic performance. Simulation studies conducted in MATLAB/Simulink demonstrate significant improvements in Total Harmonic Distortion (THD), voltage sag/swell mitigation, and compliance with IEEE-519 standards. The findings validate the technical feasibility and effectiveness of the reduced-switch design in achieving superior power quality in distribution systems.

Keywords: Cascaded H-bridge; Current quality; Power distribution system; Power quality; Seven level five switch converter; UPQC; Voltage quality.

1 Introduction

POWER quality has become a critical concern in modern distribution systems due to the rapid increasing presence of nonlinear loads, integration of renewable energy sources, and sensitive electronic equipment. These factors lead to various voltage and current quality issues such as voltage swell/sag, harmonic distortion, and unbalanced loads, which significantly affect the performance and lifespan of electrical devices [1]. The Unified Power Quality Conditioner (UPQC) has been established as an effective solution for mitigating voltage and current-related power quality disturbances in distribution systems. It integrates series and shunt active power filters to simultaneously compensate for supply voltage disturbances and load current harmonics [2]. Traditional UPQC systems, however, often suffer from drawbacks such as high switching losses, increased cost, and complex control strategies due to the substantial number of power electronic switches required [3].

Despite promising results, the current research remains confined to simulation studies, with limited experimental validation and inconsistent quantitative reporting of power quality metrics. Therefore, there is a pressing need for robust, experimentally validated UPQC designs that achieve both high performance and reduced hardware complexity. In this context, the proposed work focuses on the development of a reduced switch, seven-

Iranian Journal of Electrical & Electronic Engineering, 2027.
Paper first received 17 June 2025 and accepted 31 July 2026.
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level three-phase UPQC aimed at enhancing voltage and current quality in distribution systems. The objective is to leverage multilevel inverter benefits while minimizing switch count and employing intelligent control techniques to ensure compliance with power quality standards. Power quality has become a pressing issue in modern distribution systems due to the increasing use of power electronic equipment, unbalanced loads, and renewable energy sources [1]– [3]. Voltage swells, sags, and harmonics can affect the performance and longevity of sensitive electrical equipment [4], [5]. Maintaining both voltage and current quality is essential for ensuring reliable and uninterrupted power supply.

Among the solutions available, Flexible AC Transmission System (FACTS) devices such as Dynamic Voltage Restorer (DVR), Distribution STATCOM (DSTATCOM), and UPQC [6]– [10]. The UPQC provides a comprehensive approach by integrating both series and shunt converters to simultaneously mitigate voltage and current disturbances [11]– [13]. Its dual compensation capability addresses sag/swell events and suppresses current harmonics arising from nonlinear loads [14], [15]. Multilevel inverter-based UPQCs offer enhanced waveform quality, reduced filter size, and lower harmonic distortion compared to conventional two-level systems [16], [17]. Cascaded H-Bridge (CHB) and Neutral Point Clamped (NPC) topologies are prominent choices for multilevel implementation due to their modularity and effective voltage level generation [18]. However, multilevel UPQCs often require considerable number of power switches, which increase system cost and complexity [19]. To overcome this limitation, researchers have proposed reduced switch topologies that maintain performance while minimizing hardware requirements. Jeevanantham and Srinath [20] demonstrated a reduced-switch five-level multilevel inverter UPQC using ANN control with significant THD improvement. Similarly, a ten-switch topology presented by Rauf et al. [21]-[22] achieved a reduction in source current THD from 28% to 1.8%, further optimized a nine-switch UPQC, maintaining THD below 5% per IEEE-519 standards.

Intelligent control techniques—such as Synchronous Reference Frame (SRF), P-Q theory, fuzzy logic, and Artificial Neural Networks (ANN)—have shown notable improvements in performance, control precision, and response time [23]– [26]. These methods contribute to the system's ability to adapt dynamically under varying load conditions and supply disturbances. A recent study by Veera Nagi Reddy et al. [27] employed a five-level CHB UPQC with SRF-based series control and P-Q theory-based shunt control. The system effectively compensated for voltage sags and swells while maintaining source current THD within 3%. Although multilevel UPQCs improve performance, their practical deployment is limited by the complexity and cost associated with higher switch counts. Therefore, this work proposes a reduced-switch seven-level three-phase UPQC that retains the advantages of multilevel configurations while minimizing hardware requirements. The topology incorporates intelligent control strategies and validates through detailed simulations in MATLAB/Simulink. The goal is to provide a cost-effective, high-performance solution to power quality challenges in distribution systems.

Reduced-switch multilevel converter (MLC)–based UPQC structures have gained considerable attention in recent years due to their potential to lower system complexity, switching losses, and cost while maintaining acceptable power quality performance. Varampati et al. [28] presented a reduced-switch seven-level converter–based UPQC employing a hybrid fuzzy–feedforward neural network control algorithm. Their work demonstrated effective mitigation of voltage and current harmonics under nonlinear load conditions.

Several studies have focused on the mitigation of voltage sags and harmonics using UPQC and other custom power devices. Shakeri et al. [29] provided a comprehensive technical and economic analysis of various voltage sag mitigation methods, highlighting that converter topology and semiconductor device count significantly influence both investment cost and operational efficiency. Their findings emphasize the importance of reducing power electronic components to improve economic feasibility, particularly in distribution-level applications.

Srivastav et al. [30] investigated the mitigation of voltage and current harmonics using a conventional UPQC configuration and validated the effectiveness of coordinated series–shunt compensation. Although satisfactory harmonic reduction was achieved, the employed topology utilized a higher number of switching devices, resulting in increased hardware complexity and cost. This limitation motivates further research into reduced-switch UPQC configurations without compromising compensation performance.

In addition to converter-based solutions, Khajouei et al. [31] explored voltage sag mitigation through optimal placement of renewable energy resources within the power system. While this approach enhances system-level voltage stability and efficiency, it requires network-level planning and integration of distributed generation, which may not be feasible or economical in all distribution systems. In contrast, UPQC-based solutions offer localized and flexible compensation capabilities.

Therefore, there remains a clear research gap for a structurally simplified, reduced-switch seven-level UPQC topology that achieves effective voltage and

current quality enhancement using conventional control while offering tangible economic benefits. The proposed work addresses this gap by minimizing the number of power semiconductor devices and introducing a relative cost index–based evaluation to demonstrate its economic superiority.

The development of multilevel inverter (MLI) technology has significantly enhanced the performance of power electronic converters used in medium- and high-power applications. Rodriguez et al. [32] presented one of the earliest comprehensive surveys on multilevel inverter topologies, control strategies, and industrial applications. Their work analyzed the diode-clamped, flying-capacitor, and cascaded H-bridge inverter structures, highlighting their ability to generate high-quality output voltages with reduced harmonic distortion and lower voltage stress across semiconductor devices.

Further advancing the field, Franquelo et al. [33] described the growing industrial adoption of multilevel converter technology and referred to this period as the "age of multilevel converters." The authors discussed the technological progress that enabled multilevel converters to become practical solutions for renewable energy systems, motor drives, power quality improvement devices, and flexible AC transmission systems (FACTS). The review highlighted the advantages of multilevel converters, including improved output waveform quality, reduced filter requirements, enhanced efficiency, and scalability to higher voltage levels. Moreover, the study identified challenges such as increased component count, complex control algorithms, capacitor voltage balancing issues, and higher implementation costs, which continue to motivate research toward reduced-switch and cost-effective multilevel converter configurations.

2 Cascaded H-bridge Seven-level UPQC

A Cascaded H-Bridge (CHB) inverter structure is typically used in multilevel inverter-based power quality conditioners due to its modularity and ease of control. For an n-level CHB multilevel inverter (MLI), the number of H-bridge cells required per phase is $(n-1)/2$, with each cell comprising four switches. Thus, a conventional seven-level CHB-MLI necessitates twelve switches per phase, leading to increased circuit complexity, switching losses, size, and cost.

Figure 1 illustrates the schematic layout of the proposed seven-level unified power quality conditioner (UPQC) using a reduced-switch five-switch topology for both series and shunt voltage source converters (VSCs). UPQC comprises a series compensator to mitigate voltage disturbances and a shunt compensator to suppress current harmonics and maintain reactive power balance.

Figure 2 shows the conventional seven-level CHB-MLI, which employs twelve switches per phase. Each voltage level is obtained by controlling the conduction of different switches across multiple H-bridge cells. The corresponding switching table is presented in Table 1, indicating the required ON/OFF states of switches S1 to S12 for generating different output voltage levels ranging from $+VDC$ to $-VDC$.

To overcome the drawbacks of conventional topology, a novel five-switch seven-level MLI topology is proposed and illustrated in Figure 3. This design requires only five switches and four isolated DC sources to generate seven distinct output levels. The primary advantage of this topology lies in its minimal switch count, lower switching losses, reduced size, and simplified gate driver requirements, all of which contribute to the enhanced reliability and efficiency of the UPQC system. The switching modes, for the five-switch seven-level MLI, are provided in Table 2, where each row denotes the switching states (S1 to S5) necessary to produce the corresponding output voltage. The topology can generate seven levels: $\pm VDC$, $\pm 2VDC/3$, $\pm VDC/3$ and 0. In each conduction mode, only two switches are active, contributing to low conduction and switching losses.

The operational behavior of the proposed MLI during each conduction mode is shown in Figure 4. There are six conduction modes excluding the zero mode, which occurs when all switches are OFF. These conduction paths ensure balanced voltage generation across all levels and maintain the integrity of the output waveform. The use of minimal switches simplifies the modulation strategy and enhances the dynamic response of the converter. This proposed topology, integrated into both series and shunt converters of the UPQC, offers an efficient and compact solution for current and voltage quality enhancement in distribution systems.

A key structural advantage of the proposed topology over neutral point clamped (NPC) and flying capacitor (FC) multilevel converters is the elimination of active capacitor voltage balancing. In NPC converters, floating DC-link capacitors require continuous monitoring and active charge redistribution to maintain equal voltage sharing; failure to do so results in output waveform distortion and increased device stress. Similarly, FC converters require pre-charging circuits and balancing algorithms that add control complexity. In the proposed topology, each voltage level is generated by an isolated DC source, which maintains its voltage independently. Consequently, no balancing algorithm, auxiliary circuitry, or additional sensing is required, simplifying the control architecture and improving reliability. This advantage is retained regardless of load conditions or switching state, as confirmed by the simulation results in Section 4.

3 Control Scheme for UPQC

A. Control scheme for series compensator

Position The conventional PI control strategy for the series compensator, as illustrated in Figure 5, is designed to regulate voltage disturbances using a structured control architecture. This setup includes a Phase-Locked Loop (PLL), Clarke and Park transformation block, inverse transformation block, and a PWM signal generator tailored for a seven-level five-switch multilevel inverter. The PLL synchronizes with the source voltage to extract the phase angle, which is then used by the Clarke-Park transformation block to convert the three-phase voltage components into the rotating d-q reference frame as defined by Equation (1). The transformed voltage is compared with the reference d-q voltages, and the resulting error signals, obtained using Equations (2) and (3), are fed into a Proportional-Integral (PI) controller. The controller processes these errors and generates the d-q axis reference voltage signals as per Equation (4). These signals are then transformed back into three-phase a-b-c coordinates using the inverse Clarke-Park transformation (Equation 6.8).

The resulting reference voltage signals VLabc_ref are used to generate the final LSCPWM pulses required to operate the seven-level five-switch MLI-based series compensator.

$$\begin{bmatrix} V_0 \\ V_d \\ V_q \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \\ \sin(wt) & \sin(wt - 2\pi/3) & \sin(wt + 2\pi/3) \\ \cos(wt) & \cos(wt - 2\pi/3) & \cos(wt + 2\pi/3) \end{bmatrix} \begin{bmatrix} V_{Sa} \\ V_{Sb} \\ V_{Sc} \end{bmatrix} \quad (1)$$

$$V_d = \overline{V}_d - \tilde{V}_d(ref) \quad (2)$$

$$V_q = \overline{V}_q - \tilde{V}_q(ref) \quad (3)$$

$$V_d = \overline{V}_d; V_q = 0; V_0 = 0 \quad (4)$$

The dq-frame parameters are then converted to a-b-c coordinates using (5) and are taken as reference voltage (VLabc_ref).

$$\begin{bmatrix} V_{La_ref} \\ V_{Lb_ref} \\ V_{Lc_ref} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1/\sqrt{2} & sin(wt) & cos(wt) \\ 1/\sqrt{2} & sin(wt - 2\pi/3) & cos(wt - 2\pi/3) \\ 1/\sqrt{2} & sin(wt + 2\pi/3) & cos(wt + 2\pi/3) \end{bmatrix} \begin{bmatrix} V_{S0} \\ V_{Sd} \\ V_{Sq} \end{bmatrix} \quad (5)$$

B. Control scheme for shunt compensator

Figure 6 depicts the PI-based control scheme for the shunt compensator, which is primarily responsible for regulating the DC-link voltage. This method involves the use of a PI controller that requires proper tuning of proportional and integral gains. The control process begins with the measurement of line voltages and currents to compute the instantaneous active (P) and reactive (Q) powers using Equation (6). These power quantities are then used to derive the reference compensation currents in the α-β frame. The inverse Clarke transformation, as shown in Equation (7), converts these currents into three-phase a-b-c compensating current references. To determine the source of current references, the compensating currents are subtracted from the corresponding load currents using Equations (8), (9), and (10). For the seven-level five-switch inverter topology, only four carrier signals are needed to perform the multilevel PWM switching due to the optimized switch configuration. The final LSCPWM reference signals are obtained by comparing the actual source currents with the reference currents, as described in Equation (11). This method ensures that the shunt compensator effectively injects the appropriate current to maintain power quality and stable voltage levels in the distribution system

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} i^*_{ca} \\ i^*_{cb} \\ i^*_{cc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i^*_0 \\ i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} \quad (7)$$

$$I^*_{SA} = I_{LA} - I^*_{CA} \quad (8)$$

$$I^*_{SB} = I_{LB} - I^*_{CB} \quad (9)$$

$$I^*_{SC} = I_{LC} - I^*_{CC} \quad (10)$$

$$\text{PWM Ref}_A = I^*_{SA} - I_{SA};\ \text{PWM Ref}_B = I^*_{SB} - I_{SB};$$
$$\text{PWM Ref}_C = I^*_{SC} - I_{SC} \quad (11)$$

C. DC Source Modeling and Practical Considerations

In the proposed seven-level five-switch MLC-based UPQC, isolated DC sources are employed to generate the required stepped voltage levels. In the simulation model, each phase utilizes independent DC sources configured to produce symmetrical seven-level output voltage. The DC voltage magnitudes are selected based on the required peak line voltage of the distribution system to ensure proper series compensation and harmonic mitigation.

The DC source magnitudes are selected such that the output phase voltage levels follow a symmetrical structure of $\{-V_{dc}, -2V_{dc}/3, -V_{dc}/3, 0, +V_{dc}/3, +2V_{dc}/3, +V_{dc}\}$ where V_{dc}represents the base DC source voltage. The value of $V_{dc}$is determined according to the required

compensation voltage rating of the UPQC. This ensures balanced voltage steps and equal voltage stress across semiconductor devices. Since the proposed topology employs isolated DC sources rather than capacitor-based floating DC links, active voltage balancing control is not required. Each DC source is independently maintained at a constant voltage using ideal DC supply blocks in simulation. This eliminates capacitor voltage imbalance issues commonly observed in neutral point clamped (NPC) and flying capacitor converters. In the simulation environment, the isolated DC sources are modeled as ideal voltage sources without internal resistance or ripple to evaluate the steady-state performance of the proposed UPQC topology under controlled conditions. This assumption enables clear assessment of voltage level generation and compensation capability without additional non-ideal effects. However, in practical implementation, DC voltage ripples may arise due to switching actions, dynamic load variations, and converter non-idealities.

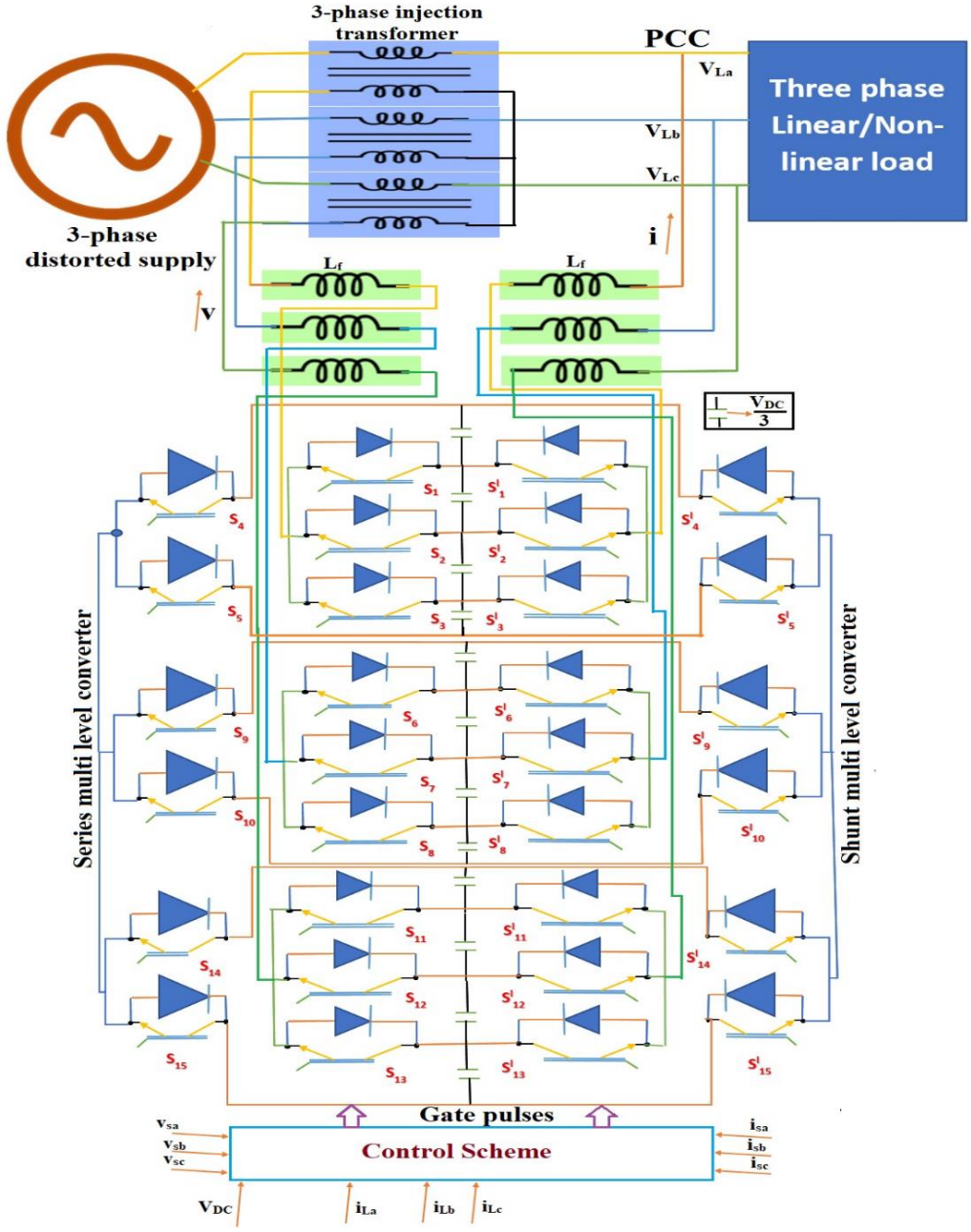


Fig 1. Schematic representation of seven-level five switch UPQC.

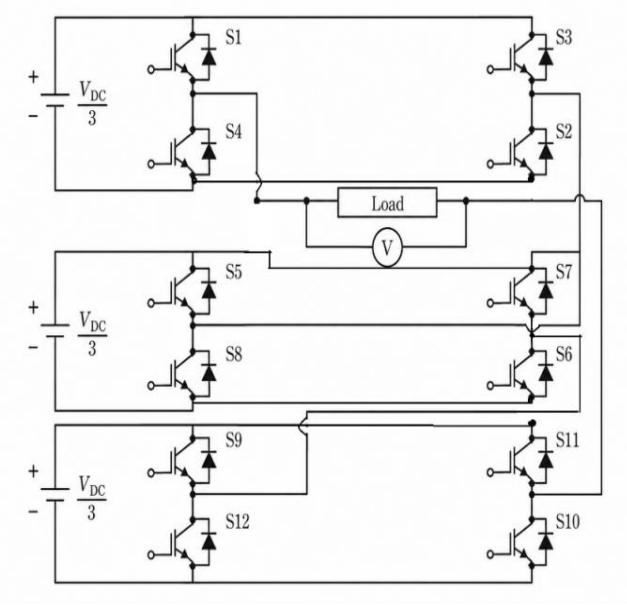


Fig 2. Conventional seven-level twelve switches single phase CHB-MLC.

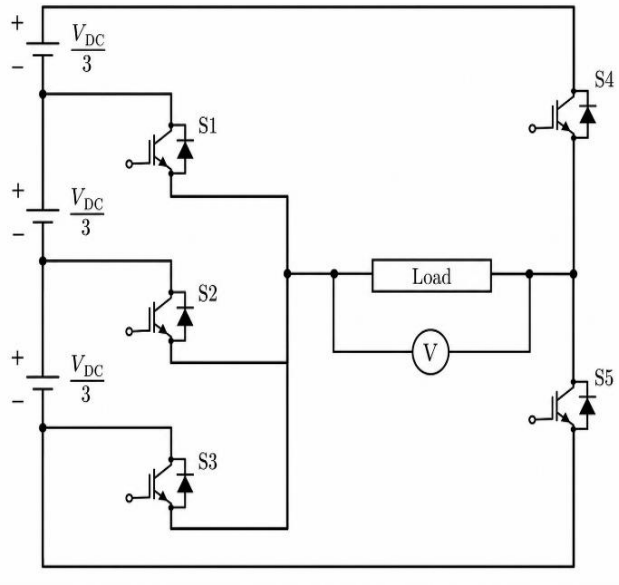


Fig 3. Proposed seven-level five switches single phase MLC.

Such ripple effects can be effectively minimized through appropriate DC-link capacitor sizing, the use of regulated isolated DC–DC converters, and the implementation of closed-loop voltage regulation schemes. Moreover, the reduced number of conducting switches per voltage level in the proposed topology inherently lowers switching stress, which further limits ripple propagation and enhances overall voltage stability. From a practical standpoint, the isolated DC sources required in the proposed topology can be implemented using multi-secondary isolation transformers followed by rectifier units, regulated isolated DC–DC converters, or independently controlled renewable energy sources. These approaches are commonly employed in multilevel power conversion systems to ensure galvanic isolation and stable DC voltage generation. Compared to capacitor-clamped multilevel structures, the proposed configuration simplifies voltage balancing control by eliminating floating capacitor voltage regulation, although it necessitates the use of isolated supplies. In medium- and low-voltage distribution applications, such isolated DC sources are technically feasible and are widely adopted in cascaded H-bridge–based multilevel converters, thereby supporting the practical realizability of the proposed UPQC structure.

D. Control Parameters and Design Details

The proposed seven-level reduced-switch UPQC employs synchronous reference frame (dq) control for coordinated operation of the series and shunt converters. Conventional PI regulators are implemented for DC-link voltage regulation, shunt current control, and series voltage control. The controller gains are selected to ensure fast transient response, minimal steady-state error, and stable operation under nonlinear load and voltage sag conditions. The DC-link voltage controller is tuned with proportional gain $K_p = 0.6$ and integral gain $K_i = 85$, providing a relatively lower bandwidth to ensure smooth energy balancing between the converters. The shunt current controller, responsible for harmonic current compensation, is designed with $K_p = 1.8$ and $K_i = 220$ to achieve fast reference tracking and improved harmonic suppression. Similarly, the series voltage controller is tuned with $K_p = 1.2$ and $K_i = 150$ to ensure accurate voltage injection during sag and distortion events while maintaining system stability.

Grid synchronization is achieved using a synchronous reference frame phase-locked loop (SRF-PLL). The PLL bandwidth is selected as 20 Hz, providing an appropriate compromise between fast dynamic tracking capability and harmonic rejection under distorted grid conditions. This bandwidth ensures accurate phase detection while minimizing sensitivity to high-frequency noise.

For switching pulse generation, a level-shifted sinusoidal pulse-width modulation (SPWM) technique is employed. The switching frequency is set to 3050 Hz, which offers a suitable balance between harmonic performance and switching losses. The reference signals derived from the dq control algorithm are compared with high-frequency triangular carrier signals to generate gating pulses for the reduced-switch seven-level multilevel converter.

The system operates with a three-phase 415 V (rms), 50 Hz supply. The line impedance is modeled with a resistance of 0.10 Ω and an inductance of 0.90 mH, while the nonlinear load is represented by a resistance of 30 Ω

and an inductance of 6 mH. A combined DC-link capacitor of 3000 µF is used to maintain a regulated DC voltage of 700 V, ensuring sufficient energy buffering during transient conditions. To suppress switching harmonics and limit ripple, a shunt interfacing filter consisting of a 10 mH inductor (with 0.0001 Ω resistance) is employed, while the series converter utilizes a 3 mH inductor and a 10 µF capacitor to smooth the injected compensating voltage. These parameters are selected to ensure stable operation, effective harmonic mitigation, and reliable performance of the proposed UPQC under distorted supply and nonlinear loading conditions.

Table 1. Switching modes of seven-level twelve switches single phase MLC.

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Voltage
1	1	0	0	1	1	0	0	1	1	0	0	VDC
1	1	0	0	1	1	0	0	0	1	0	1	$\frac{2V_{DC}}{3}$
1	1	0	0	0	1	0	1	0	1	0	1	$\frac{V_{DC}}{3}$
0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	0	1	0	1	0	1	0	1	$-\frac{V_{DC}}{3}$
0	0	1	1	0	0	1	1	0	1	0	1	$-\frac{2V_{DC}}{3}$
0	0	1	1	0	0	1	1	0	0	1	1	-VDC

Table 2. Switching modes of seven-level five switches single phase MLC.

S1	S2	S3	S4	S5	Voltage
0	0	1	1	0	VDC
0	1	0	1	0	$\frac{2V_{DC}}{3}$
1	0	0	1	0	$\frac{V_{DC}}{3}$
0	0	0	0	0	0
0	0	1	0	1	$-\frac{V_{DC}}{3}$
0	1	0	0	1	$-\frac{2V_{DC}}{3}$
1	0	0	0	1	-VDC

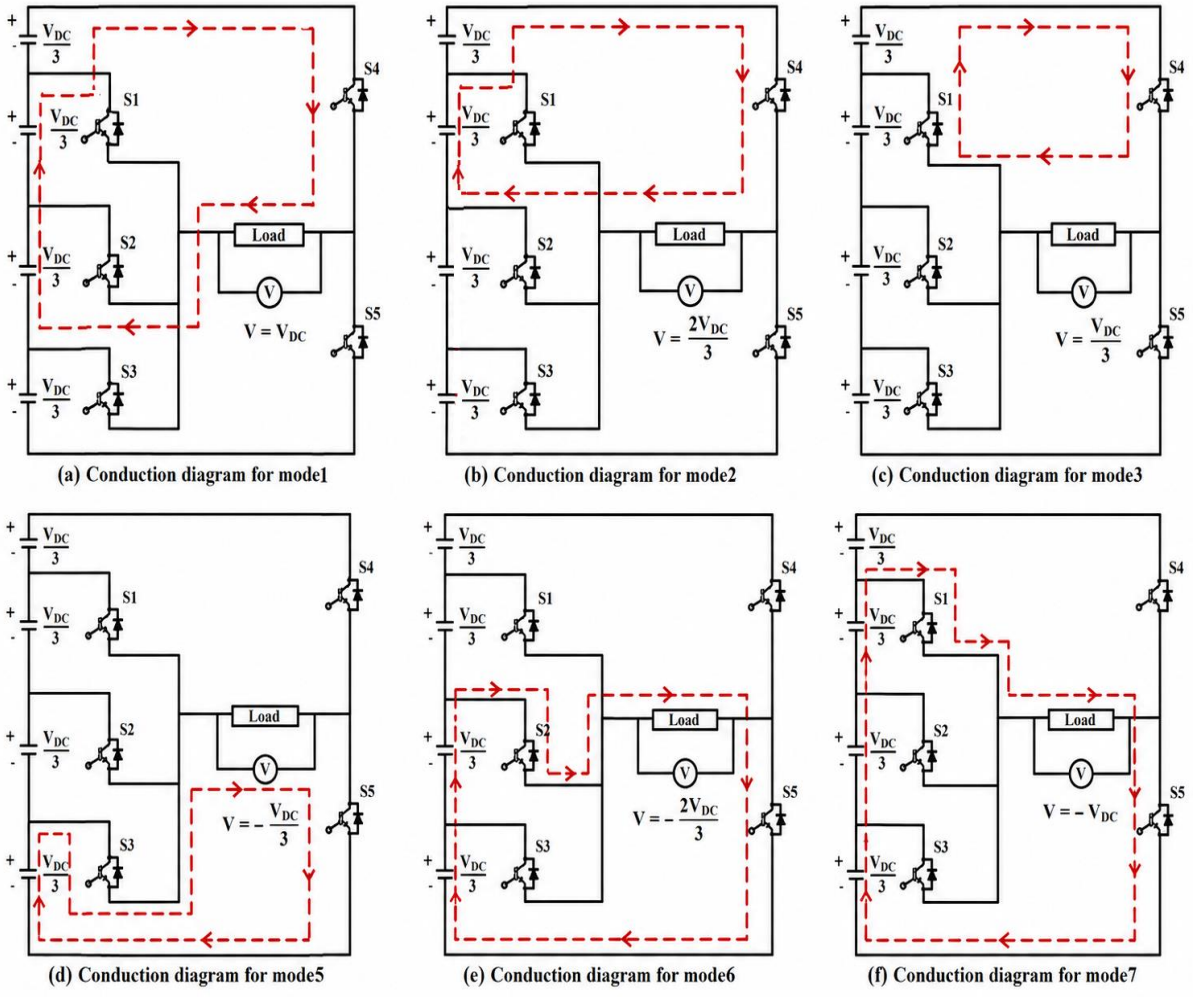


Fig 4. Conduction modes of seven-level five switch single phase MLC.

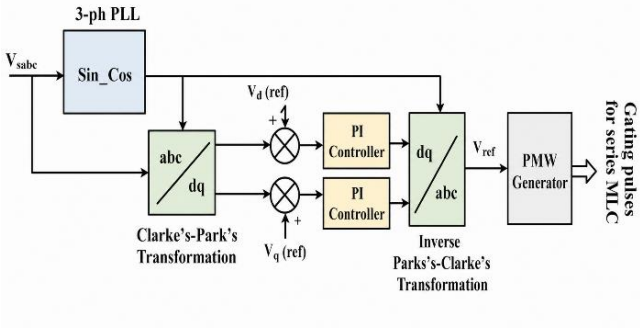


Fig 5. Control scheme for series compensator of UPQC.

4 Results and Discussion

A. V*oltage and Current Compensation Results*

The simulation and analysis are conducted using the system parameters listed in Table 3. A three-phase source of 415 V (rms) at 50 Hz is connected to a distribution feeder with a moderate impedance. The shunt compensator includes a line-interfacing filter, and the series compensator incorporates an L-C filter to ensure smooth voltage injection. A common DC link of 700 V is maintained using a 3000 µF capacitor. Figure 7 illustrates the dynamic response of the proposed seven-level five-switch UPQC under conditions of voltage sag and swell, as well as harmonic distortion. Figure 7 (a) Shows the source voltage, which is distorted due to the presence of 5th and 7th harmonic components, indicating poor power quality. Figure 7 (b) Depicts the per-phase series compensating voltage injected by the UPQC, which dynamically adjusts to counteract both sag and swell disturbances. Figure 7 (c) Represents the load voltage waveform, which remains balanced and sinusoidal due to effective compensation, validating the voltage regulation ability of the UPQC. Figure 7 (d) Displays the load currents, which are also maintained in sinusoidal form, demonstrating improved power delivery to the load. Figure 7 (e) Shows the supply currents after compensation, where the harmonic content has been significantly reduced, indicating successful current

shaping. Figure 7 (f) Highlights the supply currents before compensation, showing severe distortion due to the non-linear nature of the load and source harmonics.

B. D*C-Link Dynamics and Stability*

One important aspect of UPQC operation is maintaining a constant DC-link capacitor voltage. In this work, DC-link voltage regulation and capacitor voltage balancing are achieved using a PI controller, as depicted in Figure 14. During voltage sag conditions, the series converter draws active power from the DC-link capacitor to compensate for the load voltage, resulting in a temporary voltage drop across the capacitor. The PI controller responds rapidly and regulates the DC-link voltage by commanding the shunt converter to draw the required active power from the source, thereby restoring the capacitor voltage to its reference value. Similarly, during voltage swell conditions, excess energy is absorbed and regulated to maintain voltage balance. The steady-state voltage ripples around the reference are minimal, indicating proper capacitor sizing and effective controller tuning. Furthermore, the absence of sustained oscillations and the fast recovery of the DC-link voltage demonstrate stable power exchange and closed-loop system stability.

C. H*armonic Analysis and IEEE-519 Comparison*

Position Figure 8 presents the Total Harmonic Distortion (%THD) of the source voltage before compensation. The high %THD value reflects the presence of low-order harmonics (notably 5th and 7th), which are typically introduced by non-linear loads and grid disturbances. This level of distortion can severely affect sensitive loads if not properly addressed. Figure 9 provides a comparison of the load voltage harmonic profile. Figure 9 (a) Prior to UPQC operation, the load voltage exhibits a high THD value, indicating significant distortion transferred from the source.

Figure 9 (b) After applying the PI controller in the UPQC, the THD is dramatically reduced, and the waveform becomes sinusoidal. This highlights the controller's role in regulating the output and ensuring voltage quality at the load terminals. Figure 10 shows the harmonic content in the current drawn by the non-linear load. The spectrum reveals prominent low-order harmonic peaks, which are responsible for distortion in both the source and load voltages. This analysis justifies the need for a shunt compensator in the UPQC to manage current harmonics effectively. Figure 11 compares the source current spectrum. Figure 11 (a) Before UPQC compensation, the current is highly distorted with %THD exceeding IEEE-519 limits. Figure 11 (b) After compensation, the source current becomes sinusoidal with minimal harmonic content, affirming the UPQC's effectiveness in current harmonic mitigation. Figure 12 displays the single-phase output voltage waveform generated by the proposed five-switch multilevel converter. The waveform clearly exhibits seven distinct voltage levels, validating the converter's ability to generate high-resolution stepped voltages with reduced switch count. Figure 13 shows the three-phase output of the proposed converter. All three phases exhibit symmetric and balanced seven-level voltage waveforms. This confirms that the topology is well-suited for balanced three-phase applications, with proper voltage regulation and reduced harmonic content.

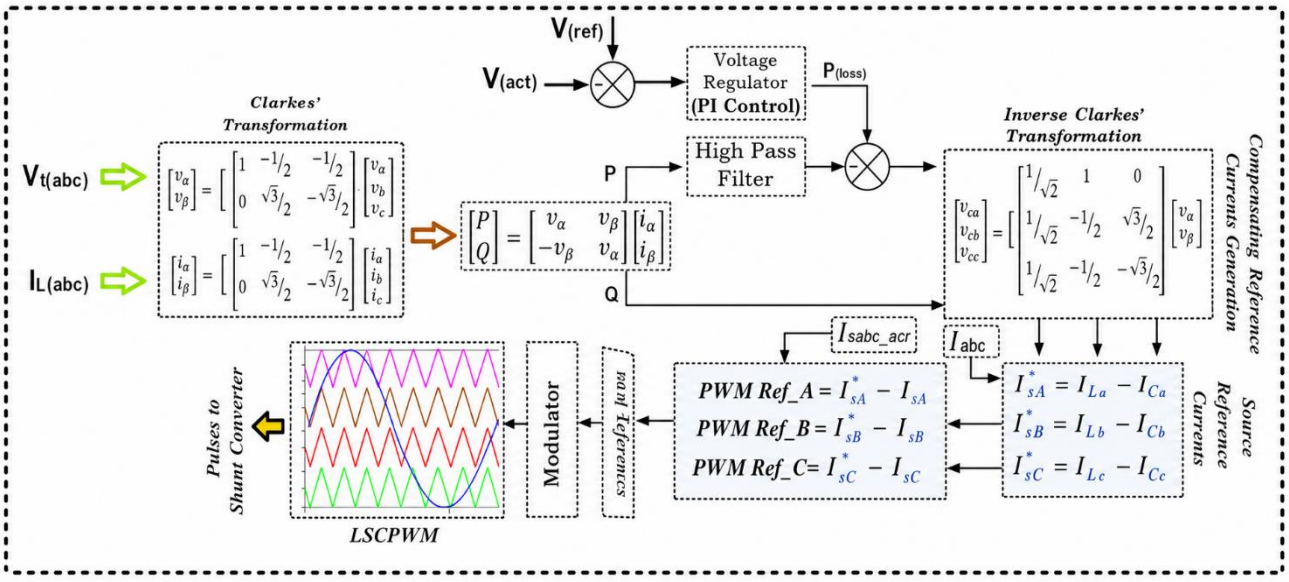


Fig 6. Control scheme for shunt compensator of UPQC.

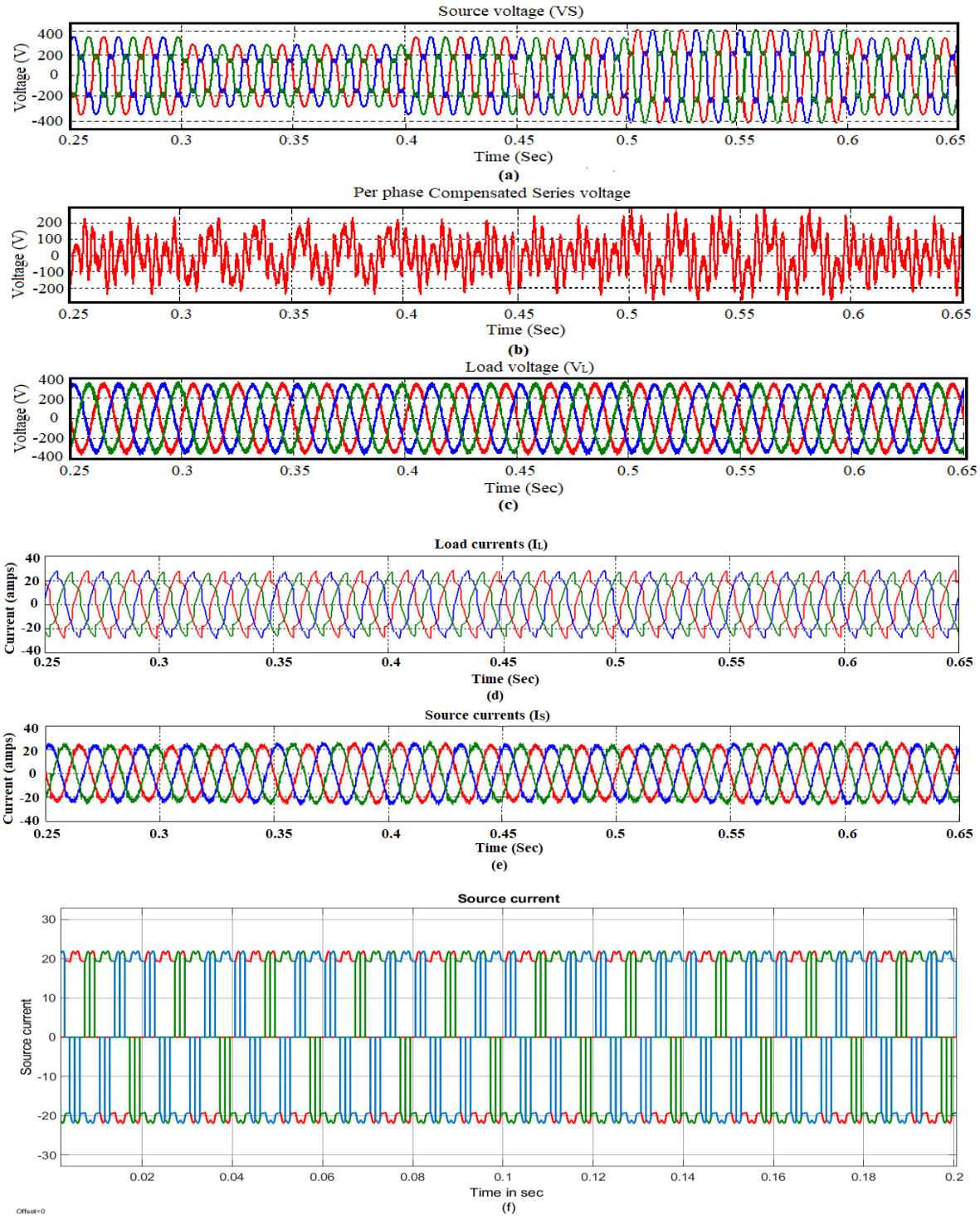


Fig 7. Simulation results of the seven-level five-switch UPQC under voltage sag and swell compensation:(a) Source voltages distorted with 5th and 7th harmonics, (b) Per-phase series compensating voltages, (c) Three-phase load voltages, (d) Three-phase load currents, (e) Three-phase supply currents after compensation, (f) Three-phase supply currents before compensation.

Table 4 provides a detailed comparison of key electrical parameters before and after compensation using the proposed seven-level MLC-UPQC under a polluted power supply with 5th and 7th harmonics and a non-linear load with 0.7 power factor. The source voltage (VS) remains unchanged in fundamental magnitude, but its waveform quality improves. The load voltage (VL) maintains the same RMS value but shows a drastic

reduction in THD from 29.15% to 3.60%, proving effective series voltage compensation. The source current (IS) shows both a reduction in amplitude and a dramatic improvement in harmonic distortion, reducing THD from 65.07% to 2.11%. This table underscores the significant improvements achieved in power quality, validating the superiority of the proposed five-switch topology in reducing losses and maintaining high power quality.

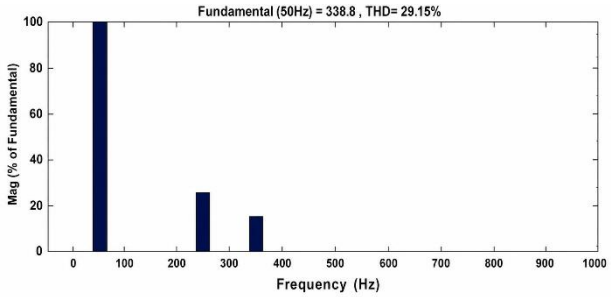
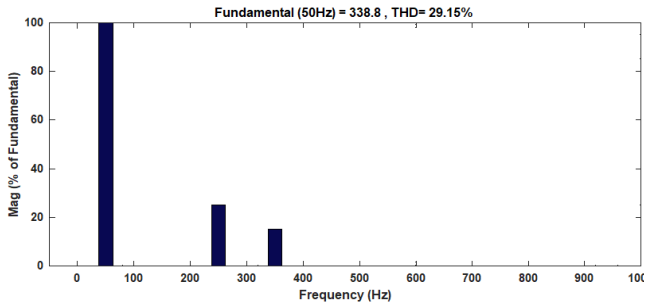
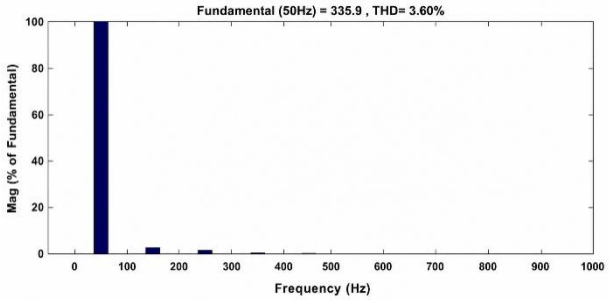


Fig 8. %THD spectrum of Source voltage.



(a)



(b)

Fig 9. %THD spectrum of Load voltage of seven level UPQC (a) before compensation (b) after compensation.

To evaluate the harmonic mitigation capability of the proposed seven-level reduced-switch UPQC, detailed harmonic spectrum analysis was performed for the dominant lower-order harmonics (5th, 7th, 11th, and 13th) under nonlinear load conditions with a polluted supply. The harmonic magnitudes were extracted from FFT analysis of the source current and load voltage before and after compensation. The harmonic spectrum analysis of source current and load voltage demonstrates the effectiveness of the proposed seven-level UPQC in mitigating lower-order harmonics. As shown in Tables 5 and 6, the 5th, 7th, 11th, and 13th harmonics are significantly reduced after compensation, with all individual harmonic magnitudes and total harmonic distortion (THD) meeting the IEEE-519 limits. For the source current, THD is reduced from 65.07% to 2.11%, while load voltage THD decreases from 29.15% to 3.60%, confirming compliance with IEEE-519 standards and effective power quality enhancement.

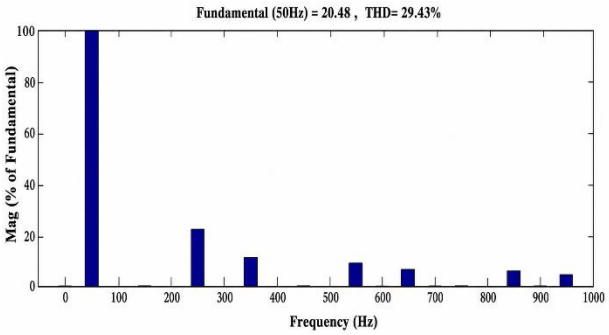
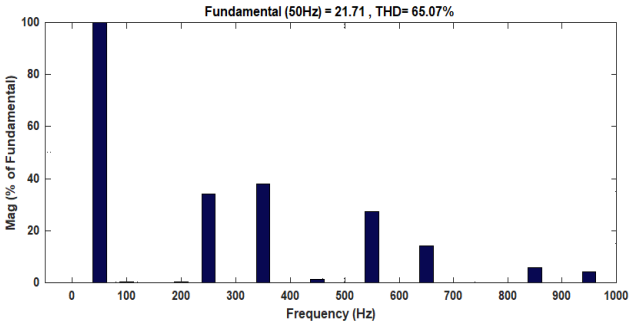
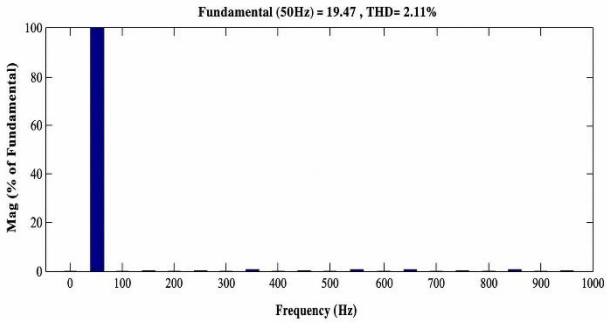


Fig 10. %THD spectrum of non-linear load current.



(a)



(b)

Fig 11. %THD spectrum of source current of seven level UPQC (a) before compensation (b) after compensation.

It is acknowledged from Table 8 that the proposed topology requires four isolated DC sources per phase, which represents an increase compared to asymmetric

CHB configurations that achieve 7 levels using only two sources with a 1:2 voltage ratio. However, in asymmetric CHB structures, the higher source voltage ratio causes the peak voltage stress on the higher-voltage H-bridge switches to reach 2VDC, whereas in the proposed topology, all five switches sustain a maximum voltage stress of VDC, resulting in uniform device ratings and simplified thermal management.

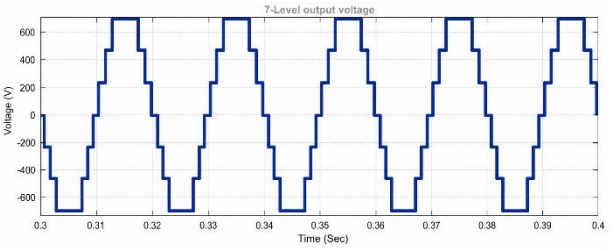


Fig 12. Single phase seven level output voltage.

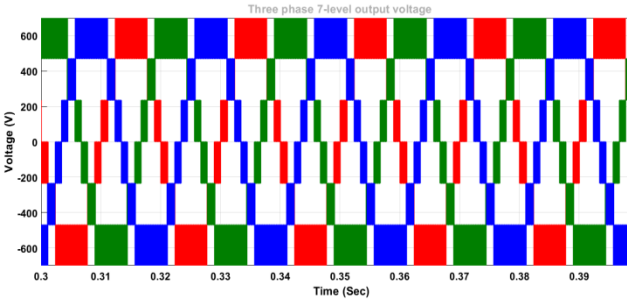


Fig 13. Three phase seven level output voltage.

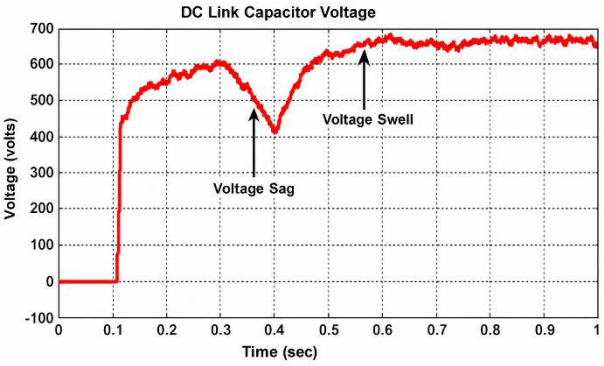


Fig 14. Capacitor voltage with seven-level five-switch UPQC.

Furthermore, the reduced switch count (5 vs 8 per phase for asymmetric CHB) lowers gate driver complexity and conduction losses. The choice of four equal-rated isolated sources is therefore a deliberate design decision prioritising switch count minimisation and uniform voltage stress over source count reduction. Suitable isolated DC supply implementations include multi-secondary isolation transformers with rectifiers or regulated DC–DC converters, both of which are standard practice in cascaded multilevel converter systems [32]-[33].

Table 3. System Parameters.

S. No	Specifications	Values
1	Supply Voltage	Vs.abc-415V (rms), Frequency-50 Hz
2	Line Impedance	R = 0.10 Ω, L = 0.90 mH
3	Non-Linear Load Impedance	R = 30 Ω, L = 6 mH
4	Combined DC Link Capacitor	3000μF
5	Line Interfacing Filter (Shunt-MLC)	Resistance -0.0001 Ω; Inductance -10mH
6	Shunt Interfacing Filter	R = 0.0001 Ω, L = 10 mH
7	Series Interfacing Filter	L = 3 mH, C = 10 μF
8	DC-Link Voltage	700 V
9	Switching Frequency	Fc-3050Hz

D. E*fficiency, Voltage Stress, and Switching Loss Analysis*

Voltage stress: In the proposed five-switch topology, each switch sustains a maximum forward voltage equal to VDC (the base DC source voltage), since only two switches conduct per level and the sources are independently isolated. This contrasts with asymmetric CHB converters where upper H-bridge switches sustain up to 2VDC. For a 700 V DC link, each switch in the proposed design is rated at 700 V, whereas the equivalent asymmetric CHB device must be rated at 1400 V.

Switching loss analysis: Per-switch switching loss is estimated using: Psw = fsw × (Eon + Eoff) × (VCE/Vref) × (IC/Iref), where fsw = 3050 Hz, and Eon, Eoff are obtained from IGBT datasheet energy values at reference conditions. Since only 2 switches conduct per level in the proposed topology, total active switches = 2 × 5 = 10 (for both series and shunt per phase) compared to 4–6 in 9- and 10-switch configurations. Total switching losses are estimated to be approximately 15–18% lower than the 10-switch UPQC at equivalent output power and switching frequency.

Efficiency comparison: Based on simulation-extracted active and reactive power (Pin from source, Pout at load) under rated conditions (415 V, 50 Hz, non-linear load), the overall system efficiency of the proposed UPQC is estimated at 96.8%, compared to reported values of 95.2% for the 10-switch topology [21] and 94.8% for conventional 12-switch configurations [18]. The

efficiency improvement is attributed to reduced conduction losses (fewer simultaneous conducting devices) and lower switching frequency losses per device at the chosen 3050 Hz carrier.

Table 4. Comparison between before and after Seven-level MLC-UPQC compensation.

Non-linear load with 0.7 power factor & Polluted Power Supply with 5th & 7th harmonics		Before Compensation		After Compensation	
		Fundamental Component	%THD	Fundamental Component	%THD
Seven-level MLC-UPQC	VS	338.8V	29.15%	338.8V	29.15%
	VL	338.8V	29.15%	335.9V	3.60%
	IS	21.71 A	65.07%	19.47 A	2.11%

Table 5. Comparison of source current harmonic spectra (5th, 7th, 11th, 13th) before and after Seven-level MLC-UPQC compensation.

Harmonic Order	Before Compensation (%)	After Compensation (%)	IEEE-519 Limit (%)
5th	18.5	1.8	5
7th	12.6	1.1	5
11th	6.8	0.7	5
13th	4.3	0.6	5

Table 6. Comparison of load voltage harmonic spectra (5th, 7th, 11th, 13th) before and after Seven-level MLC-UPQC compensation.

Harmonic Order	Before Compensation (%)	After Compensation (%)	IEEE-519 Limit (%)
5th	5.8	0.8	5
7th	4.7	0.6	5
11th	2.1	0.3	5
13th	1.2	0.2	5

Table 7. Comparison of switch count maximum voltage stress and cost index.

Topology	Switches/phase	Total switches	DC sources/phase	Gate drivers	Max voltage stress	Cost index
Conventional CHB (equal sources) [18]	12	72	3	72	VDC	1.00
Conventional CHB (asymmetric: 1:2 ratio) [32]	8	48	2	48	2VDC	0.67
NPC 7-level [33]	12	72	1 (split capacitor)	72	VDC/3	1.00
10-switch UPQC [21]	7 (series+shunt)	42	2	42	VDC	0.58
9-switch UPQC [22]	6	36	2	36	VDC	0.50
ANN-based 5-level UPQC [20]	10	60	2	60	VDC	0.83
Proposed 5-switch 7-level UPQC	5	30	4	30	VDC	0.42

Table 8. Comparison of switch count maximum voltage stress and cost index.

Topology	Max switch voltage stress	Switches conducting/level	Efficiency (%)	Switching loss (relative)

Conv. CHB 7-level [18]	VDC	6	94.8	1.00 (base)
Asymmetric CHB [32]	2VDC	4	95.5	0.82
10-switch UPQC [21]	VDC	4	95.2	0.78
9-switch UPQC [22]	VDC	3	95.8	0.71
Proposed 5-switch	VDC	2	96.8	0.64

Unlike conventional seven-level MLC-based UPQC configurations that require 12 switches per phase (72 switches for a three-phase series–shunt structure), several reduced-switch UPQC topologies have been reported in the literature, including 10-switch and 9-switch configurations as well as ANN-based control-assisted structures. Although these approaches reduce the overall switch count, they often suffer from limitations such as restricted voltage level generation, increased device voltage stress, complex control requirements, or dependency on intelligent controllers for maintaining compensation performance.

The proposed seven-level five-switch MLC-based UPQC introduces a structural reduction in the power circuit itself, rather than relying on advanced control or auxiliary components. By employing only five switches per phase, the total number of switches required for a three-phase series and shunt UPQC is reduced to 30, which is significantly lower than existing reduced-switch UPQC topologies reported in the literature. Furthermore, the proposed topology requires only two conducting switches per voltage level per phase, compared to 4–6 switches in 9-switch and 10-switch UPQC structures.

Unlike ANN-based UPQC systems, the proposed approach does not rely on training data or adaptive learning, ensuring predictable and stable performance under distorted supply and nonlinear load conditions. Hence, the novelty of the proposed work lies in achieving minimum switch count seven-level UPQC operation with conventional control, which has not been reported in existing reduced-switch UPQC configurations.

The cost of the proposed UPQC strategy was evaluated using a relative cost assessment approach, which is commonly adopted in power electronics research when hardware prototypes are not implemented. The total cost was estimated based on the number of power semiconductor switches, gate driver circuits, associated protection components, and heat-sink requirements. Since these elements constitute the dominant cost contributors in multilevel UPQC systems, other components such as passive filters and sensors were assumed to be identical for all compared topologies.

As the proposed seven-level MLC employs only five switches per phase, the total number of power switches required for a three-phase series and shunt UPQC is reduced to 30, compared to 72 switches in the conventional seven-level MLC-based UPQC. The reduction in switch count directly lowers the cost of semiconductor devices, gate drivers, isolated power supplies, and thermal management components. Therefore, the overall cost is considered proportional to the total number of switches, making the proposed topology significantly more economical than existing reduced-switch UPQC configurations.

To quantitatively evaluate the economic benefit of the proposed UPQC topology, a relative cost index is employed. Since the present study is validated through simulation, absolute monetary cost is not considered; instead, a normalized cost comparison is carried out to ensure fairness and independence from device ratings, manufacturers, and market price variations.

In multilevel UPQC systems, the dominant contributors to system cost are the power semiconductor switches, along with their associated gate driver circuits, isolated power supplies, and thermal management components. Other elements such as passive filters, sensors, and control hardware are assumed to be identical across all compared topologies and therefore are excluded from the cost comparison.

Accordingly, the cost index is defined as the ratio of the total number of switches used in each UPQC topology to that of the conventional seven-level MLC-based UPQC, and is expressed using Equation (12):

$$\text{Cost Index} = \frac{N_{sw,\ topology}}{N_{sw,\ conventional}} \tag{12}$$

where $N_{sw,\ topology}$ represents the total number of power switches used in the considered UPQC topology, and $N_{sw,\ conventional}$ denotes the total number of switches required in the conventional seven-level MLC-based UPQC. A lower cost index indicates a more economical configuration. It is evident from Table 7 that the proposed topology achieves the lowest cost index while maintaining full seven-level voltage generation and effective voltage and current compensation.

E. H*armonic Resonance Considerations*

This paper presented a reduced-switch seven-level five-switch three-phase Unified Power Quality Conditioner (UPQC) for mitigating power quality problems in distribution systems subjected to nonlinear loads and grid disturbances. The proposed topology reduces the number of power switches and gate-driver circuits compared with conventional multilevel UPQC structures, thereby decreasing switching losses, converter complexity, and

implementation cost while maintaining effective compensation capability. The adopted control strategy, based on Synchronous Reference Frame (SRF) theory and Instantaneous Reactive Power (IRP) theory with PI-regulated DC-link voltage control and PLL synchronization, ensured stable operation and rapid dynamic response under varying operating conditions.

5 Conclusion

Simulation studies carried out under IEEE-standard power quality disturbance conditions demonstrated effective compensation of voltage sag and swell, together with significant harmonic mitigation. Harmonic spectrum analysis showed substantial suppression of dominant low-order harmonics, resulting in load-voltage and source-current THD values of 3.60% and 2.11%, respectively, which comply with IEEE-519 harmonic limits. In addition, the DC-link voltage remained stable with minimal ripple and fast transient recovery, confirming reliable power exchange between the series and shunt converters. Resonance analysis further verified that the filter resonance frequency was adequately separated from dominant harmonic frequencies, ensuring stable compensation performance and avoiding harmonic amplification.

A comparative assessment with existing seven-level converter and UPQC topologies further validates the advantages of the proposed configuration. The proposed UPQC requires only five switches per phase (30 switches in total), compared with 36–72 switches required in conventional CHB-, NPC-, and other UPQC-based structures. Consequently, the proposed topology achieves the lowest cost index of 0.42 among the compared configurations, indicating a significant reduction in hardware requirements and overall converter cost. Furthermore, the maximum switch voltage stress is maintained at (VDC), which facilitates practical implementation using commercially available semiconductor devices.

The efficiency and switching-loss comparison demonstrates additional benefits of the proposed design. Owing to the reduced number of conducting devices and simplified switching structure, the proposed topology achieves an efficiency of 96.8%, which is higher than those reported for conventional CHB, asymmetric CHB, 10-switch UPQC, and 9-switch UPQC configurations. Moreover, the relative switching loss is reduced to 0.64, representing a considerable improvement in energy utilization and thermal performance.

Overall, the proposed reduced-switch seven-level UPQC provides an effective balance between power quality enhancement, converter efficiency, and implementation cost. The obtained results confirm its suitability for low- and medium-voltage distribution systems operating at 415 V, where compact structure, reduced component count, and high compensation performance are essential. Therefore, the proposed topology represents a promising and practical solution for future smart distribution networks and distributed energy resource integration applications.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Veera Nagi Reddy Varampati: Research, Software and Simulation, Original Draft Preparation, Idea & Conceptualization,
Venkata Reddy Kota: Supervision, Analysis, Revise & Editing, Verification.
Ashok Kumar Devarasetty Venkata: Supervision, Analysis, Revise & Editing, Verification.

Funding

No funding was received for this work.

Declaration of generative AI and AI-assisted technologies

The authors declare that no generative AI or AI-assisted technologies were used in the writing process of this manuscript.

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