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Power-Gated Memristor-Based Optimized PIPO Shift Register

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Abstract: Memristors are a viable future semiconductor memory substitute because of its nanoscale size, quick switching, low power consumption, and CMOS compatibility. CMOS flip-flops face drawbacks like large size, high power use, and charge loss at smaller scales. However, memristors provide a novel approach to the construction of FFs that improves outcomes. In the previous work, the execution of a four-bit PIPO shift register design was demonstrated using a D flip-flop. D Flip-flops are designed with NAND Gates. In this paper, we will improve the performance of flip-flops by using memristors, followed by the performance of D flip-flops and PIPO shift register using the Power Gating Technique. As the Results Session displays the power usage of the NAND Gate. The power consumption of a D flip-flop using the memristor design is 6.182 µW, while using the power gating technique, the power usage of D flip-flop is 5.827 µW. For DFF Power reduced by 86.1%, Delay reduced by 47.1% and PDP improved by 99.86% compared to conventional design. The power consumption of a PIPO using the memristor design is 22.52 µW, while using the power gating technique, the power usage of PIPO is 21.28 µW. The power consumption of PIPO circuit is reduced by 98.3% compared with conventional design.

Keywords: Flip-flops, NAND Gate, Memristor, Power Gating, Parallel in parallel Out

1 Introduction

SINCE Professor Chua's 1971 prediction and 2008 physical realization, memristors have attracted a lot of attention from researchers [1],[2],[3]. Scaling problems including reliability and power difficulties still exist despite CMOS advancements.The logic architectures like MAGIC, IMPLY, and MRL possible, but due to real-world constraints, hybrid CMOS–memristor circuits are necessary for dependable operation [7],[8].

Flip-flops, which store binary data in two stable states (0 and 1), are essential components of digital systems. Digital circuits frequently use flip-flops, however they require external memory because they lose data when not powered on [10].Memristors reduce complexity and power consumption since they are nonvolatile and maintain flip-flop states when power is lost. Originally the main type of computer memory, shift registers are made of flip-flops and are used to store and transfer binary data. Memristor-based shift registers, in contrast to conventional ones, have the ability to support multiple states, which makes them suitable for sophisticated protocols, analogue computing, and better storage[13].

Therefore, Using memristors, a NOT and NAND gates are built, and flip-flops (FFs) are then designed using this gates.A PIPO (Parallel-In, Parallel-Out) register is then created with designed D flip-flops (DFFs) based on memristors.Power gating method is used for effectively minimizing delay, lowering power consumption, lowering the Power-Delay Product (PDP), and

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improving speed and overall efficiency. The research gap with previous memristor based PIPO design is it consumes large amount of power; this drawback has been covered by use of power gating method which help in reducing the leakage current.

1.1 Outline

The following sections follow the article: Section 2 summarizes the previous work. Section 3 details the about memristor and memristor based gates. In Section 4, proposed flip-flops are explained. Proposed method is showcased in Section 5. Section 6 contain simulation results confirm and performance of the designs. Section 7 conclusion.

2 Literature Survey

Memristors are viewed as prospective memory replacements in the report, which highlights their performance and calls for additional research on materials, integration, and dependability [1]. Advances in memory and logic systems are made possible by authors, which validates Chua's memristor hypothesis [2]. Implemented on a DSP platform, the work presents a chaotic system with hidden attractors based on memristors that exhibits potential for secure communications and encryption [3]. With applications in secure communications and nonlinear systems, authors suggest an intermittent control technique to stabilize a memristor-based hyper-chaotic system [4]. A hyperchaotic memristor circuit on FPGA is presented in 2023 study, allowing for nonlinear modeling and secure communication [5]. Through the use of QCA Designer simulations, this study develops optimised D-latches and shift registers (PIPO, PISO) with QCA, resulting in smaller size, fewer cells, and low delay [6].For future computing, authors suggest MAGIC, a family of logics based on memristors that allows for faster, more compact, and more effective circuits [7].With the help of simulations and Lyapunov analysis, authors demonstrate chaos in a memristor circuit, underscoring its potential for hardware encryption [8].In order to facilitate power-free data storage and CMOS integration for upcoming digital systems, this work introduces memristor-based nonvolatile SR and D flip-flops [9].Memristor-based flip-flops demonstrate strong CMOS integration, provide dependable, nonvolatile memory with 99.9% accuracy after power loss, and have the potential to revolutionize memory architecture [10]. The low power, scalability, and quick switching of memristor-based logic circuits as CMOS substitutes are reviewed in this work. It contrasts various designs, talks about problems and potential fixes, and looks into potential future uses in neural networks, large-scale arrays, and in-memory computing [11]. A compact, low-power, and dependable memristor-based non-volatile latch with MRL and CMOS is presented in this study. With applications in flip-flops, counters, and shift registers, simulations demonstrate a 24% power reduction and a 10% area savings when compared to current topologies [12]. Flip-flops, of which SISO, SIPO, PISO, and PIPO kinds are essential to digital processing, are used in shift registers to handle binary data [13].Two memristor-based N-bit multipliers with IMPLY and MAD logic are shown in the research. MAD outperforms CMOS and allows for efficient Booth multiplication [14]. This study demonstrates the promise of memristors for CAM and small, low-power, nonvolatile logic gates [15].In order to improve PIPO shift registers and make them suitable for low-power digital applications, the study suggests a transistor gating technique that lowers leakage current and power consumption [16]. The work introduces a memristor-based D flip-flop that outperforms CMOS in terms of power consumption, efficiency, and reliability for BIST circuits [17]. In order to improve digital data processing and storage, the study suggests a memristor-based multi-state shift register that uses varying resistance levels to store and transfer more data [18]. In order to increase reliability, streamline design, and preserve data in the event of a power outage, the study suggests non-volatile D latch and flip-flop architectures utilizing CMOS and memristors [19]. The ElProCus article emphasizes how PIPO shift registers, which are used for timing, storage, and transfer, can load and retrieve data quickly and easily in a single clock pulse [20]. In order to enable compact and effective sequential circuits such as PIPO and SIPO shift registers, a low-power QCA D flip-flop is presented [21].Compared to MOSFETs, a PIPO shift register employing AlGaAs/GaAs MODFET D flip-flops exhibits reduced power and latency, providing a more effective design [22].The memristor's theory, initial implementation by HP Labs, and main uses in circuit design and computing are reviewed in this article by authors [23].In order to achieve latching using a memristor–resistor voltage divider, this research suggests a new D-latch that uses a threshold-type memristor with fewer components. Additionally, a modified memristor emulator circuit (MEC) is presented, exhibiting non-volatility and dependable operation via experiments and simulations [24].

3 Memristor Model

The memristor is an effective way to increase the performance of logic circuits. Using memristors, several logic gates have been built, including NOT and NAND. Here, 45nm models are used to design the logic gates.

3.1 Memristor Model

The memristor, a passive part that links magnetic flux and electric charge by having a charge-dependent resistance, was first presented by Professor Leon Chua in 1971[1]. A device that retains data by altering its resistance is called a "memristor," a combination of the words "memory"+"resistor." While a tiny current senses voltage to read data, a big current changes resistance to write data. Because of this, memristors are helpful for storing non-volatile memory[14]. Memristors are two-terminal, non-volatile components that work with contemporary integrated circuits. They change resistance according to the charge flow by connecting magnetic flux and electric charge. They react to charge rather than voltage and do not store energy like other components do[15].

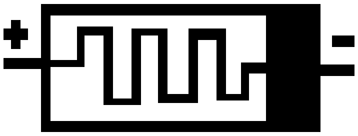

Fig 1. Symbol for Memristor.

The symbol for the memristor is displayed in Figure 1. The black bar at the right terminal is negative, while the one at the left is positive. When the voltage falls below Vreset, a memristor transitions to a High Resistance State (Roff), and when it rises over Vset, it converts to a Low Resistance State (Ron). Otherwise, resistance remains constant. Beta determines the switching speed; faster transitions are made possible by larger β. Because Ron and Roff stand for binary 1 and 0, memristors are perfect for nonvolatile memory. Even when the power is turned off, data can be written with high voltage and read with low voltage [9]. Characteristic of memristor is showed in Figure 2.

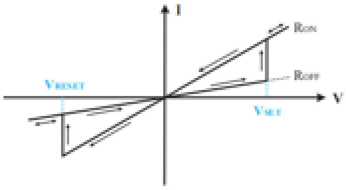

Fig 2. Current-Voltage characteristic of memristor.

3.2 Proposed NOT Gate

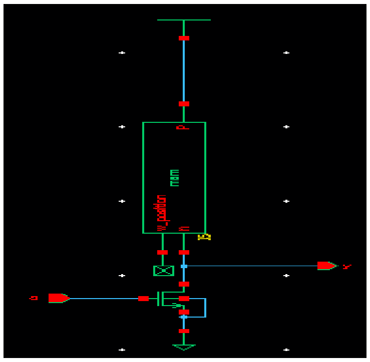

Fig 3. Memristor based NOT.

Figure 3,This is memristor based NOT gate only the NMOS will be present at the design in the place PMOS we have used the memristor. The output will be false if the input is true. In the same way, a fake input yields a genuine output.

3.3 Proposed NAND Gate

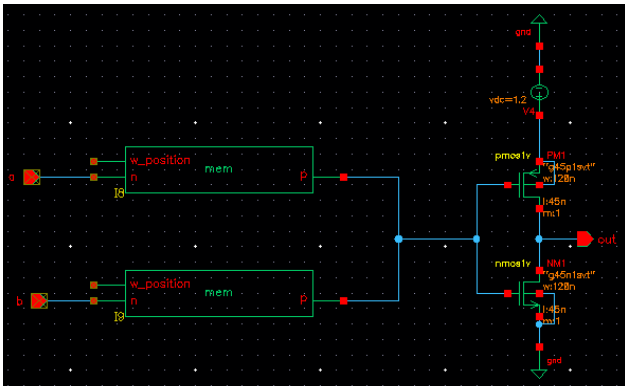

Fig 4. Memristor based NAND

The above Figure 4 shows the NAND gate using memristors, where 2 memristors are connected in parallel to the polarities. When A = B = 1, both NMOS transistors are ON and both PMOS are OFF, creating a path to GND, pulling the output low (0).In all other cases, at least one PMOS is ON or one NMOS is OFF, so the output is high (1), which matches the NAND gate behavior.

4 Proposed Memristor Based Flip-Flops

4.1 SR Flip-Flop

An SR flip-flop using NAND gates consists of two cross-coupled NAND gates, forming a feedback loop between the gates. This configuration allows the flip-flop to store a bit of data based on the Set (S) and Reset (R) inputs. The operation of the SR flip-flop can be summarized in a truth table: The output Q is set to 1 and Q' is set to 0 when S is high (1) and R is low (0); Q is reset to 0 and Q' is set to 1 when S is low (0) and R is high (1). When S and R are both low (0), there is no change because the outputs remain in their initial states. But when S and R are both high (1), the flip-flop's state is deemed invalid, resulting in an indeterminate state. There are two NAND gates in the circuit design. The first gate receives inputs S and Q' to generate output Q, while the second gate receives inputs R and Q to generate output Q'. Figure 5 displays SR Flip-flop using NAND gates.The NAND gates used here is memristor based gate, which has been illustrated Figure 4.

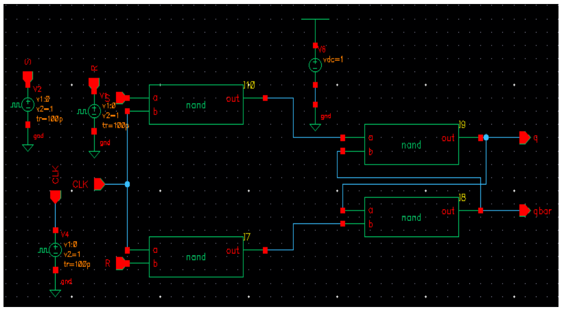

Fig 5. Memristor based SR Flip-Flop.

4.2 JK Flip-Flop

Using inputs J (Set) and K (Reset) and outputs Q and Q', a JK flip-flop is a sequential circuit that stores a single bit of data. It can function asynchronously in the absence of a clock or synchronously with one.We can look at its structure diagram below in Figure 6. Two 3-input NAND gates with third inputs connected to Q and Q' are used in place of two 2-input AND gates. When J = K = 1, the JK flip-flop can be toggled thanks to this interlocking. Since Q and Q' are always opposite, the NAND gates ensure correct control by blocking J or K as necessary.When both inputs "J" and "K" are set to 1, the flip-flop switches between states based on the truth table. The JK flip-flop operates based on the J and K inputs. The output is unaltered when both are 0. The output returns to 0 if J and K are both 0. The output is set to 1 if J is 1 and K is 0. The output alternates between 0 and 1 depending on the current condition when both J and K are 1.The NAND gates used here is memristor based gate, which has been illustrated Figure 4.

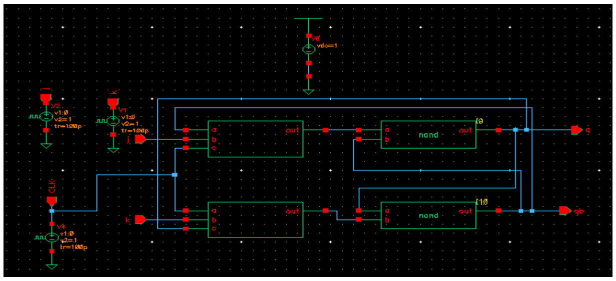

Fig 6. Memristor based JK Flip-Flop.

4.3 D Flip-Flop

To guarantee that data is only stored on the clock edge, a Master-Slave D Flip-Flop sequentially employs two D flip-flops. To improve timing control, the slave updates the output on the opposite clock edge, which is typically falling, while the master records input on one edge, which is typically rising.

This method ensures steady data flow in sequential circuits and helps avoid problems like race circumstances.Master-Slave D Filp-Flop is showcased in Figure 7. To develop it, NAND and NOT gates based on memristors, which are shown in Figures. 4 and 3. A clock regulates two latches in the master-slave D flip-flop: when the clock is low, the slave copies the master while the master retains its value, and when the clock is high, the master follows the input while the slave is off. This avoids race situations and guarantees steady output.

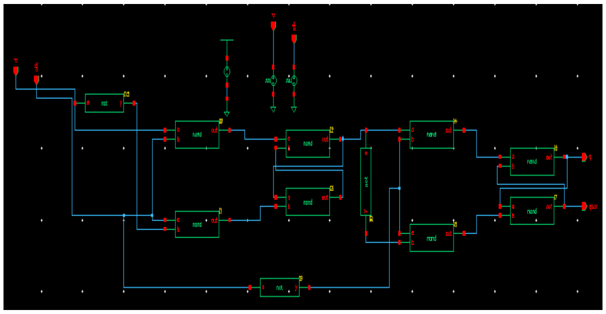

Fig 7. Memristor based D Flip-Flop.

4.4 T Flip-Flop

An XOR gate and a D flip-flop are used to create a T flip-flop, which efficiently switches its output state depending on the T input. The output can act as a memory element that changes state depending on the input condition when T is low since it stays the same when T is high and toggles on each clock pulse when T is high. Figure 8 shows T flip-Flop. To design T Flip-Flop we have used memristor based D Flip-Flop which has been illustrated Figure 7. The flip-flop's current output (Q) and T input (toggle) serve as the inputs for the XOR gate.The output (Q) doesn't change while T is zero; it toggles when T is one.

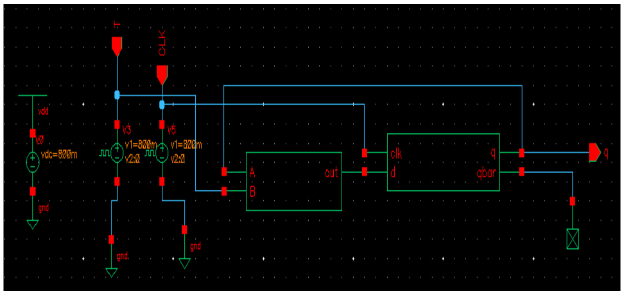

Fig 8. Memristor based T Flip-Flop.

5 Parallel In-Parallel Out Shift Register (PIPO)

A shift register is a type of sequential circuit in which the input and previous output determine the output. It stores and shifts binary data using cascaded flip-flops. For instance, two flip-flops hold 2-bit data. The number of flip-flops corresponds to the number of bits saved.A PIPO shift register loads and outputs data in parallel across several input and output lines using a single clock signal. It can function as a time delay device and enables quick data transfer and temporary storage. It processes entire data words in a single cycle, in contrast to serial registers [20].

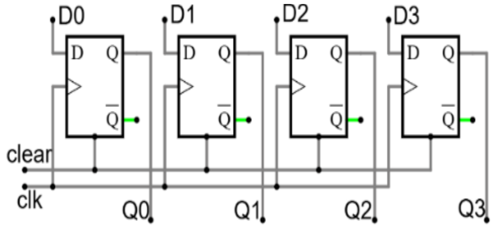

Fig 9. Parallel In Parallel Out Design.

Figure 9 shows circuit of PIPO.In a PIPO shift register, every data bit that is entered in parallel shows up at the outputs simultaneously. A four-bit PIPO register uses D flip-flops to accept inputs (Ds) and simultaneously output them (Qs) when timed.

6 Proposed Methodology

Figure 10 shows the step by step workflow of the proposed design.

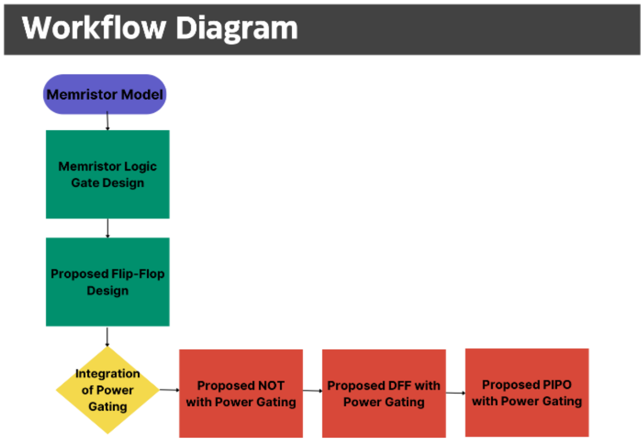

Fig 10. Workflow of the Proposed Design.

6.1 Power Gating Technique

Power gating turns off unused blocks in integrated circuits to lower power consumption. This is perfect for contemporary chips and battery-powered gadgets since it reduces leakage current and conserves energy.The Technique of power gating is displayed in Figure 11.

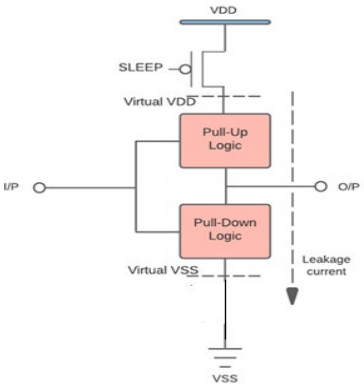

Fig 11. Power Gating Technique.

In order to preserve energy and cut off power to unused blocks, power gating uses switches in circuit power lines that are managed by a power unit. Figure 12 showes the extension part where power gating method is applied to the pmos transistor &vdd supply via that pmos transistor, due to this power consumption of the design is reduced.

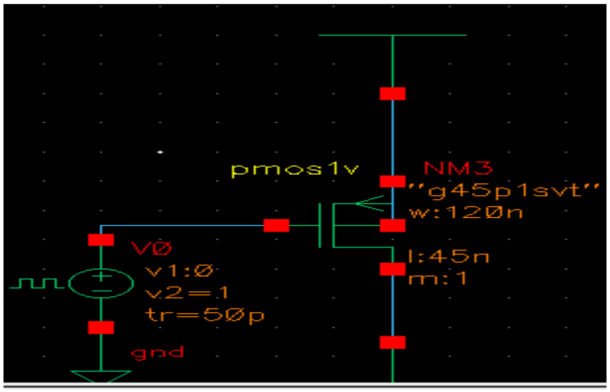

Fig 12. PMOS Transistor for Power Gating.

6.2 Proposed NOT Gate by Power Gating

Figure 13 showes the proposed NOT gate design with power gating it completely disconnects the gate from the power supply to reduce leakage power when the gate is not in use. Here pmos transistor of power gating showed in Figure 12 is added to the memristor based NOT gate which is represented in Fig 3. The output is the logical inverse of the input, and it requires a single input.

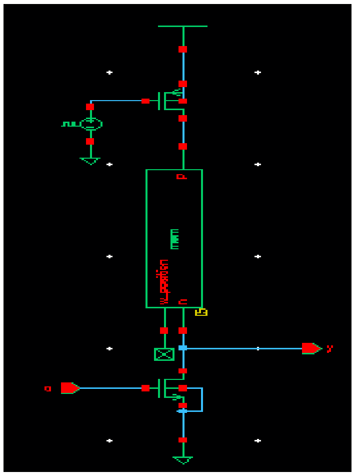

Fig 13. Proposed NOT gate with Power Gating to reduce Leakage Current.

6.3 Proposed DFF by Power Gating

Figure 14 is showing D Flip Flop (DFF) by use Power gating Technique. In this design ,3 NOT Gate Circuits of the D flip flop are replaced by proposed NOT gate circuit. It helps in reducing the power consumption and delay of DFF.

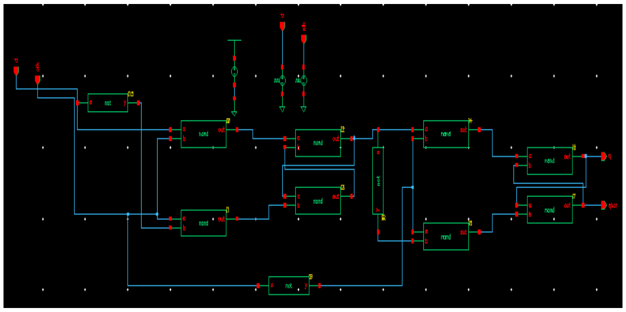

Fig 14. Proposed DFF with Power Gating to reduce Leakage Current.

6.4 Proposed PIPO by Power Gating

Figure 15 is showing PIPO circuit by use Power gating Technique. In this Circuit, Power Gating Based proposed D Flip Flop(DFF) which is has been set out in Fig 14 is used. This D Flip-Flops are arranged in parallel in such a way that each DFF receives a separate input and has its own output and due to this leakage current is reduced.

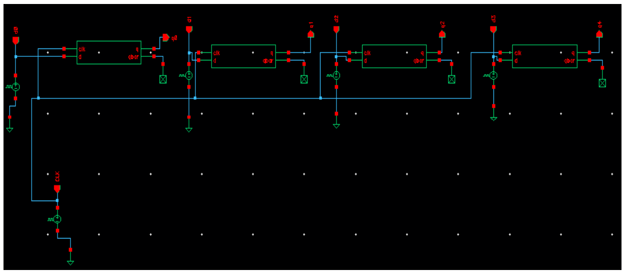

Fig 15. Proposed PIPO with Power Gating to reduce Leakage Current.

7 Results

Design and simulations of all circuits are conducted using Cadence Virtuoso with 1.2 V supply, room temperature and 45 nm CMOS technology.

7.1 Gates and Flip-Flops

Table 1 represents the compression of performance parameters of gates and flip-flops. The performance of flip-flops and logic gates based on memristors, including new Proposed designs, is compared in this analysis. The proposed NOT gate is extremely energy-efficient due to its significantly lower power consumption and improved Power-Delay Product (PDP). The performance of gates and Flip-Flips.

In comparison, the Proposed D-Flip-Flop achieves minor reduction in parameters, indicating a trade-off, where speed is surrendered for power in this design. The data demonstrates the need for balanced optimisation across different circuit types while also highlighting the potential of memristors for low-power applications, especially with optimised designs.

Table 1. The compression of performance parameters of gates and flip-flops.

	Power Consumption((µW)	Delay(ps)	PDP(fJ)
Proposed Memristor Based NOT	0.00985	15.32	0.150902
Proposed NOT with Power Gating	0.000003122	23.24	0.026362
Proposed Memristor Based NAND	0.426	4.812	2.049912
Proposed Memristor Based SR Flip-Flop	3.174	40.96	130.0
Proposed Memristor Based JK Flip-Flop	5.195	44.83	232.9
Proposed Memristor Based T FF	7.043	104.7	737.4
Existing DFF[17]	41.96	508	21315.68
Proposed Memristor Based DFF	6.182	308.1	1904.6742
Proposed DFF with power gating	5.827	268.5	1564.5495

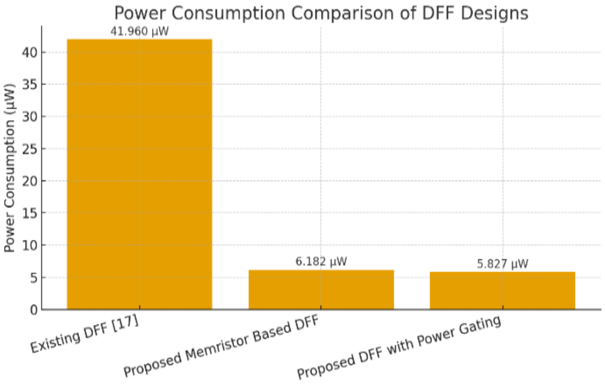

Fig 16. Power Comparison of DFF

Here in Figure 16, The power consumption of the three DFF designs is shown graphically. The suggested designs use substantially less power than the current DFF, as the illustration makes it clear.

A graphical comparison of DFF Delay is presented in Figure 17. The graph illustrates how much less latency the suggested designs cause as compared to the current DFF.

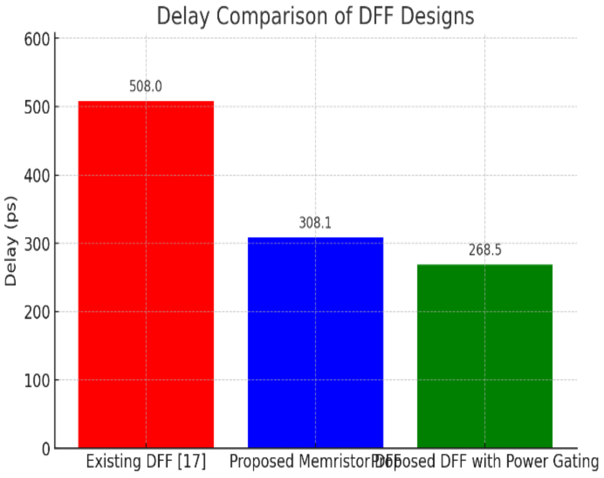

Fig 17. Dealy Comparison of DFF

7.2 PIPO Design

Figure 18 presents design of PIPO by use of both memristor based D Flip-Flop and Proposed memristor based DFF which are shown in Figures 7 and 14, respectively. Figure 19 displays the waveform of PIPO. A 4-bit binary word is stored in a 4-bit Parallel-In Parallel-Out (PIPO) shift register using four D-type flip-flops. All four bits are input simultaneously on a single clock edge and are always accessible at the outputs because data is loaded and retrieved in parallel. As a crucial buffer or latch in digital systems, it is therefore extremely effective for quick, synchronous 4-bit data store and retrieval in a single clock cycle.

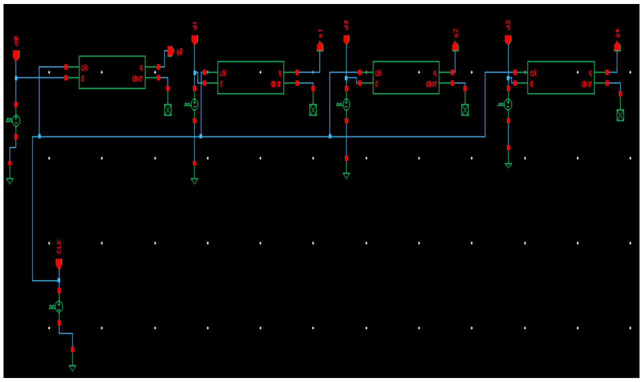

Fig 18. PIPO Shift Register

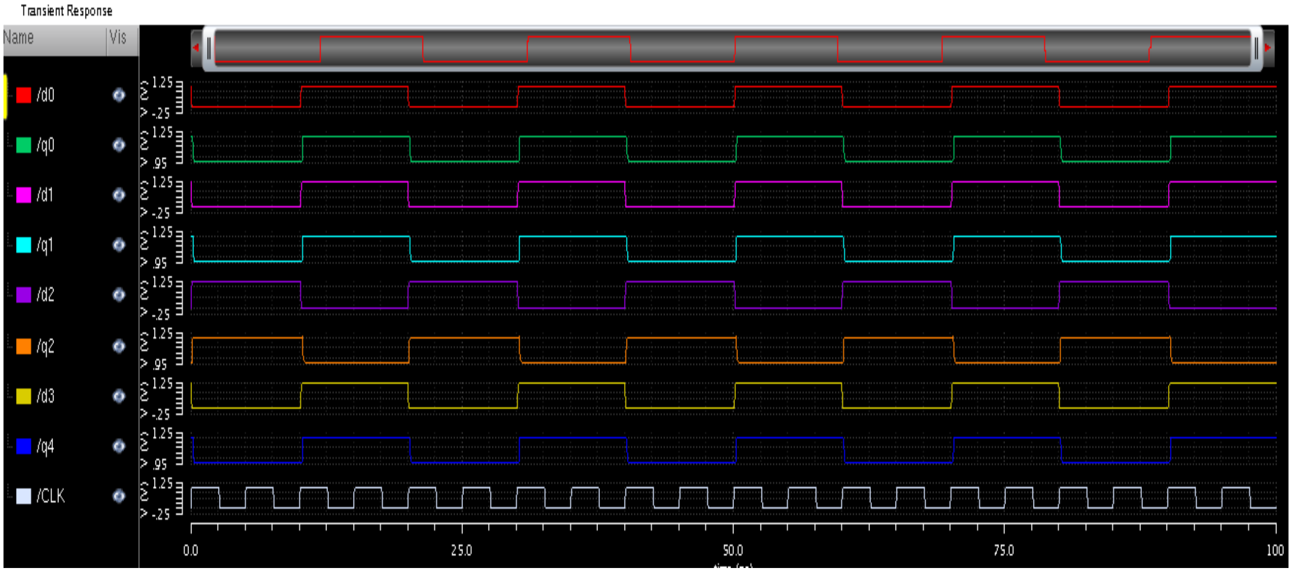

Fig 19. Waveform of PIPO Shift Register

Table 2 shows performance of PIPO. Table 2 represents the performance parameters of both PIPO shift register. We can see the Proposed PIPO with power gating reduced power by 5.5%, and delay by 16.5% when compared with proposed memristor based PIPO. But at the cost of increased area when compared with memristor based PIPO.

A graphical comparison of the three PIPO designs' power usage is displayed in Figure 20. When compared to the current PIPO, the suggested memristor-based and power-gated versions exhibit a drastic decrease.

Table 2. Performance of PIPO Shift Register.

	Power Consumption (µW)	Delay(ns)	PDP(fJ)	Area(µm^2)
Existing PIPO[16]	1340	-	-	-
Proposed Memristor based PIPO	22.52	192.1	4.326	76
Proposed PIPO with power gating	21.28	160.4	3.405	88

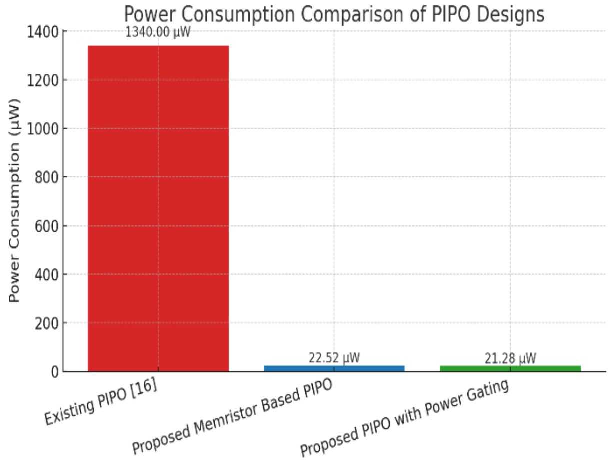

Fig 20. Power Comparison of PIPO Shift Register

A graphical comparison of the three PIPO designs' power usage is displayed in Figure 20. When compared to the current PIPO, the suggested memristor-based and power-gated versions exhibit a drastic decrease.

It has been noted that a little greater space is needed for the suggested design. This increase is offset by significant improvements in power efficiency and delay performance. Since power and speed are critical characteristics in modern VLSI design, the trade-off justifies the space overhead while making the suggested architecture more efficient for realistic applications.

8 Conclusion

In this research, Cadence virtuoso tool has been used to design all the designs. The design of a 4-bit PIPO shift register utilising memristor-based NOT and NAND gates is demonstrated in this study. Flip-flops were implemented using a master-slave setup, while NOT gates and DFFs were optimised by the use of power gating techniques. The proposed PIPO design was successfully validated through simulation, highlighting its effectiveness and energy efficiency. Power consumption of PIPO reduced from 22.52 µW to 21.28 µW and Delay has been reduced from 192.1 ns to 160.4 ns, when compared between two proposed PIPO. Power reduction is 98.3% of proposed PIPO with power gating when compared with current PIPO. However, further work can concentrate on reliability analysis, hardware prototype, scalability to higher bit registers (8-bit, 16-bit), and memory module integration for small storage. In the Future, we can work at Area also. We can reduce the Area of the circuit.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

E. Vijaya Babu: Conceived the research idea, conducted experiments, analyzed the data.

G. Shanthi: wrote the manuscript. Supervised the research.

Ayesha Thabassum Ara: conducted experiments, analyzed the data, and contributed to the interpretation of the results.

K V Balaramakrishna: provided guidance on methodology

Madhu Nakirekanti: reviewed the manuscript

K Narsimha Reddy: created visuals in the manuscript

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