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Contemplation of QCA based Cryptographic Nano Communication Circuit using Multilayer Approach

Paramjeet.*, Saptarshi Gupta*(C.A.), Rupali Singh*

Abstract: CMOS technology, after contributing a lot to electronics world, is now facing difficulties in designing of more efficient circuits in terms of compactness, power efficiency and speed. It is happening due to various side effects being generated on account of further down scaling of feature size. The Quantum Dot Cellular Automata (QCA) technology seems to be alternate and promising technology for designing of more efficient circuits. The cryptographic encoder and decoder are the key component for secure and safe communication. This paper presents an efficient design of 1:2 demultiplexer, 1:4 demultiplexer and 4:1 multiplexer which are further used to design a cryptographic nano communication circuit. The proposed circuits are efficient in terms of energy, area and speed. The architectures are designed through multilayer approach in QCA technology that makes it compact. The efficiency of the proposed circuits has been verified through the tool QCA Designer 2.0.3.

Keywords: Quantum Dot Cellular Automata, multiplexer, demultiplexer, multilayer design, cryptographic architecture, nano communication.

1 Introduction

THE CMOS technology, the most dominating technology, is serving the electronics industry since last several decades. But, now, due to several limitations like short channel effects, leakage currents, power dissipation, and etc., the said technology will not be able to continue its journey in very near future. Therefore, it is imperative for the researchers to work on the other alternative technologies. However, a number of technologies, viz. Single Electron Transistor, Resonant Tuning Diode, Quantum Dot Cellular Automata and Carbon Nano Tubes etc., are being researched, but, as per International Technology Roadmap for Semiconductor (ITRS), Quantum Dot Cellular Automata (QCA) has the potential to be the most effective and emerging technology [1]. The technology is capable of producing high speed, compact and consuming low power logic circuits. Using QCA technology, an extensive work has been carried out and a number of efficient combinational as well as sequential circuits have been designed by the researchers. The process of designing more efficient circuits using QCA technology is still going on, but, not much work has been done in the field of cryptography using QCA technology. The QCA technology can play an important role in securing the communication system. The messages have to be protected from the unauthorized access for the safe and secure communication. Thus, in cryptography, the message to be sent is first converted into the unreadable form through encoder and then the encrypted message, also called as cipher text, is decoded back to original message i.e. plaintext with the help of decoder at the receiver side. The encoders and decoders are the key components of the cryptography. The QCA technology can be utilized in designing of the encoders and decoders for the secure communications.

This paper presents an efficient design for cryptographic nano communication circuit using QCA technology. The structure of the paper is organized as follows: Section 2 presents the basic background of QCA and cryptography, Section 3 discusses the existing designs and research gaps. The proposed QCA structure of the multiplexer, demultiplexer and cryptographic nano communication circuit is given in the section 4.

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*The authors are with the Department of Electronics and Communication Engineering, Faculty of Engineering and Technology, SRM Institute of Science and Technology, Delhi-NCR Campus, Modinagar, Ghaziabad 201204, U.P., India.
E-mails: chauhan.paramjeet@gmail.com, ece.saptarshi@gmail.com and rupal.rishi@gmail.com
Corresponding Author: Saptarshi Gupta

Section 5 gives the discussions on simulation results of the proposed circuits and the paper is concluded in Section 6.

2 QCA and Cryptography Background

C.S. Lent, in 1993, introduced the Quantum Dot Cellular Automata technology [2]. The devices designed with QCA technology are found to be more efficient in terms of area, energy and speed as compared to their counterparts in CMOS technology. The QCA technology is based on the different concept in which the logics states are defined according to the electrons position in the QCA cell rather than the voltage or current level as happens in CMOS technology. Several researchers have designed and fabricated the devices with the use of QCA technology. The fabricated devices have been tested successfully which shows the feasibility of QCA technique [3], [4]. Recently, due to advancement in QCA technology, several combinational as well as sequential circuits are being extensively researched by the researchers [5], [6], [7], [8], [9].

2.1 QCA Cell

The QCA cell is the basic component in QCA technology having four quantum dots consisting of two electrons as shown in the Fig. 1.

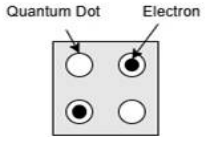


Fig 1. QCA Cell

The quantum dots are connected through a tunnel via which the electrons can move from one quantum dot to the other one. Due to the coulombic repulsion, the electrons will always occupy the antipodal position in the cell [10]. Thus, there are two possible positional arrangements of electrons in the cell, as shown in the Fig. 2 and the two polarizations P = -1 and P = +1 represent Logic ‘0’ and Logic ‘1’, respectively.

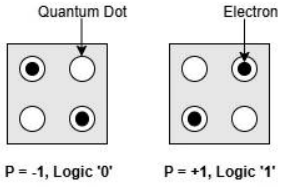


Fig 2. Polarizations of QCA Cell

2.2 QCA Wire

The wire can be designed in QCA technology by placing the QCA cells in a queue. The cell placed adjacent to other cell will influence the polarization of the quantum cell due to coulombic interaction between the electrons of both the cells. The QCA wire can be formed with two different techniques, as shown in the Fig. 3, and wires made with these arrangements are called 90° Binary Wire and 45° Binary Wire.

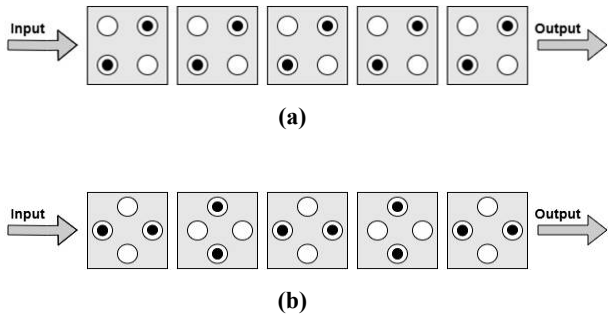


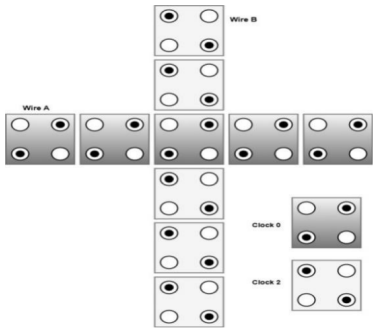
Fig 3. QCA Wire **(a)** 90° Binary Wire **(b)** 45° Binary Wire

The information can be transferred to next cell with the help of transfer of the polarization from one cell to next cell as each cell influence the polarization of its next cell due to coulombic repulsion between the electrons of neighbor cells. There is a difference between 90° Binary Wire and 45° Binary Wire. The value at input cell of 90° Binary Wire is transferred to the consecutive cell and finally to output cell without any change but in case of 45° Binary Wire, each cell will have the opposite polarization to its adjacent cell and thus both logics i.e. logic ‘0’ and logic ‘1’ are propagated simultaneously.

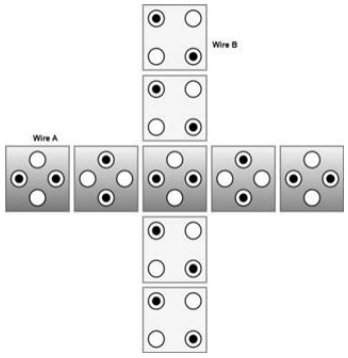
2.3 QCA Wire Crossover

In QCA technology, the crossing of wire can be implemented with two approaches: single-layer wire crossing also called as coplanar wire crossing and multilayer wire crossing. The single-layer wire crossing is further implemented with two different approaches. In first approach, logical wire crossing is implemented and 180° phase difference is incorporated between the crossing wires, as explained in Fig. 4(a). In the second approach, the wire crossing is done with the help of an inverter chain, as demonstrated in Fig. 4(b).

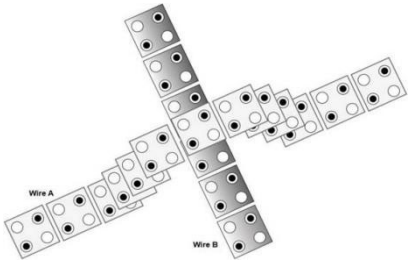
The multilayer wire crossing is implemented with the help of at least three layers, as shown in Fig. 4(c). Further, as discussed earlier that when the cells are placed adjacently, these are polarized in the similar state. But, when the cells faces each other, then the cells will be polarized in the opposite state, as depicted in Fig. 5(a).



(a)

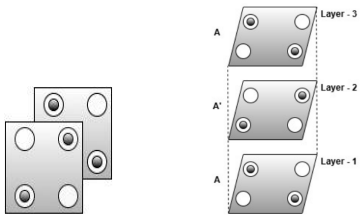


(b)



(c)

Fig 4. QCA Wire Crossing **(a)** Coplanar Logical Crossing **(b)** Inverted Chain Crossing **(c)** Multilayer Crossing



(a) (b)

Fig 5. QCA multilayer cells **(a)** Facing Cells **(b)** Logic Inversion in layers

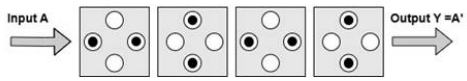
Thus, placing the cells vertically over one another will always be in opposite polarization and consequently the logic gets inverted when propagated from one layer to other layer, as illustrated through Fig. 5(b).

2.4 Basic Gates

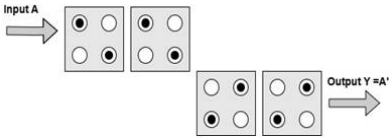
Various logic functions can be designed by arranging the QCA cells properly. There are some basic gates in QCA technology which can be further used for designing of other combinational and sequential circuits. The main basic gates in QCA technology are inverter and majority Gates [10].

2.4.1 QCA Inverter

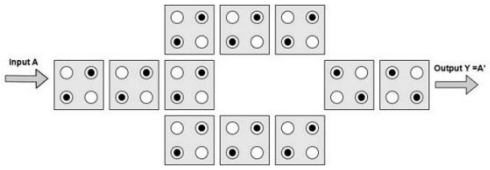
The important designs of QCA inverter are shown in the Fig. 6 (a), (b) and (c). The 45° Binary Wire with even number of cells can be used as inverter as depicted in the Fig. 6(a).



(a)



(b)



(c)

Fig 6. Inverter gate

The 90° cells placed diagonally can behave like not gate as illustrated in two different deigns in Fig. 6 (b) and Fig. 6(c).

2.4.2 QCA Majority Gate

Majority gate is the key circuit used to design other complex circuits due to its special functionality. It consists of three input cells, one device cell and one output cell. Output cell maintains it polarization equal to that polarization which is shown by the majority of the input cells. As the output follows the majority of the input cell's polarization, hence it is named as majority gate. There are two types of majority gates categorized as Original Majority Gate (OMG) and Rotate Majority Gate (RMG) which are shown in Fig 7.

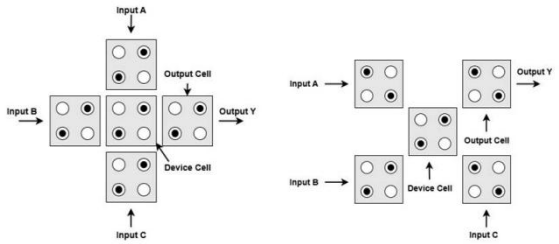


Fig 7. Majority Gates (**a)** Original Majority Gate (OMG) (**b)** Rotate Majority Gate (RMG)

The output and input relationship can be denoted by the equation 1 below.

$$Y = Maj (A, B,C) = AB + BC + CA \quad (1)$$

Majority gate can function like AND gate and OR gate, if one of its input is set to polarization equals to +1 and -1, respectively. Further, 5-Input majority gates also exist which helps in designing of various QCA circuits.

2.5 Clocking in QCA circuits

No additional power supply is given in the circuits designed through QCA technology. The clock pulse serves the both purposes, power supply to the circuit as well as controlling and synchronization of the cells for transfer of the information. As shown in the Fig. 8, the clock consists of four phases viz. Switch, Hold, Release and Relax phase [11].

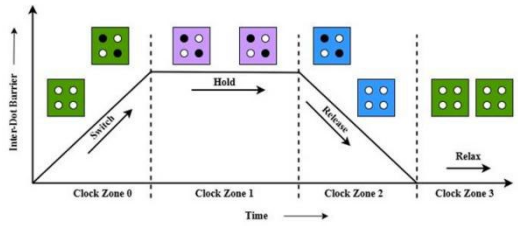


Fig 8. QCA Clocking

- **Switch Phase:** In this phase, the clock signal adiabatically goes from low state to high state due to which the inter-dot barrier rises up. Thus, in this situation, the neighboring cells can influence the cell polarization and this phase allows the computations.
- **Hold Phase:** The polarization of the cell is made at hold position and thus, the electron will not be able to move from its existing position.
- **Release Phase:** During release phase, the clock goes adiabatically from the high state to the low state resulting movement of inter-dot barrier towards zero and this turns the QCA cell un-polarized.
- **Relax Phase:** During the relax phase, the cell remains in un-polarized state as the clock is at low state.

2.6 QCA implementation techniques

The manufacturing of QCA-based nano computers is problematic today but "simulation-based designs drive the QCA nanotechnology forward" [12]. There exist a few techniques for the physical implementation of the QCA designs, the main four techniques are outlined below:

2.6.1 Metal-Island QCA

The metal islands are made of aluminum. The QCA cell is made up of capacitive coupled metal islands [13]. The drawback of this technique is its difficult working at room temperature as the Metal-island QCA works on cryogenic temperature. It is highly sensitive to temperature and noise.

2.6.2 Semiconductor QCA

The quantum dots are fabricated with the use of semiconductor material such as InAs/ GaAs and GaAs/ AlGaAs etc. [14]. The CMOS technology can be used to fabricate the QCA cells. The mass production of the cells is difficult with semiconductor QCA.

2.6.3 Molecular QCA

It is based on the specially designed molecule that acts as a cell. This technique is considered as best of the fabrication technique as the designs fabricated with this technique are able to work at room temperature. Further, it also support mass production of cells and able to produce high density circuits [15]. It is able to produce the circuits with high switching speed and symmetric cell structure.

2.6.4 Magnetic QCA

It was proposed by Cowburn and Welland. The nano dots which are made of magnetic supermalloy are placed in a straight line fashion and an oscillating field is applied to the dot. It has the advantage of working at room temperature, but the designed circuits work on low frequency [16].

2.7 Cryptography

Cryptography word is derived from the Greek word 'kryptos' meaning "secret writing". Thus, cryptography can be considered as a technique used to secure the information or message during communication, so that no unauthorized party can read or decode the information [17]. The cryptography is based on the following four principles.

- **Confidentiality** means rules, instructions and guidelines that are followed to ensure the data is only for specific persons or places.
- **Data integrity** means to ensure the correctness, consistency and accuracy of the information during the complete process of the communication.
- **Authentication** means to ensure the authenticity of the sender whether data being sent belongs to him/ her or not.
- **Non-repudiation** is a mechanism adopted in communication due to which a person cannot deny the action done by him/ her.

The block diagram of the cryptography is given in Fig. 9.

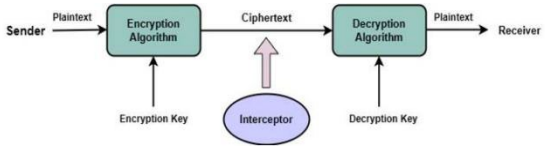


Fig 9. Cryptography Block Diagram

As shown in the block diagram, the sender converts the plain text (message to be sent) into cipher text (encoded or encrypted message) through the encryption process. The cipher text is transmitted through the channel which is decoded/ decrypted by the receiver through decryption process.

The process of converting the data or information to be sent into secure/ encrypted data at the sender side is called the encryption and converting back it to the original form at the receiver end is called as decryption process. The encryption and decryption process are completed with the help of a secret key. As truly stated by Kerckhoff "All algorithms must be public; only the keys are secret".

However, huge work has been done on cryptography and numerous circuits like encoders/ decoders have been designed using CMOS technology, but, due to the limitations in CMOS technology, the designing of more efficient circuits is becoming difficult for the researchers. Side Channel Analysis attack which is based on power analysis is serious issue in CMOS technology based cryptography. So, the researchers are moving towards other different alternatives like Single Electron Transistor (SET), Carbon Nano Tubes (CNT) and Quantum dot Cellular Automata (QCA) etc.

Single Electron Transistor (SET) operation is based on the controlled tunneling of a single electron through an "island." It uses Coulomb blockade phenomena. Single-Electron Transistors are able to produce the designs which consume very low power, immune to noise and have reduced dimensions. The SET has a drawback of being sensitive to environment conditions especially to temperature. Further, it is very difficult to interface the Single Electron Transistor (SETs) with the external environment. Thus, SET is impractical for large-scale circuits due to temperature and noise sensitivity.

Carbon Nano Tubes(CNT) uses carbon nano tubes as channels in transistors. CNTs can behave like ballistic transport devices that offer high mobility. The fabrication imperfections, complex and costly manufacturing process are the main obstacles in its way.

The major issues with the QCA technology are difficulty in fabrication and expensive lithography. Due to nano scale size, there is possibility of defects in QCA devices. QCA requires precise placement of quantum dots; challenging at nanoscale. QCA devices are extremely vulnerable to various defects like cell misalignment, dot displacement, missing or additional dots and edge roughness etc. Even a single defective cell in the architecture can leads to malfunctioning or non working of the circuit. Further, the wires in QCA are made up of chain of cells. The long wires in QCA lead to signal degradation, delay and error. Issue of crosstalk also arises in dense circuits.

The issues in QCA are being addressed by the researchers and the technology is growing due to its ability to produce high speed, compact and low power circuits. Thus, among the current alternatives available, Quantum Dot Cellular Automata (QCA) seems to be more efficient for the designing of high speed, area and power efficient circuits. Extensive research is being carried out in QCA and more efficient logic circuits are being designed by the researchers, but, not much work has been done in the field of cryptography with the use of QCA. However, some researchers have designed cryptographic architecture in coplanar mode but work done in multi-layer mechanism is limited. Thus, a great potential is available for designing of cryptographic architecture in multi-layer system using QCA that motivated for the proposed designs.

To maintain methodological consistency, the present work restricts its evaluation to existing QCA implementations; direct comparison with other nanoscale technologies is not feasible and lies beyond the scope of this paper and cannot be performed reliably due to incompatible modeling assumptions.

3. Related work on QCA Nano communication Circuits and research gaps

Previous research on cryptographic architecture and nano communication in QCA has made significant strides in optimizing circuit design and efficiency.

Quantum-dot Cellular Automata (QCA) is an advanced and emerging technology for nanoscale circuit design. Nano communication circuits rely heavily on data path selectors as a fundamental component for signal routing. These selectors typically integrate multiplexers and demultiplexers to control data flow. Various research efforts have been conducted to optimize these components. Research Paper [18] presents a multilayer QCA layout for the data path selector, consisting of nine layers and requiring 419 cells. The design was simulated using the coherence vector engine of the QCA Designer tool. Research Paper [19] introduces a cryptographic nano router, incorporating multiplexers and demultiplexers within its architecture. The complete cryptographic design utilized 581 cells, with a total area of 1.14 μm². The area usage was reported as 16.5%, with a latency of 5.50 clock cycles.

The design and optimization of 4:1 multiplexers in QCA technology have been extensively studied. Research Papers [20-23] propose various 4:1 multiplexer structures with different cell counts and area requirements. Research Paper [20] utilized 215 cells with an area of 0.25 μm². Research Paper [21] required 166 cells and occupied an area of 0.27 μm². Research Papers [22], [23] optimized designs using 107 cells, with areas of 0.17 μm² and 0.15 μm², respectively.

Prior research has also explored the development of 1:2 demultiplexers, with most of these designs being coplanar structures. Research Paper [24] presents a 1:2 demultiplexer requiring 21 QCA cells and occupying an area of 0.03 μm², with a delay of 0.50 clock cycles. Research Paper [25] also utilizes 21 cells but achieves a more compact area of 0.017 μm² while maintaining the same delay of 0.50 clock cycles. In Research Paper [26], the design required 27 cells and occupied 0.04 μm², with a delay of 0.50 clock cycles. Similarly, Research Paper [27] utilized 21 cells, covering an area of 0.02 μm² and maintaining a delay of 0.50 clock cycles. Lastly, Research Paper [28] proposed a design that employed 32 cells with an area of 0.026 μm², also achieving a delay of 0.50 clock cycles. These studies demonstrate ongoing efforts to optimize the design and efficiency of 1:2 demultiplexers in QCA technology.

Expanding on the research surrounding 1:4 demultiplexers, several studies have focused on the development of 1:4 demultiplexers. Various designs have been proposed, each utilizing different optimization techniques. Research Paper [24] presents a 1:4 demultiplexer constructed using four 3-input AND majority gates and two inverters, requiring 187 quantum cells and occupying an area of 0.18 μm², with a latency of 1.75 clock cycles. Research Paper [25] employs a multilayered approach, utilizing 140 cells with an area of 0.102 μm² and a delay of 1 clock cycle. In Research Paper [29], the design consists of 149 cells and covers an area of 0.21 μm². Research Paper [30] adopts the wire crossing cell state difference approach, using 125 cells, occupying an area of 0.15 μm², and achieving a delay of 1.25 clock cycles. Research Paper [26] integrates rotated cells for wire crossing, requiring 188 cells and an area of 0.22 μm², with a latency of 1 clock cycle. Finally, Research Paper [19] employs 150 cells, occupying an area of 0.18 μm², with a latency of 1.75 clock cycles, while also utilizing the crossover cell state difference approach. These studies illustrate the continuous advancements in optimizing 1:4 demultiplexer designs within QCA technology.

4. Proposed QCA Nano communication Circuits

The cryptographic architecture designed with the help of proposed multiplexer and demultiplexer is presented. The cells of the design are spread over the three layers that make it area efficient. The multiplexer and demultiplexer followed by cryptographic nano communication circuit are explained in subsequent sub-sections. The proposed cryptographic architecture is composed of three primary sections: the encoder, the communication channel, and the decoder. The encoder comprises XOR gates[31], which process the original input along with encrypted keys to generate the cipher text. Following this, the cipher text is transmitted through a data path selector and router, which is implemented using multiplexers and demultiplexers to facilitate efficient data flow. Finally, the cipher text is fed into the decoder, which also consists of XOR gates. The decoder performs the decryption process, reconstructing the original message from the received cipher text.

4.1 Proposed Multilayer Multiplexer

The multiplexer is a device to route data from one of the several input lines to single output line depending on the status of the select lines. A 4:1 multiplexer is a device having four inputs lines, two select lines and one output line as demonstrated in the Fig. 10.

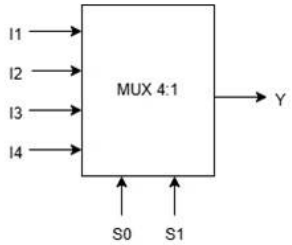


Fig 10. 4:1 Multiplexer Block Diagram

The truth table of 4:1 multiplexer is shown in the Table 1.

Table 1. 4:1 Multiplexer Truth Table

Select Lines		Output Y
S1	S0	
0	0	I1
0	1	I2
1	0	I3
1	1	I4

The multilayer designs have been proved to be more efficient in terms of device density as compared to their coplanar counterpart. Table 5 mentioned the comparative analysis of 4:1 multiplexer. It is also pertinent to mention here that the signal gets inverted when it is propagated from one layer to another layer. Accordingly, a multilayer 4:1 Multiplexer has been designed with the help of three 2:1 multiplexers, as shown in the Fig. 11. A total of 94 cells covering an area around 0.08 μm² have been used for the implementation of the proposed multiplexer. The clock latency of the circuit has come out to be 1.75.

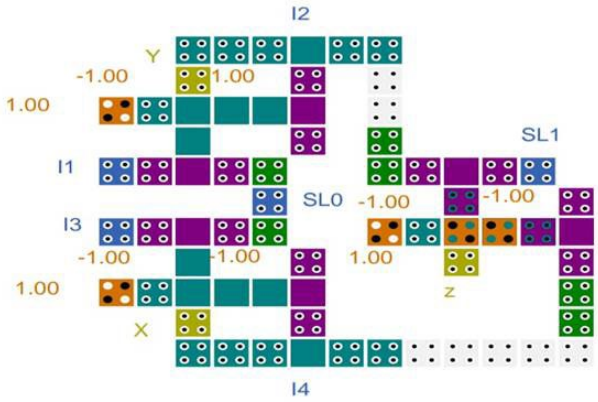
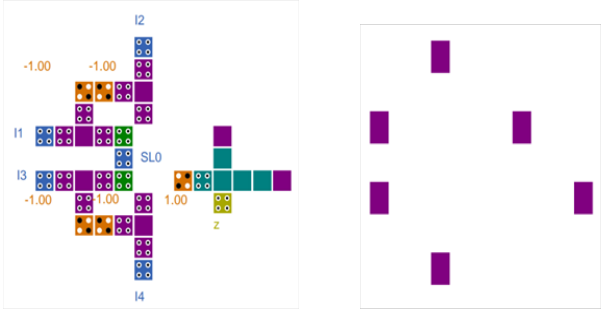
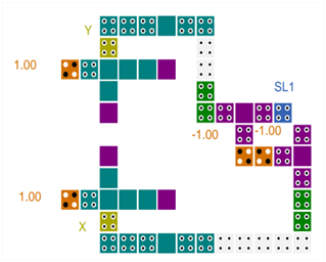


Fig 11. Proposed Multilayer 4:1 Multiplexer

The proposed multilayer design has been prepared with the use of three layers as shown in Fig 12.



(a) **(b)**



(c)

Fig 12. 4:1 Multiplexer Layered Structure **(a)** Layer 1 **(b)** Layer 2 **(c)** Layer 3

4.2 Proposed Multilayer Demultiplexer

The demultiplexer is a device that performs the reverse of the multiplexer i.e. the data is transferred from a single input line to one of the several output lines and the selection of the output line will depend on the select lines.

4.2.1 1:2 Demultiplexer

The block diagram of a 1:2 Demux is shown in the Fig. 13. The data from input line In will be transferred to output line X1 and X2, if the value of select line SL is '0' and '1', respectively.

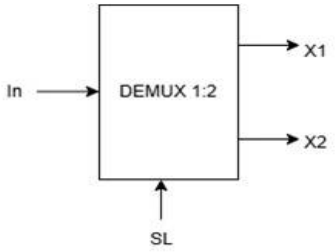


Fig 13. Block Diagram of 1:2 Demux

The truth table of the 1:2 Demux is illustrated in Table 2.

Table 2. Truth Table 1:2 Demux

Input		Output	
SL	In	X1	X2
0	0	0	0
0	1	1	0
1	0	0	0
1	1	0	1

The proposed 1:2 demultiplexer designed in QCA technology is shown in the Fig. 14. It took 19 cells to complete this 1:2 demultipler and Table 6 shows the comparative analysis of 1:2 demultiplexer.

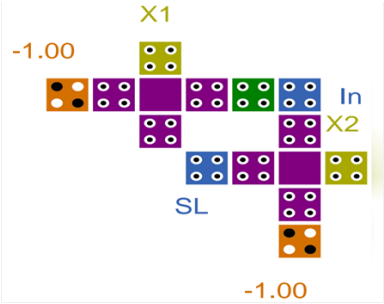


Fig 14. Proposed 1:2 Demultiplexer

4.2.2 1:4 Demultiplexer

1:4 demultiplexer is a device used to transfer the information from a single input line to one of the four output lines depending on the value of two select lines. The block diagram of 1:4 Demultiplexer is demonstrated in Fig. 15.

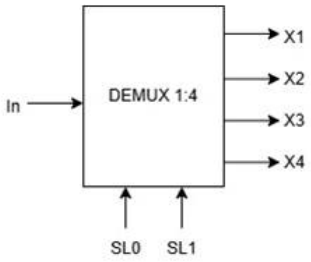


Fig 15. 1:4 Demultiplexer Block Diagram

The working of 1:4 demultiplexer is explained through the truth table in Table 3.

Table 3. Truth Table of 1:4 DeMux

Input			Output			
SL1	SL0	In	X1	X2	X3	X4
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

Three 1:2 demultiplexers are utilized to construct a 1:4 demultiplexer in three layers. The proposed 1:4 demultiplexer is shown in Fig. 16. The comparative analysis of 1:4 demultiplexer is shown in Table 7.

Two 1:2 demultiplexers are designed in 1st layer and the outputs Y1 & Y2 of these two demultiplexers are connected to the third 1:2 demultiplexer in third layer that results in outputs X1, X2, X3 and X4, as shown in Fig. 16. The circuit has been constructed with 92 QCA cells. The design utilizes 1.5 clock phases and occupies an area of 0.11 um^2.

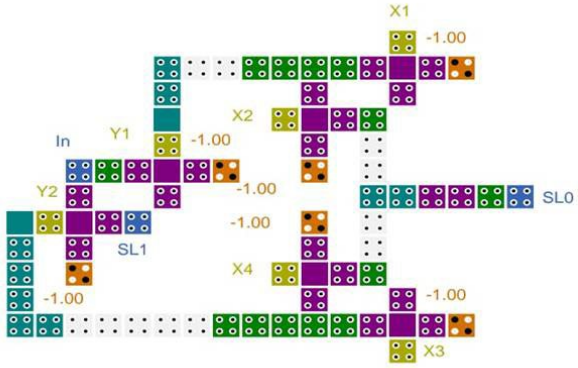
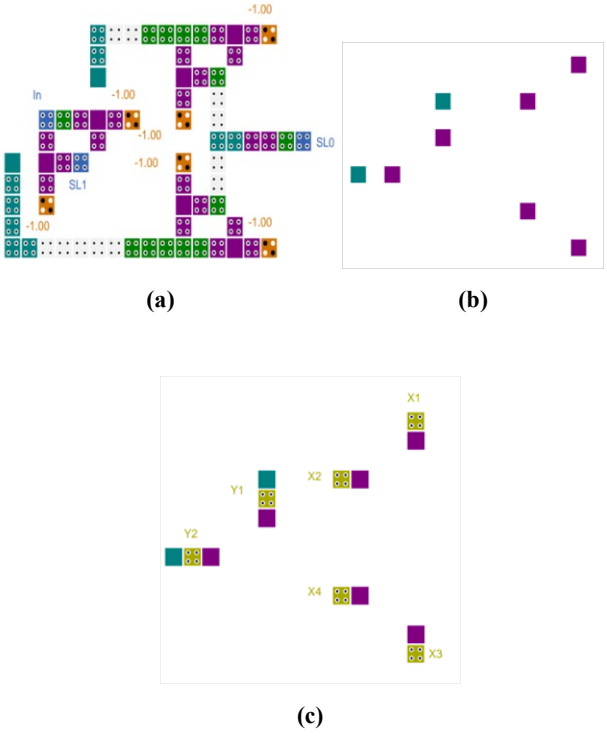


Fig 16. Multilayer 1:4 Demultiplexer

The proposed multilayer design has been prepared with the use of three layers as shown in Fig. 17.



(a) **(b)**

(c)

Fig 17. Proposed 1:4 Demultiplexer Layered Structure (**a**) Layer 1 (**b**) Layer 2 (**c**) Layer 3

4.3 Proposed Multilayer Cryptographic Nano communication circuit

The block diagram and schematic diagram of the cryptographic architecture is shown in the Fig. 18. The input data is first encrypted with the help of encoder and the encrypted data is sent to the recipient through the channel. Table 8 discusses the comparative analysis with the exiting nanorouters. The data is eventually received by the receiver after having the decryption process at the receiver side. To complete this whole cryptographic

circuit using the proposed multiplexer and demultiplexer it took 501 quantum cells. The QCA architecture of the cryptographic nano communication is shown in Fig. 19. The complexity of the proposed cryptographic architecture and its components is discussed in Table 10.

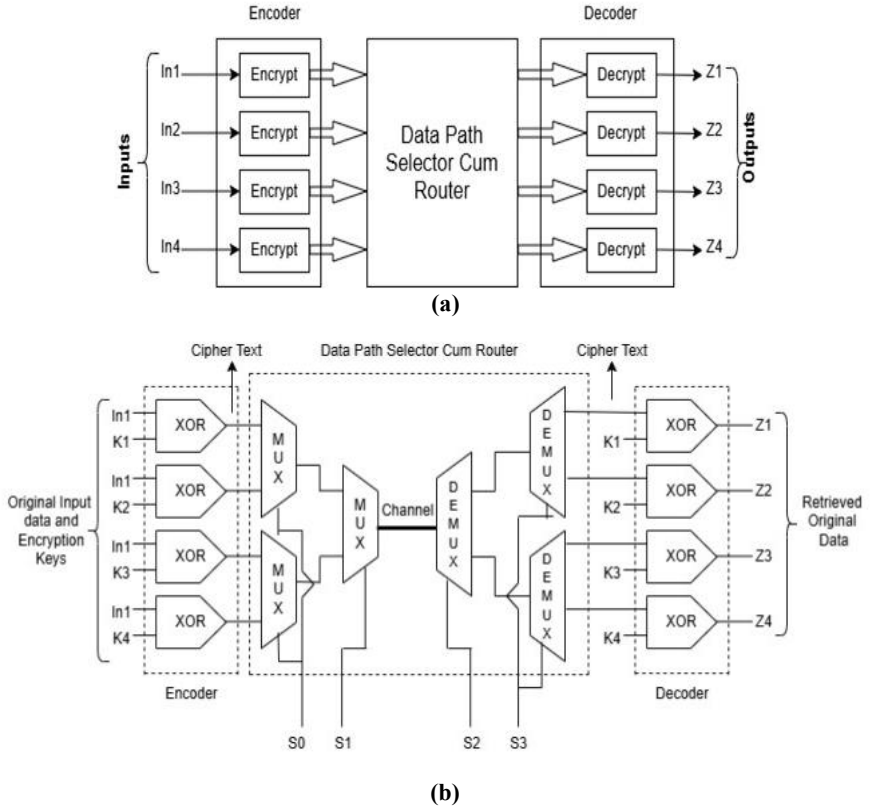


Fig 18. Cryptographic Encoder Decoder **(a)** Block Diagram **(b)** Schematic Diagram

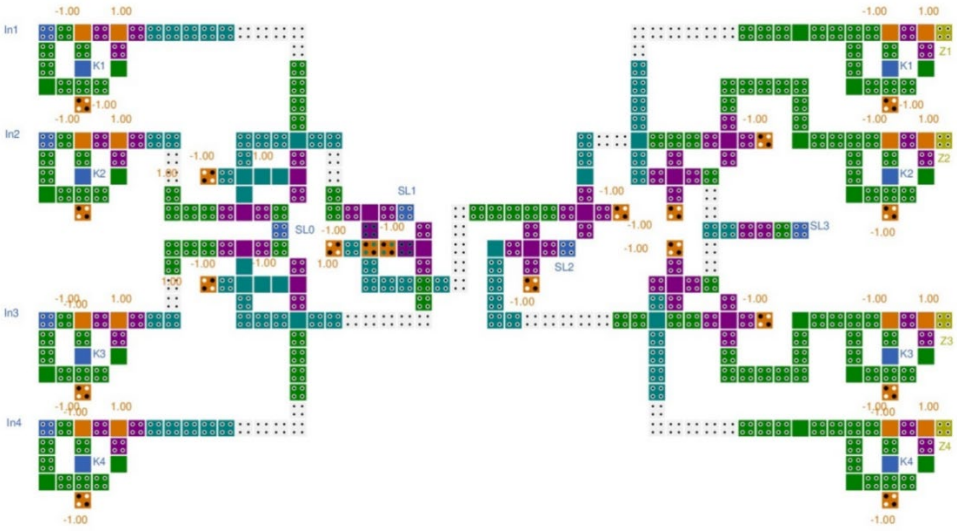


Fig 19. Proposed Cryptographic Nanocommunication Circuit

5 Simulation Results and Discussion

The QCADesigner 2.0.3 tool [11] has been used to check the simulation results for the suggested designs. This simulation is done using the bistable approximation engine of the QCA Designer 2.0.3 tool. The simulation parameters of the bistable approximation engine are shown in Table 4.

The simulation waveforms for the 4:1 multiplexer are shown in Fig 20. The Inputs I1 & I2 are applied to first 2:1 multiplexer and inputs I3 & I4are applied to second 2:1 multiplexer. The outputs X and Y of these both 2:1 multiplexers are further applied to the inputs of third 2:1 multiplexer resulting final output Y. SL0 and SL1 are the select lines for this multiplexer circuit. The truthness of working of this architecture is clear from the waveforms.

Table 4. Simulation parameter of the bistable approximation engine

Parameters	Value
Cell size	18 nm
Number of samples	12800
Convergence tolerance	0.0010
Radius of effect	65 nm
Relative permittivity	12.90
Clock high	9.80e-022
Clock low	3.80e-023
Clock amplitude factor	2.00
Layer separation	11.50
Max iteration per sample	100

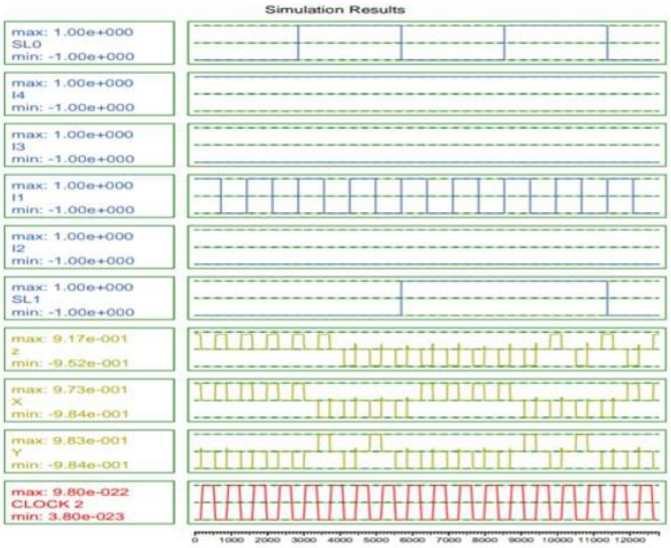


Fig 20. Multiplexer Waveforms

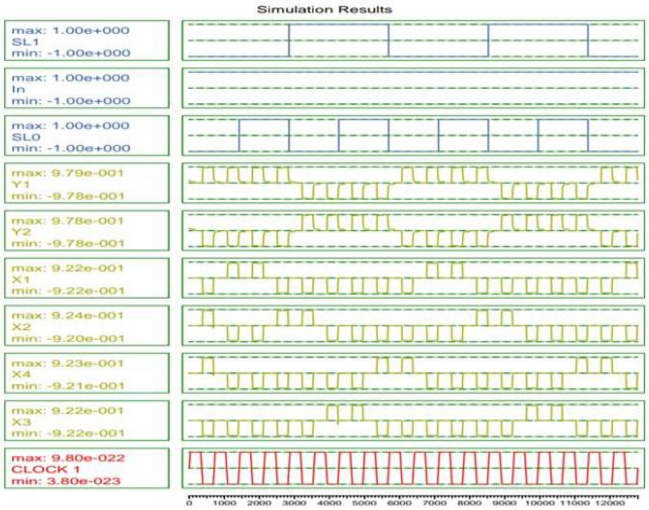


Fig 21. Demultiplexer Waveforms

The simulation results of 1:4 demultiplexer are shown in Fig. 21. The circuit takes 1.5clock cycles to produce the final output.

The following parameters are the key factors for the analysis of the QCA circuit [27].

***Complexity*:** Complexity refers to the number of Quantum-dot Cellular Automata (QCA) cells used in the design. It is a key parameter in determining the efficiency of the circuit, as a lower number of cells typically results in reduced area and power consumption.
***Total Area*:** Total area represents the total rectangular space covered by the design. It is calculated based on the number of vertical and horizontal cells and the dimension of each cell. For example, if a design consists of 2 vertical cells and 2 horizontal cells, with each cell having a dimension of 18 nm × 18 nm, the total rectangular area is given by: $2\times2\times18\times18$ nm^2.
***Cell Area*:** Cell area is the total space occupied by the quantum cells within the design. It is calculated as the product of complexity (i.e., the number of QCA cells) and the area of a single cell: 18 nm × 18 nm.
***Area Usage*:** Area usage is a measure of how efficiently the design utilizes the total available area. It is calculated as $\frac{\text{cell area}}{\text{total area}} \times 100\ \%$.

***Cost*:** Cost is an important performance metric that takes into accounts both area and latency. It is defined as the product of the total area and the square of the latency.
***Latency*:** Latency, also referred to as the delay of the circuit, is the number of clock cycles required by a signal for its propagation from the input to the output. It directly influences the performance and efficiency of the QCA circuit, with lower latency indicating faster operation.

Table 5. Comparative analysis of 4:1 multiplexer

Reference	Number of cells	Area (um^2)	Latency (clock cycles)
[20]	215	0.25	1.50
[21]	166	0.27	1.00
[22]	107	0.17	1.25
[23]	107	0.15	1.00
[19]	135	0.20	1.75
Proposed	94	0.08	1.75

Table 6. Comparative analysis of 1:2 demultiplexer

Reference	Number of cells	Area (um^2)	Latency (clock cycles)
[24]	21	0.03	0.50
[25]	21	0.017	0.50
[26]	27	0.04	0.50
[27]	21	0.02	0.50
[28]	32	0.026	0.50
Proposed	19	0.03	0.75

Table 7. Comparative analysis of 1:4 demultiplexer

Reference	Number of cell	Area (um^2)	Latency (clock cycles)
[24]	187	0.18	1.75
[25]	140	0.10	1
[29]	149	0.21	2
[30]	125	0.15	1.25
[26]	188	0.22	1
[19]	150	0.18	1.75
Proposed	92	0.11	1.5

Table 8. Comparative analysis with existing nano routers

Reference	Number of cells	Area (um^2)	Latency (clock cycles)
[32]	419	0.54	3.00
[29]	4026	13.81	12
[19]	293	0.53	3.75
Proposed	267	0.35	4.25

The cost of the proposed circuits is demonstrated in Table 9.

Table 9. Cost of the proposed QCA circuit

Circuit Components	Circuit Cost
4:1 Mux	0.245
1:2 Demux	0.017
1:4 Demux	0.247
Full circuit	19.05

Table 10. Complexity of the proposed Cryptographic architecture and its Components

QCA Circuit	Cell count	Total area (um^2)	Cell area (um^2)	Area usage (%)	Latency (clock cycles)
4:1 Mux	94	0.08	0.03	37.50	1.75
1:2 Demux	19	0.03	0.006	20	0.75
1:4 Demux	92	0.11	0.029	26.36	1.5
Cryptographic architecture	501	0.63	0.162	25.71	5.5

The comparative analysis of the existing cryptographic architectures is illustrated in Table 11.

Table 11. Comparative analysis of the existing cryptographic architectures

Reference	Cell Count	Total Area (um^2)	Cell Area (um^2)	Area usage (%)	Latency (Clock cycles)
[19]	581	1.14	0.188	16.5	5.50
Proposed	501	0.63	0.162	25.71	5.50

6 Conclusion

The proposed 4:1 multiplexer and 1:4 demultiplexer are used to construct a cryptographic nano communication circuit. The designs have been proposed in three layers that enhances its efficiency. The working of the designed structures i.e. cryptographic nano communication circuit and its components have been verified with the help of the tool QCA Designer 2.0.3. The proposed structures have also been compared with their existing counterparts. The circuits have been found to be more efficient in terms of area, energy and speed as compared to the previous designed architectures.

Conflict of Interest

The author declares no conflict of interest.

Author Contributions

Paramjeet.: Idea & Conceptualization, Research & Investigation, Data Curation, Analysis, Methodology, Software simulation and Original Draft Preparation. **Saptarshi Gupta:** Supervision, Verification and Revise & Editing. **Rupali Singh:** Supervision, Verification, Revise & Editing, Analysis, Methodology, Software and Simulation.

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Declaration of generative AI and AI-assisted technologies

The author(s) declare that no generative AI or AI-assisted technologies were used in the writing process of this manuscript.

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Biographies

Mr. Paramjeet. received his B.Tech. degree from Doon Valley Institute of Engineering and Technology, Karnal, Haryana in 2005 and M.Tech. degree from University Institute of Engineering and Technology, Kurukshetra University, Kurukshetra, Haryana in 2007. He has worked as Assistant Director at All India Council for Technical Education (AICTE), New Delhi, India. Currently, he is working as Lecturer at Govt. Polytechnic, Nilokheri and also working at the Disbursing Centre for PMS scheme for Technical Education Haryana. His research area includes Quantum dot cellular automata and Nano-circuits.

Dr. Saptarshi Gupta received his Ph.D. in Antenna Design from Noida International University, Gautam Budh Nagar, India, in 2020. From 2010 to 2013, he worked as a Lecturer in the Department of Electronics and Communication Engineering at All Nations University, Koforidua, Ghana, West Africa. Currently, he is working as an Associate Professor in the Department of Electronics and Communication Engineering at SRM Institute of Science and Technology, Delhi NCR Campus, Ghaziabad, U.P., India. His research interests include Embedded Systems, Antenna Theory, and IoT Design.

Dr. Rupali Singh received her PhD from SRM Institute of Science and Technology, Chennai. India. Currently she is working as an Associate Professor & Head in Electronics and Communication Engineering, SRM Institute of Science and Technology, Delhi NCR Campus, Ghaziabad, U.P., India. She has a vast experience of 22 years in the field of Teaching and Research. Her research area includes reversible logic circuits, Quantum dot cellular automata, and Nano-circuits. Currently, one scholar is awarded with PhD degree and 5 are pursuing PhD under her supervision

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