Iranian Journal of Electrical and Electronic Engineering

Journal Homepage: ijeee.iust.ac.ir

High Gain Hybrid DC-DC Topology Combining Switched -Inductor and Switched-Capacitor Techniques for PV Applications

Seyed Moein Mortezaie *, Mohammad Sarvi **(C.A.)

Abstract: This paper proposes a transformerless, non-isolated high-gain DC–DC conversion stage intended for interfacing photovoltaic (PV) sources. The topology uses a hybrid leg arrangement in which inductor-based switching cells are combined with a symmetrically arranged capacitor switching network forming three identical branches. These branches share the input power and collectively provide a large step-up ratio while maintaining balanced branch currents. The converter operates with continuously flowing inductor currents, and an analytical model is developed to obtain closed-form relations for voltage gain, semiconductor stresses, and design equations for the main passive components. Guidelines are provided for selecting inductors, capacitors, and device ratings under ripple constraints, resonant concerns, and safe operating limits. To validate the analysis, a 250-W implementation is examined using a detailed switching model in MATLAB/Simulink. The results show stable steady-state waveforms over a broad range of duty-cycle combinations and indicate that semiconductor voltage stress remains well below the output level, enabling the use of fast, low-voltage-rated switches and yielding good efficiency. The dual-duty modulation strategy improves adaptability to variations in PV irradiance and load by allowing flexible gain control through coordinated adjustment of duty cycles.

Keywords: Transformerless Converter, Enhanced voltage conversion, Switched-Inductor-Switched Capacitor Topology, Photovoltaic Systems

1 Introduction

The rapid penetration of photovoltaic (PV) generation into modern power networks has sharpened the demand for step-up converter that simultaneously offer high efficiency, compact realization, and dependable operation. Because a single PV module typically provides only tens of volts about (20-60)V-the native output is unsuitable for direct connection to high-voltage DC links or inverter front-ends. Consequently, DC-DC converters with strong step-up capability are required to bridge the voltage gap and ensure effective energy transfer in standalone and grid-interactive PV systems [1, 2]. Isolated solutions can furnish the needed gain, yet the transformer brings added bulk and cost as well as parasitic effects (e.g., leakage-inductance-induced transients) that penalize performance [1, 3]. Conversely, classical non-isolated boost converters must push the duty ratio toward unity to reach comparable levels, which aggravates device stress, raises conduction loss, and undermines dynamic behavior—factors that limit their practicality in PV conditioning stages [1, 4].

Expectations for PV converters now extend beyond sheer voltage amplification. Long-term reliability, dense integration, and consistent operation under changing irradiance and load are equally important. Rooftop and distributed settings impose tight constraints on volume, thermal handling, and serviceability. under such conditions, high efficiency, moderated device stress, and restrained component count are key to achieving power

Iranian Journal of Electrical & Electronic Engineering, YYYY.
Paper first received DD MONTH YYYY and accepted DD MONTH YYYY.
* The author is with the Department of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran.
E-mail: moein_mortezaie80@elec.iust.ac.ir.
** The author is with the Department of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran.
E-mails: msarvi@iust.ac.ir.
Corresponding Author: Mohammad Sarvi.

density and thermal stability [4]. Maintaining regulated output despite environmental variability is also essential. Prior studies indicate that avoiding extreme duty operation while containing switch stress contributes materially to sustained efficiency and robust dynamics [5]. These considerations motivate fresh high-gain topologies that pair strong voltage elevation with practical integration in PV plants. Fig 1 summarizes the intended function of the proposed topology: it processes the inherently fluctuating PV input and elevates it to a regulated high-DC output suitable for interfacing with DC loads, battery-charging stages, or grid-connected converters.

A range of non-isolated families has been explored to satisfy these needs, each with clear advantages but also non-trivial trade-offs. Switched-capacitor (SC) schemes are attractive for their transformerless nature and theoretical gain; however, variants relying on autotransformers or resonant partitions may suffer from narrow soft-switching windows and elevated device stress under imperfect control [6, 7]. Multi-stage SC and regenerative boost arrangements can introduce sizable input-current pulsation, EMI concerns, and added control burden, complicating PV deployment [8, 9]. Hybrid realizations that combine switched-inductor, switched-capacitor, or multiplier cells target higher gain with moderated stresses, yet often at the expense of numerous passives, increased conduction loss, and heightened design complexity [10, 11]; sensitivity to inductor mismatch may trigger resonant over voltages and uneven stress sharing [12], and some variants still impose high voltage on particular switches or require intricate multi-mode coordination [11, 13]. Coupled-inductor converters deliver large gain with continuous input current, but they entail multiple current paths and sophisticated gating [14, 15]; leakage inductance can produce voltage spikes that demand careful turns-ratio tuning and clamps [14, 16], and the magnetics footprint and capacitor sizing elevate cost while diode stress may remain significant [15, 17]. Interleaved arrangements improve input-current quality and reduce ripple; nonetheless, architectures in [18-21] marry interleaving with multiplier cells or phase-shifted control require precise current sharing and synchronization, increasing control effort and part count. Z-source and quasi-Z-source networks enable wide-range boost through impedance structures. despite enhancements with coupled inductors and multipliers [22, 23], practical issues such as complex design, start-up inrush, and overshoot under PV dynamics persist [24]. Finally, cascaded cells offer very high gain and distributed MPPT, beneficial under partial shading [25, 26], but incur larger size, cumulative losses, and potential fault propagation across stages [27].

Recent advancements in high-gain resonant and hybrid DC–DC converters demonstrate diverse architectural strategies to extend voltage-gain capability in renewable-energy systems. A reconfigurable LLC/LLC-C dual-output resonant converter offers wide gain control and soft switching but suffers from high switching frequency, auxiliary detection complexity and moderate efficiency [28]. A hybrid switched-inductor/switched-capacitor structure with dual duty cycles achieves flexible gain and robustness against PV variations, yet relies on a customized high-leakage transformer, large HV capacitors, light-input test conditions, and high resonant current peaks [29]. A bidirectional topology integrating a quadratic boost cell, SC network, and zero-current-ripple unit provides enhanced gain and ripple suppression, though its multi-element structure raises cost and complexity, with limited dynamic analysis and low-power experimental validation [30]. A current-fed quasi-resonant design delivers ZVS/ZCS operation, high gain, and low input ripple but lacks small-signal modeling, transient studies, non-ideal analysis, and high-power scalability assessment [31]. A single-switch topology using a three-winding transformer and Cockcroft–Walton multiplier achieves ultra-high gain with low device stress, yet introduces magnetic complexity, capacitor-balancing sensitivity, ESR-dependent gain degradation, and limited scalability due to its single-switch nature [32]. Another high-gain converter employing a three-winding coupled inductor provides continuous input current and reasonable gain, but suffers from complex magnetic design, high component count, and increased implementation cost due to multi-path operation, reducing its practicality [33]. A single-switch multistage topology offers acceptable gain, but its passive components grow significantly with stage number, all devices face full output voltage stress, the operating region is tightly constrained by $nD < 1$, and parasitic degrade real gain while transient capacitor currents introduce additional stress [34].

Among the high-gain converters proposed for PV applications, both structures show important practical limitations despite providing reasonable voltage boosting. The first design faces noticeable conduction losses due to multiple diode paths, and its single switch is subjected to output-level voltage stress, restricting device selection and limiting scalability for higher-power PV systems [35]. In the second design, although some voltage stresses are alleviated, switch S1 still endures considerable current stress that complicates thermal management, while its multi-stage charging mechanism increases sensitivity to parameter variations and reduces robustness under fast irradiance or load fluctuations [36].

In this paper, a high step-up, non-isolated topology tailored for photovoltaic operation is introduced. The structure combines inductor-based switching cells with a capacitor switching network, forming a hybrid configuration for enhanced voltage boosting in a symmetric three-leg layout. Each leg integrates an inductor, an active switch, and its associated capacitor

path, yielding a compact structure with balanced energy transfer. The converter operates in the continuous conduction region and adopts a dual-duty modulation approach that enables flexible regulation of the output voltage. Owing to its optimized component count, the topology attains a substantial voltage amplification while mitigating device stress and maintaining high energy-conversion efficiency, making it well suited for compact photovoltaic systems.

In contrast to previous designs built around SL and SC switching networks that often feature partially asymmetric energy-transfer structures or rely on single-duty modulation, the proposed topology introduces a new hybrid configuration that uniquely integrates three switched-inductor and three switched-capacitor branches within a single symmetrical structure. This innovative hybrid arrangement enables the simultaneous operation of all SL and SC branches, forming a unified architecture that coordinates multiple energy paths for enhanced voltage boosting and balanced power flow. The converter employs simple MOSFET switches, and due to the inherent symmetry of the proposed structure, no reverse or recirculating currents appear in any branch. This eliminates the need for unidirectional devices such as RB-IGBTs or series MOSFET–diode combinations and naturally prevents turn-off voltage spikes across the switches, while maintaining full functionality and reliable operation. It establishes coordinated energy transfer among inductive and capacitive stages, achieving parallel charging and series discharging of the energy-storage elements during different switching intervals. This configuration significantly enhances the voltage-boosting capability—achieving a higher conversion ratio compared with conventional hybrid SL–SC converters—while maintaining balanced operation, where all semiconductor devices experience uniform voltage stress below the output voltage. Furthermore, a dual-duty modulation scheme provides independent control of the energy-sharing intervals, enabling flexible gain adjustment without extreme duty ratios. Although the converter features a symmetrical hybrid structure, it maintains a minimal number of components, resulting in a compact and efficient topology. As a result, the converter achieves high step-up gain, reduced component stress, and improved efficiency without using transformer coupling, voltage multipliers, or magnetically coupled elements. The proposed configuration therefore represents a new structural advancement over existing SL–SC architectures in terms of gain enhancement, stress balancing, and topological compactness.

The organization of this paper is as follows: Section 2 presents the circuit architecture and explains the operation throughout its three switching intervals; Section 3 derives the conversion ratio via volt-second balance and presents passive-component sizing; Section 4 evaluates semiconductor stresses and estimates efficiency under non-idealities; Section 5 benchmarks the proposed topology against recent step-up designs; Section 6 presents the simulation setup and key waveforms, followed by a concise interpretive discussion of the observed results that highlights the main advantages of the proposed converter; and Section 7 concludes the paper with the main merits and application outlook.

2 Functional Mechanism and Architectural Modes of the Presented Converter

The proposed topology is a high step-up, non-isolated DC–DC structure tailored for photovoltaic applications. Rather than relying on magnetic coupling or transformer-based solutions, the circuit combines switched-inductor paths with a coordinated switched-capacitor arrangement to achieve a pronounced increase in output voltage. The converter operates under continuous conduction conditions, maintaining a steady inductor current flow while limiting the voltage stress imposed on its active switching components. Its control strategy utilizes four power switches with a straightforward gating sequence that facilitates efficient operation.

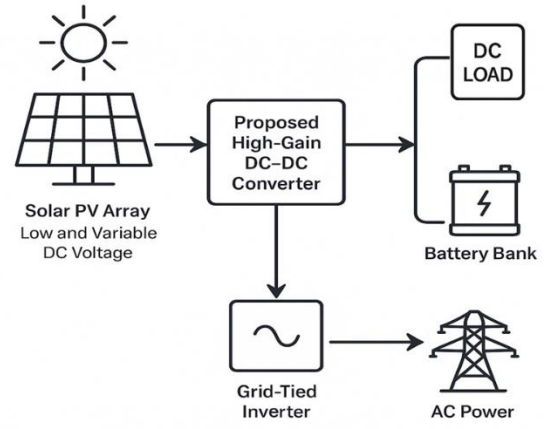


Fig 1. Overall PV setup and the location of the introduced high step-up DC–DC converter within the system.

The dual-duty modulation scheme adopted in the proposed converter does not introduce any additional hardware complexity, as both duty cycles D_1 and D_2 are generated by standard PWM channels available in common microcontrollers. The two control signals operate with fixed alignment and do not require phase shifting or interleaving, which minimizes their sensitivity to timing mismatch and dead-time variations. As a result, the implementation remains straightforward and does not demand specialized control hardware, making the dual-duty scheme practical for photovoltaic applications with minimal additional circuitry.

As illustrated in Figure 2**,** the power circuit consists of four active switches (S_1 to S_4)**,** four diodes **(**D_0 to D_3)**,**

three inductive elements **(**L_1 to L_3**),** and four capacitors **(**C_0 to C_3**),** systematically organized into three identical functional branches, each featuring a switched-inductor branch, while the combination of diodes and capacitors establishes the voltage-lift mechanism. During each switching period, the coordinated switching of the transistors dictates the charging of inductors and the redistribution of charge among capacitors. This multi-interval energy exchange process enables efficient voltage boosting, as represented in Figures 3 to 5, and the associated control waveforms are displayed in Figure 6**.**

For analytical simplicity, idealized conditions are assumed—voltage drops across diodes, conduction resistance of switches, and the minor ohmic losses introduced by the passive elements are excluded from consideration to keep the analysis concise. The inductors L_1**,** L_2**,** and L_3 are assumed to have equal inductance and identical magnetic characteristics, sharing equal inductance and magnetic properties; thus, they are modeled uniformly as $L_1 = L_2 = L_3 = L$, which simplifies the derivation of steady-state relations and voltage-gain equations.

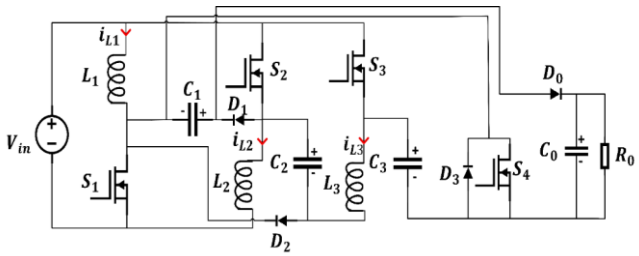


Fig 2. Circuit of the transformerless boost stage employing a hybrid switched-inductor and switched-capacitor network.

Mode 1 (D_1.T):

At the start of the switching period, S_1 to S_3 are commanded to conduct, while S_4 is held non-conducting. With Vin applied, the three inductors L_1 to L_3 are magnetized in parallel, accumulating energy in their cores. In this subinterval, D_1 to D_3 conduct and establish charging paths so that C_1 to C_3 draw charge directly from the source. The output diode D0 remains in a blocking state, electrically isolating the load from the input network; consequently, the output capacitor CO alone supplies the load current during Mode 1. Because L_1 to L_3 are identical and experience the same applied voltage, their current and voltage trajectories are equivalent and can be described by a single set of expressions. The corresponding equivalent network for this mode is shown in Figure 3.

$$V_{L_1} = V_{L_2} = V_{L_3} = V_{in} \tag{1}$$

$$V_{C_1} = V_{C_2} = V_{C_3} = V_{in} \tag{2}$$

$$V_{D_1} = V_{D_2} = V_{D_3} = 0 \tag{3}$$

$$V_{D_0} = V_{in} - V_O \tag{4}$$

$$V_{S_1} = V_{S_2} = V_{S_3} = V_{S_4} = 0 \tag{5}$$

$$i_{C_O} = \frac{-V_O}{R} \tag{6}$$

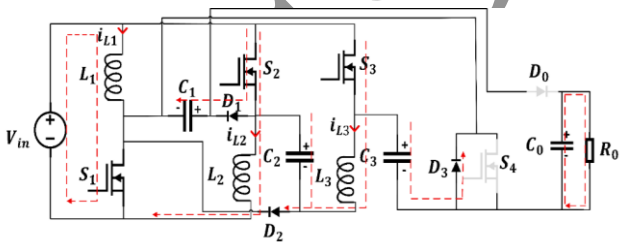


Fig 3. Mode-1 operating portrait: reduced network highlighting the active energy-transfer paths in the first interval.

Mode 2 (D_2.T):

During the second operating phase, S_1 to S_3 remain non-conducting, whereas S_4 is switched ON. In this configuration, every diode (D_0 to D_3) is reverse-biased, preventing current from circulating through their respective branches. The input supply together with C_2 and C_3 establishes a series charging loop, generating an additive voltage that re-energizes the inductors L_1 to L_3. Throughout this subinterval, the load is fed by the output capacitor CO, which maintains seamless energy transfer, ensuring an uninterrupted power transfer. The electrical equivalent corresponding to this stage of operation is illustrated in Figure 4.

$$V_{L_1} = V_{L_2} = V_{L_3} = V_{in} \tag{7}$$

$$V_{C_1} = V_{C_2} = V_{C_3} = V_{in} \tag{8}$$

$$V_{D_1} = V_{D_2} = V_{D_3} = 0 \tag{9}$$

$$V_{D_0} = V_{in} - V_O \tag{10}$$

$$V_{S_1} = V_{S_2} = V_{S_3} = V_{S_4} = 0 \tag{11}$$

$$i_{C_O} = \frac{-V_O}{R} \tag{12}$$

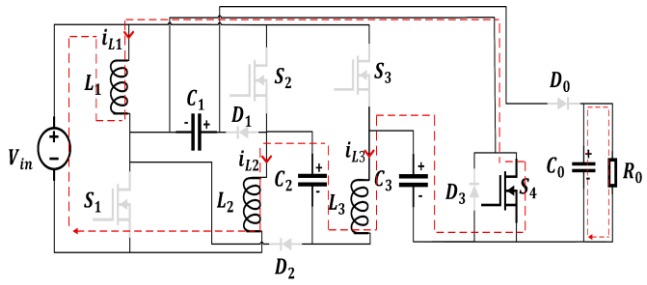


Fig 4. Mode-2 conduction map showing voltage and current routing during the S_4-on interval.

Mode III to Output Energy Transfer Phase [(1-D_1-D_2)T]:

In the closing phase of the switching cycle, all switches (S_1 to S_4) remain turned off. Under these circumstances, the input source, along with inductors L_1 to L_3 and capacitors C_1 to C_3, forms a series conduction path that directly feeds the output stage. At this instant, the voltage induced across the inductors drops below the output level, which reverses their polarity and releases the magnetic energy accumulated in earlier intervals. In this operating state, diodes D_1 to D_3 stay reverse-biased, while the output diode D_O conducts and transfers the combined energy to the load.

Throughout this interval, energy drawn from the source and the reactive elements is routed to the load via the output capacitor C_O, which is simultaneously replenished to maintain the required output voltage. The equivalent representation of this operating mode is illustrated in Figure 5.

$$V_{L_1} = V_{L_2} = V_{L_3} = \frac{4V_{in} - V_O}{3} \tag{13}$$

$$V_{C_1} = V_{C_2} = V_{C_3} = V_{in} \tag{14}$$

$$V_{D_1} = V_{D_2} = \frac{2V_{in} - 2V_O}{3} \tag{15}$$

$$V_{D_3} = V_{in} - V_O \tag{16}$$

$$V_{D_0} = 0 \tag{17}$$

$$V_{S_1} = V_{S_2} = \frac{V_O - V_{in}}{3} \tag{18}$$

$$V_{S_3} = \frac{2V_O - 2V_{in}}{3} \tag{19}$$

$$V_{S_4} = V_O - V_{in} \tag{20}$$

$$i_{C_O} = i_{L_1} - \frac{V_O}{R_O} \tag{21}$$

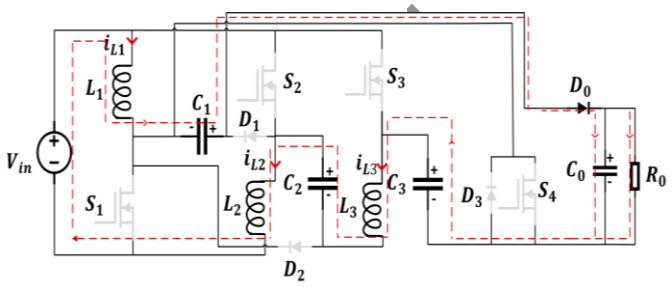


Fig 5. Mode 3 representation — inductive and capacitive release stage feeding the output through D_0.

3. Modeling Approach and Design Procedure of the Introduced Converter

In this section, an analytical framework is developed to interpret the electrical characteristics of the proposed converter. The expression for the voltage gain is obtained through a fundamental balance of inductor volt–second quantities, and the discussion continues with the design and sizing guidelines for the main passive components. Moreover, the voltage stresses imposed on all semiconductor devices, including both switching transistors and rectifying diodes, are examined to aid in selecting suitable components and to ensure reliable and efficient operation under various load and environmental conditions.

3.1 Calculation of the voltage gain

Since the net voltage across an inductor must average to zero over a full switching period, and each inductor experiences identical voltage profiles in all operating states, the analysis can be simplified by examining a single representative inductor.

Accordingly, the following expressions, (22) and (23), are derived:

$$\int_0^{D_1 T} V_L \, dt + \int_0^{D_2 T} V_L dt + \int_0^{(1-D_1-D_2)T} V_L \, dt = 0 \tag{22}$$

Utilizing the inductor voltage expression obtained in the preceding section, the following relation holds:

$$\frac{V_O}{V_{in}} = \frac{4 - D_1 - D_2}{1 - D_1 - D_2} \tag{23}$$

The dependence of the voltage gain on the duty ratios D_1 and D_2 is depicted in Figure 7. The voltage gain expression given in (23) is plotted in Figure 7 with D_2 held constant and D_1 varying. Due to the symmetry of the gain formula, the same behavior is observed when D_1 and D_2 are interchanged. As the plot indicates, increasing either D_1 or D_2 results in a proportional rise in the output voltage gain, following the relationship defined in (23).

3.2 Design of Input Inductors

For this topology, inductors L_1 to L_3 are dimensioned such that the converter sustains CCM operation during all switching intervals. With this design choice, the inductor current avoids dropping to zero, which supports a consistent energy flow between stages. The required inductance value is influenced by several parameters, including input voltage, duty ratio, switching frequency, and allowable inductor current ripple. A higher inductance minimizes current ripple but increases size and cost, whereas a lower value results in reduced efficiency and higher current stress. Therefore, the chosen inductance should represent an optimal balance between these design constraints.
Ampere-second law:

$$\int_0^{D_1T} i_{c_O}\, dt + \int_0^{D_2T} i_{c_O}\, dt + \int_0^{(1-D_1-D_2)T} i_{c_O}\, dt = 0 \tag{24}$$

Utilizing the capacitor current relationships obtained across the different switching modes in (6, 12, 21), the following equation can be concluded:

$$i_L = \frac{V_O}{R_O(1 - D_1 - D_2)} \tag{25}$$

The magnitude of current ripple in the inductor can be evaluated as:

$$\Delta i_L = \frac{(D_1 + D_2) \times V_{in}}{L \times f} \tag{26}$$

The inductor current waveform in Figure 6 allows calculation of its average current, as expressed in the following equation:

$$I_L = i_{Lmin} + \frac{\Delta i_L}{2} \tag{27}$$

In boundary condition ($i_{L,\min} = 0$):

$$I_L = \frac{\Delta i_L}{2} \tag{28}$$

Therefore:

$$L_{min} = \frac{R_O(1 - D_1 - D_2)(D_1 + D_2)V_{in}}{2 \times f \times V_O} \tag{29}$$

3.3 Output Capacitor Design

The output capacitor C_O is chosen to ensure a stable DC output and to restrict voltage ripple within acceptable limits, even under variations in load demand. Its required value is influenced by parameter capacitor alone supplies the output power. In the proposed topology, energy reaches the load directly only in the third operating interval, whereas in the first two intervals, the capacitor discharges to maintain uninterrupted load current. Consequently, C_0must provide adequate energy-storage capability to sustain continuous output delivery. Accordingly, C_0 must possess sufficient energy-storage capacity to support the load during these discharge intervals without producing excessive voltage variation. Considering these operational features, the minimum capacitance value can be established from the corresponding design relations.

$$\Delta V_C = \frac{1}{Co} \int_0^{(D_1+D_2)T} (i_o) dt \tag{30}$$

$$Co = \frac{(D_1 + D_2) \times (I_o)}{\Delta V_C \times f} \tag{31}$$

3.4 Voltage Stress Analysis

In this part of the paper, the voltage stresses applied to the converter's switches and diodes are examined. The stress levels obtained for each semiconductor device are listed in Table 1, where the maximum values are emphasized for clarity. Owing to the converter's symmetric configuration and its three-mode operating sequence, the voltage applied to both the active switches and passive rectifiers remains substantially restricted. As reported in Table 1, no device is subjected to a stress value higher than the output voltage. This characteristic permits the use of MOSFETs and diodes with relatively low voltage ratings, which naturally offer reduced conduction losses and faster transition behavior, thereby enhancing efficiency and improving thermal performance. Consequently, the proposed design offers a compact and cost-effective solution well suited for practical power-conversion applications.

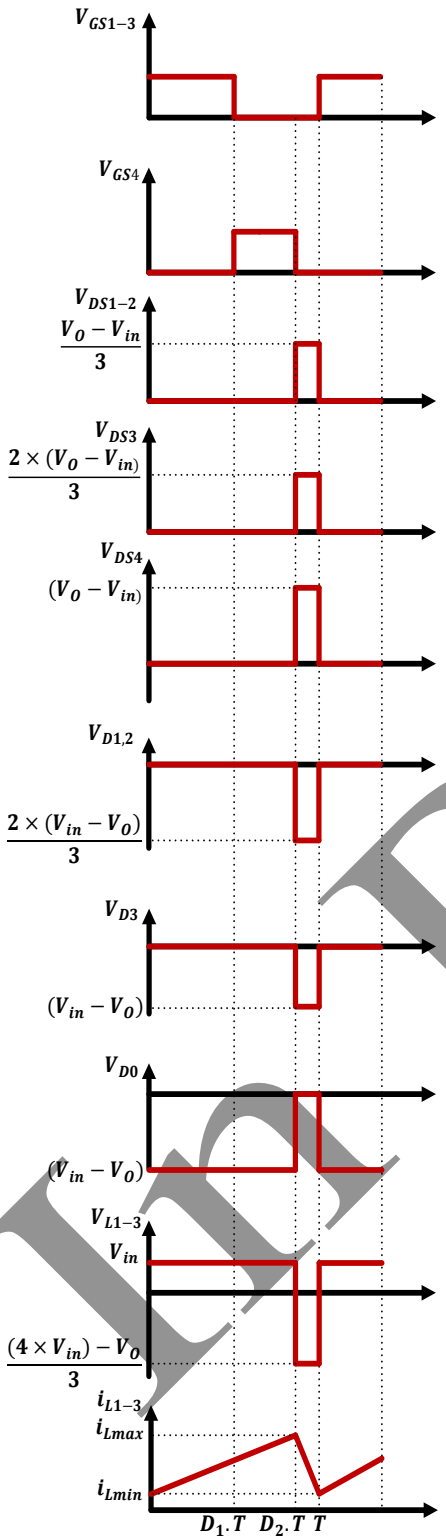


Fig 6. One-cycle switching traces of the proposed high-gain stage.

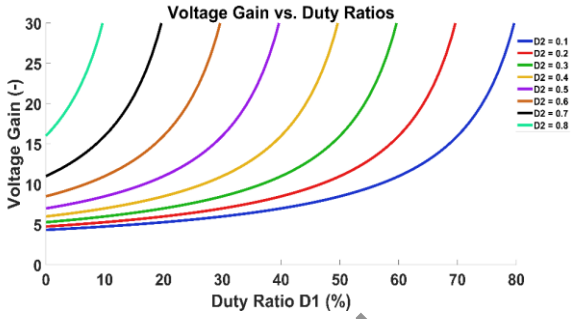


Fig 7. Voltage-gain surface versus the duty-ratio pair (D_1, D_2).

4. Efficiency analysis

The converter's behavior—especially in terms of efficiency and dynamic performance—is affected by the non-idealities inherently present in the power stage. To represent these imperfections, an equivalent circuit incorporating the key resistive elements and voltage-drop components is depicted in Figure 7. In this model, r_{L_1}, r_{L_2} and r_{L_3} denote the series winding resistances of inductors L_1, L_2, and L_3. Similarly, the capacitive losses are included through the series resistances associated with C_O and the intermediate capacitors C_1, C_2, and C_3. The conduction resistance and forward-voltage characteristics of the diodes are also accounted for in order to capture the converter's practical behavior under non-ideal operating conditions. D_0 to D_3 are expressed as $r_{D_{0-3}}$ and $V_{D_{0-3}}$, respectively, whereas the on-state drain-source resistances of switches S_1 to S_4 are symbolized by $r_{DS_{1-4}}$.

For analytical convenience, the voltage drops caused by these ESRs are neglected in the capacitor current evaluation, since their impact on the steady-state characteristics is negligible. The combined influence of parasitic resistances and device non-idealities on converter performance is analyzed using the equivalent representation shown in Figure 8**.**

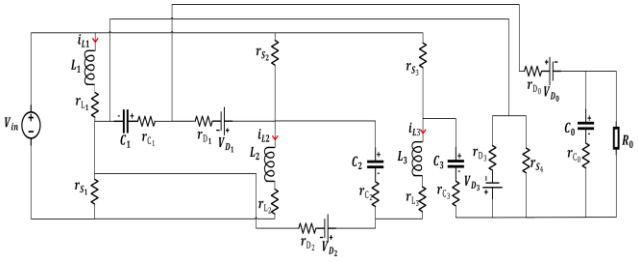


Fig 7. Expanded nonideal framework used for efficiency evaluation, including device drops and ESR paths.

Table 1. Voltage endurance limits of switching and rectifying devices within the proposed converter topology.

	MODE 1	MODE 2	MODE 3
V_{S_1}	0	0	$\frac{\mathbf{V_O - V_{in}}}{\mathbf{3}}$
V_{S_2}	0	0	$\frac{\mathbf{V_O - V_{in}}}{\mathbf{3}}$
V_{S_3}	0	0	$\frac{\mathbf{2V_O - 2V_{in}}}{\mathbf{3}}$
V_{S_4}	0	0	$\mathbf{V_O - V_{in}}$
V_{D_1}	0	0	$\frac{\mathbf{2V_{in} - 2V_O}}{\mathbf{3}}$
V_{D_2}	0	0	$\frac{\mathbf{2V_{in} - 2V_O}}{\mathbf{3}}$
V_{D_3}	0	0	$\mathbf{V_{in} - V_O}$
V_{D_0}	$\mathbf{V_{in} - V_O}$	$\mathbf{V_{in} - V_O}$	0

Mode 1:

During this operating interval, switches S_1 to S_3 remain active, while S_4 is turned off. Under these conditions, diodes D_1 to D_3 become conductive and establish a path for current flow, whereas the output

Table 1. Voltage endurance limits of switching and rectifying devices within the proposed converter topology.

diode D_O stays reverse-biased and blocks conduction. Over the time span D_1T_s, the average value of the output-capacitor current i_{CO} and the corresponding inductor voltage V_L can be determined using the analytical expressions presented in equations (32) and (33).

$$i_{c_O} = -\frac{V_O}{R} \tag{32}$$

$$V_{L_1}{}^{I} = V_{in} - i_{L_1}\left(r_{L_1} + r_{S_1}\right) \tag{33}$$

Mode 2:

During this stage, switch $\mathbf{S_4}$ is turned ON, while S_1 to $\mathbf{S_3}$ remain OFF. In this operating condition, all diodes (D_0 to D_3**)** are in the reverse-biased state, thereby preventing current conduction through their respective paths. Over the time interval $[D_2.T_s]$, Equations (34) and (35) provide the analytical expressions from which the mean current through the output capacitor and the corresponding inductor voltage V_L can be extracted.

$$i_{c_O} = -\frac{V_O}{R} \tag{34}$$

$$V_{L_1}{}^{II} = \frac{V_{in} + V_{C_2} + V_{C_3} - i_{L_1}\left(r_{L_1} + r_{S_4} + r_{C_3} + r_{L_3} + r_{C_2} + r_{L_2}\right)}{3} \tag{35}$$

Mode 3:

In the third operating interval, all switching devices S_1 to S_4 remain inactive. During this stage, the output diode D_O turns on and provides a conduction path that delivers energy to the load, while diodes D_1 to D_3 stay reverse-biased, blocking any current flow. Throughout the time span $[(1\text{-}D_1\text{-}D_2).T_S]$, the average current drawn from the output capacitor i_{CO} and the corresponding inductor voltage V_L can be determined using the analytical relations introduced in equations (36) and (37).

$$i_{C_O} = i_{L_1} - \frac{V_O}{R_O} \tag{36}$$

$$V_{L_1}{}^{III} = \frac{V_{in} + V_{C_1} + V_{C_2} + V_{C_3} - V_O - V_{D_0} - i_{L_1}\left(r_{eq}\right)}{3} \tag{37}$$

Where:

$$r_{eq} = r_{L_1} + r_{C_1} + r_{D_0} + r_{C_0} + r_{C_3} + r_{L_3} + r_{C_2} + r_{L_2} \tag{38}$$

The Ampere-second balance remains valid in this mode and is expressed by equation (25). Using the volt-second balance principle, we have:

$$\int_0^{D_1T_s} VL_1^{I}\,dt + \int_0^{D_2T_s} VL_1^{II}\,dt + \int_0^{(1-D_1-D_2)T_s} VL_1^{III}\,dt = 0 \tag{39}$$

By simplifying equation (39), the expression for the output voltage is obtained as:

$$V_o = \frac{\gamma V_i + \frac{D_2}{3}(V_{C_3} + V_{C_2}) + \frac{1-D_1-D_2}{3}(V_{C_3} + V_{C_2} + V_{C_1})}{\alpha + \beta} \tag{40}$$

where the parameters defined for simplification are given as follows:

$$\alpha = \frac{D_1}{R_o(1-D_1-D_2)}(r_{L_1}+r_{S_1})+ \frac{D_2}{3R_o(1-D_1-D_2)}\times (r_{L_1}+r_{S_4}+r_{C_3}+r_{L_3}+r_{C_2}+r_{L_2}) \quad (41)$$

$$\beta = \frac{1-D_1-D_2}{3}+\frac{1-D_1-D_2}{3R_o(1-D_1-D_2)}(r_{eq}) \quad (42)$$

$$\gamma = D_1+\frac{D_2}{3}+\frac{1-D_1-D_2}{3} \quad (43)$$

Equations (44) to (46) provide the analytical formulation for both the input and output power involved in the operation of the proposed converter.

$$P_{in} = 3V_{in}i_{L_1}D_1+V_{in}i_{L_1}D_2+V_{in}i_{L_1}(1-D_1-D_2) \quad (44)$$

Substituting (25) in (44), the input power is as given in (45):

$$P_{in} = \frac{V_{in}V_O(2D_1+1)}{R_O(1-D_1-D_2)} \quad (45)$$

$$P_O = \frac{V_O^2}{R_O} = \frac{1}{R_o}\left(\frac{\gamma V_i+\delta}{\alpha+\beta}\right)^2 \quad (46)$$

Where:

$$\delta = \frac{D_2}{3}(V_{C_3}+V_{C_2})+\frac{1-D_1-D_2}{3}(V_{C_3}+V_{C_2}+V_{C_1}) \quad (47)$$

Using the relationships defined in equations (40), (45), and (46), the converter's efficiency—evaluated under the assumption that only conduction losses are present—can be determined from equation (48).

$$\eta = \frac{P_o}{P_{in}} = \frac{\frac{1}{R_o}\left(\frac{\gamma V_i+\delta}{\alpha+\beta}\right)^2}{\frac{V_{in}V_o(2D_1+1)}{R_o(1-D_1-D_2)}} \quad (48)$$

Under practical operating conditions, where switching losses P_{sw} are taken into account, the converter's output power is expressed by equation (49).

$$P_O = \frac{V_o^2}{R_O} - P_{SW_{total}} \quad (49)$$

Switching losses for power switches:

$$P_{SW_{Power\ Switches}} = V_{DS}\times i_{DS}\times(t_r+t_f)\times f_S \quad (50)$$

Switching losses for diodes:

$$P_{SW_{Diodes}} = V_D\times i_D\times(t_r+t_f)\times f_S \quad (51)$$

Accordingly, considering all four active switches and four diodes, the cumulative switching power dissipation can be formulated as follows:

$$P_{SW_{Total}} = (4\times V_D\times i_D\times(t_r+t_f)\times f_{SW})+ (4\times V_{DS}\times i_{DS}\times(t_r+t_f)\times f_{SW}) \quad (52)$$

In this formulation, V_{DS} denotes the voltage across the drain-source terminals of each switching element, while i_{DS} corresponds to the associated drain current. Here, V_D represents the diode's conduction voltage, and i_D denotes the current flowing through it. The operating frequency of the converter is specified by f_S, while t_r and t_f characterize the turn-on and turn-off transition durations of the semiconductor switches. Based on these parameters, the final expression describing the converter's overall efficiency is formulated as follows:

$$\eta = \frac{Po}{P_{in}} = \frac{\frac{V_o^2}{R_O}-P_{SW_{Total}}}{\frac{V_{in}V_O(2D_1+1)}{R_O(1-D_1-D_2)}} \quad (53)$$

To evaluate the converter efficiency with higher accuracy, the individual power losses of each semiconductor and passive component were calculated separately. For this purpose, the RMS value of the current flowing through each device was first derived based on the mode-by-mode current waveforms of the proposed topology. These RMS currents form the basis for determining conduction losses, switching losses, and passive component dissipation.

The general expression for computing the RMS value of any periodic current waveform is given in (54), and based

on this formulation, the RMS currents and corresponding loss terms for all components are obtained as follows:

$$i_{\text{rms}} = \sqrt{\frac{1}{T}\int_0^T \left[i(t)\right]^2 dt} \tag{54}$$

Since all inductors in the proposed topology exhibit identical current waveforms due to the symmetrical three-branch structure, their RMS currents and corresponding conduction losses are equal. Therefore, the RMS inductor current and its associated loss can be expressed as follows:

$$I_{L,\text{rms}} = I_o \left(\frac{4 - D_1 - D_2}{1 - D_1 - D_2}\right)\sqrt{1 - \frac{8D_1}{9}} \tag{55}$$

$$P_L = r_L . I^2_{L,\text{rms}} \tag{56}$$

In this section, only conduction losses are considered, while the switching losses are separately included in Equations (50)–(53).

For switch S_1:

$$i_{S_1,\text{rms}} = I_o \frac{4 - D_1 - D_2}{1 - D_1 - D_2}\sqrt{D_1} \tag{57}$$

$$P_{S_1} = r_{DS_1} . I^2_{S_1,\text{rms}} \tag{58}$$

Since switches S_2, S_3 operate under identical switching conditions in the symmetrical hybrid structure, they exhibit the same current waveform. Therefore, their RMS currents and conduction losses are equal and can be expressed as follows.

$$I_{S_{2-3},\text{rms}} = I_o \frac{4 - D_1 - D_2}{3(1 - D_1 - D_2)}\sqrt{D_1} \tag{59}$$

$$P_{S_2 - S_3} = r_{DS} . I^2_{S_1 - S_3,\text{rms}} \tag{60}$$

For switch S_4:

$$I_{S4,\text{rms}} = I_o \frac{4 - D_1 - D_2}{1 - D_1 - D_2}\sqrt{D_2 - D_1} \tag{61}$$

$$P_{S_4} = r_{DS} . I^2_{S_4,\text{rms}} \tag{62}$$

Since diodes D_1 to D_3 appear only in the capacitor-branch paths and conduct exclusively during Mode 1, their conduction intervals are short and the associated current levels are relatively small. As a result, their power dissipation is negligible, and the losses of these diodes are therefore omitted from the analysis.

For the output diode:

$$I_{D_0,\text{rms}} = I_o \frac{4 - D_1 - D_2}{1 - D_1 - D_2}\sqrt{1 - D_2} \tag{63}$$

$$I_{D0,\text{avg}} = I_o \left(4 - D_1 - D_2\right) \tag{64}$$

$$P_{D_0} = r_{D0} . I^2_{D_0,\text{rms}} + V_{D0(ON)} I_{D0avg}{}^2 \tag{65}$$

For capacitor C_1:

$$P_{C_1} = r_{C_1} . I^2_{C_1,\text{rms}} \tag{66}$$

Since capacitors C_2 and C_3 have identical behavior, we have:

$$I_{C_2,C_3,\text{rms}} = I_o \frac{4 - D_1 - D_2}{1 - D_1 - D_2}\sqrt{1 - D_1} \tag{67}$$

$$P_{C_{2,3}} = r_{C_{2,3}} . I^2_{C_{2,3},\text{rms}} \tag{68}$$

For the output capacitor:

$$I_{C_o,\text{rms}} = \sqrt{I_o^2 D_2 + (I_{in} - I_o)^2 (1 - D_2)} \tag{69}$$

$$P_{C_0} = r_{C_0} . I^2_{C_0,\text{rms}} \tag{70}$$

The total power loss is calculates in (71).

$$P_{Losstotal} = P_{L_1} + P_{L_2} + P_{L_3} + P_{S_1} + P_{S_2} + P_{S_3} + P_{S_4} + P_{D_0} + P_{C_1} + P_{C_2} + P_{C_3} + P_{C_0} \tag{71}$$

5. Performance Comparison

To highlight the merits of the proposed topology, its principal performance indices were evaluated and compared with those of several recently introduced high-gain converters of similar class. Table 2 presents a consolidated comparison covering device-stress characteristics, achievable step-up capability, and the overall component requirement. For consistency, the maximum voltage stress measured on both the switching

and rectifying devices was selected as the reference metric. The analysis indicates that the introduced topology delivers a noticeably higher voltage conversion ratio than earlier designs. This enhancement is achieved without relying on magnetic coupling or transformer-assisted gain techniques; rather, it arises from the coordinated action of the combined switched-inductor and switched-capacitor branches. In addition, all semiconductor devices experience voltage stresses that remain safely below the output level, allowing the adoption of components with reduced voltage ratings and superior dynamic performance. Among the dual-duty-controlled converters examined for comparison, D_2 was fixed at 0.35, and the voltage-gain variation was plotted with respect to D_1. The comparative gain curves for several representative high-gain topologies are illustrated in Figure 9.

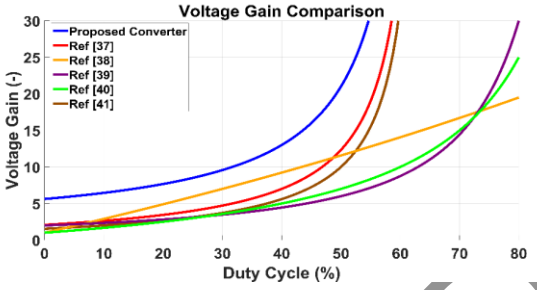


Fig 8. Comparative gain plots for five transformerless high-gain converter architectures.

6. Simulation Outcomes and Interpretive Analysis

To substantiate the analytical results, the introduced high-gain converter was modeled and evaluated within a MATLAB/Simulink framework using realistic component values. The simulation setup was configured to deliver 250 W from a 15-V input while sustaining an output voltage of 315 V. The complete list of component specifications is provided in Table 3, The steady-state waveforms and the transient behavior obtained from the simulation are shown in Figures 10–14. The converter efficiency curve over the 100 to 300 W power range is presented in Figure 15.

For a more practical assessment, non-ideal effects—such as parasitic resistances and conduction losses—were incorporated into the simulation environment. These imperfections introduced minor deviations from the idealized results, thereby reproducing actual converter behavior with higher fidelity. The simulation outcomes verify that the proposed circuit provides a substantial voltage step-up ratio, maintains stable operation, and limits voltage stress across all semiconductor elements, confirming its effectiveness and high efficiency for photovoltaic power-conditioning applications. Furthermore, inspection of the simulated waveforms revealed smooth switching transitions, where no noticeable voltage surges or unintended circulating current paths emerged during operation.

The simulated stress levels, current waveforms, and switching waveforms confirm that the proposed topology maintains stable operation and acceptable device loading across a wide range of duty-cycle combinations (D_1, D_2), demonstrating that with proper selection of semiconductor ratings, inductor specifications, and capacitor ripple capability, the design can be efficiently scaled to higher power levels.

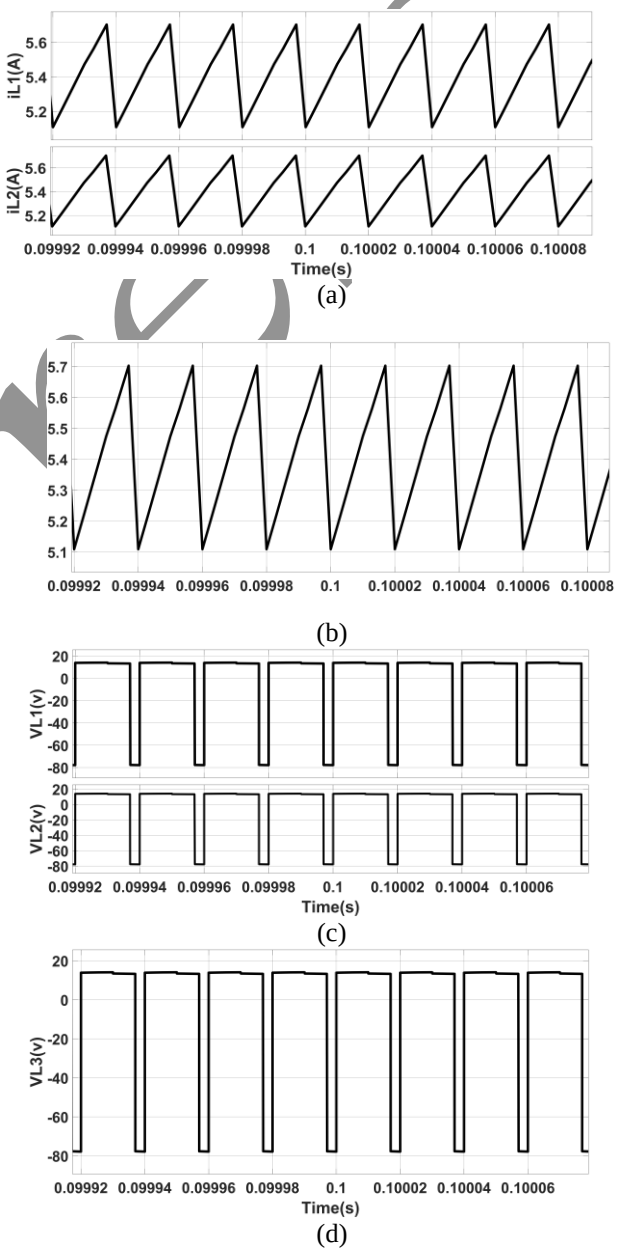


Fig 9. Inductor waveforms under steady switching: (a) $i_{L1\text{-}2}$, (b) i_{L3}, (c) $V_{L1\text{-}2}$, (d) V_{L3}.

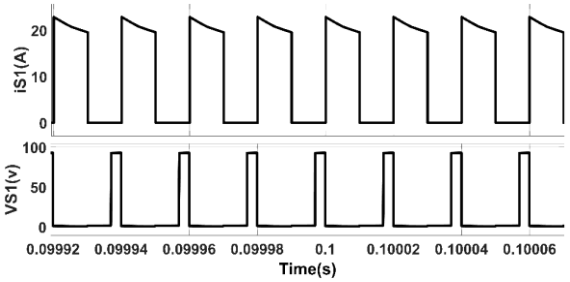
Table 2. Comparative assessment of the proposed converter against state-of-the-art transformerless high-gain DC-DC designs.

Parameter	Proposed Converter	Ref [37]	Ref [38]	Ref [39]	Ref [40]	Ref [41]
Total number of components	15	10	16	10	17	8
Switches	4	3	2	1	3	3
Diodes	4	4	8	4	7	2
Capacitors	3	1	2	3	1	1
Inductors	3	2	4	2	6	2
Voltage gain (CCM)	$\frac{(4 - D_1 - D_2)}{(1 - D_1 - D_2)}$	$\frac{(1 + D_1 + D_2)}{(1 - D_1 - D_2)}$	$\frac{1+18.25D}{1-0.25D}$	$\frac{2-D}{(1-D)^2}$	$\frac{1+5D}{1-D}$	$\frac{1+D_1}{1-D_1-D_2}$
Max. voltage stress on switches	$V_O - V_{in}$	V_O	$0.575V_O$	$\frac{V_{in}}{(1-D)^2}$	$\frac{2V_{in}+V_0}{3}$	V_O
Max. voltage stress across diodes	$V_{in} - V_O$	V_O	$0.531V_O$	$\frac{V_{in}}{(1-D)^2}$	$V_O + V_{in}$	$V_{in} + V_O$
Efficiency(%)	94-95	93.7	93	91.2	95.6	93.6
Cost	Low	Medium-High	High	Low-Medium	Medium	Low–Medium
Power density	High	Medium	Medium–High	High	Medium–High	High
Component Loss	Low	High	Low–Medium	Medium	Medium–Low	Medium

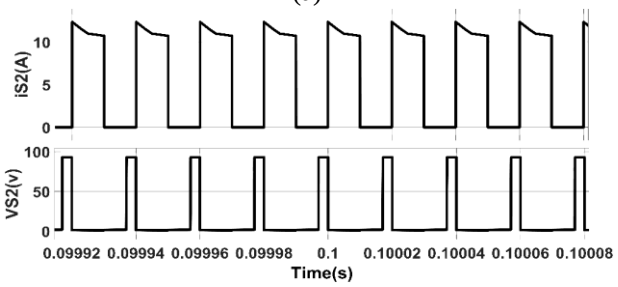
Table 3. Core design parameters and operational characteristics adopted for the proposed high step-up converter.

Parameter	Value	Parameter	Value
V_{in}	15 V	C_1, C_2, C_3	100 µF
V_O	315 V	C_0	100 µF
P_O	250 W	S_1 to S_4	IPP410N30NAKSA1
f_s	50 kHz	D_1 to D_3, D_0	STTH15L06
L_1, L_2, L_3	400 µH	Duty cycles	D_1 =0.5, D_2 = 0.35

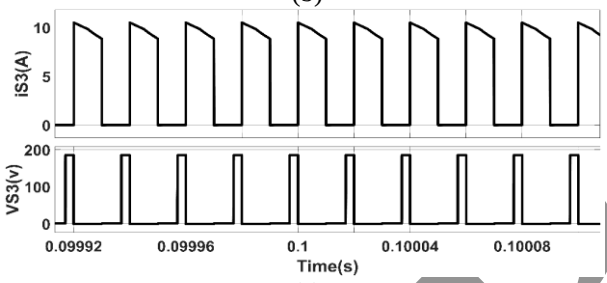
The steady-state waveforms presented in Figures 9–14 directly confirm the key operational benefits of the proposed topology. As seen in Figures 9(a)–9(d), the inductor voltages during the first two intervals are clamped to the input voltage V_{in}, while the inductor currents remain continuous and ripple-controlled. This behaviour stems from the hybrid switched-inductor/switched-capacitor arrangement and explains the high voltage gain without extreme duty cycles. Importantly, the switch and diode waveforms in Figures 10 and 11 exhibit perfectly clean transitions; no ringing, no voltage overshoot, and no high-frequency oscillations appear throughout the entire switching period. The absence of parasitic ringing eliminates the need for snubber circuits and greatly reduces electromagnetic interference (EMI), which is a recognized problem in many competing high-gain designs that suffer from leakage inductance or resonant current spikes.



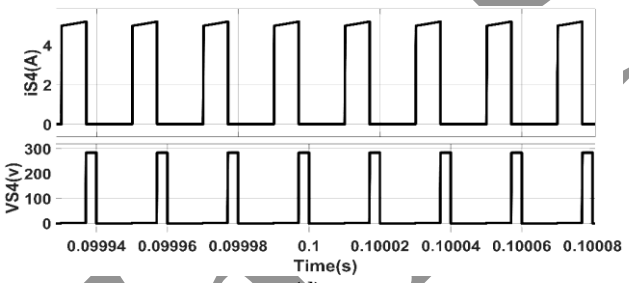
(a)



(b)

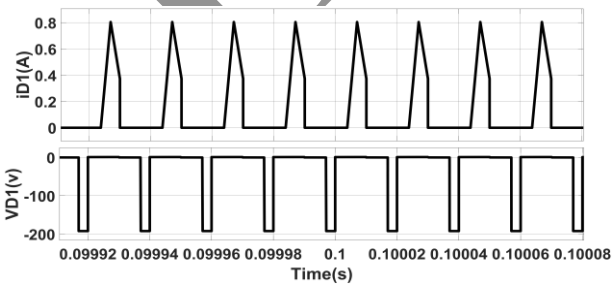


(c)

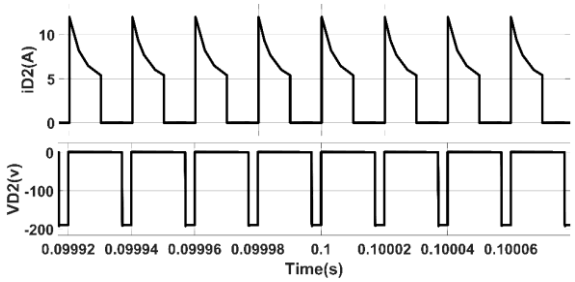


(d)

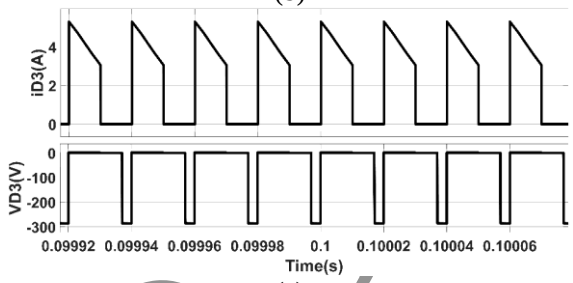
Fig 10. Switch voltages and currents over one period: (a) S_1, (b) S_2, (c) S_3, (d) S_4.



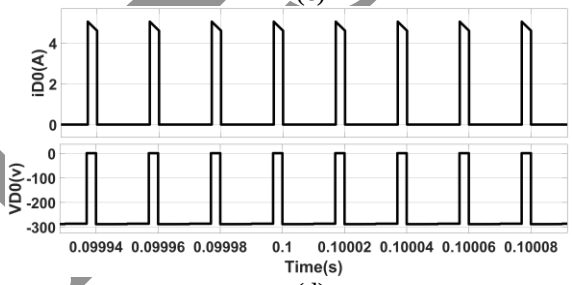
(a)



(b)

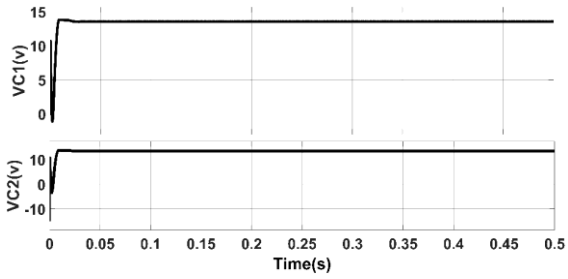


(c)

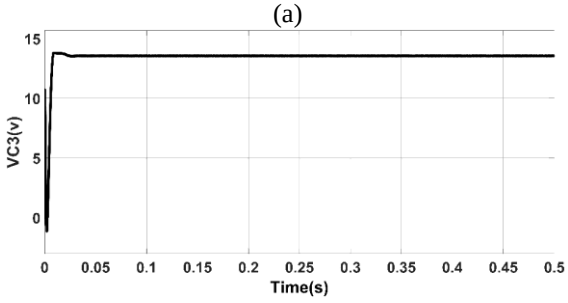


(d)

Fig 11. Diode operating states across successive cycles. (a) D_1, (b) D_2, (c) D_3, (d) D_0.



(a)



(b)

Fig 12. Voltages of Capacitors. (a) Voltages of C_1, C_2 and (b) Voltage of C_3 during steady operation.

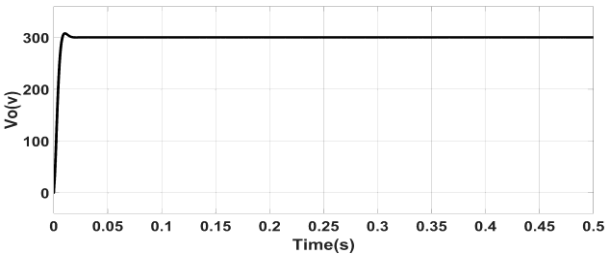


Fig 13. Output-voltage record at rated load.

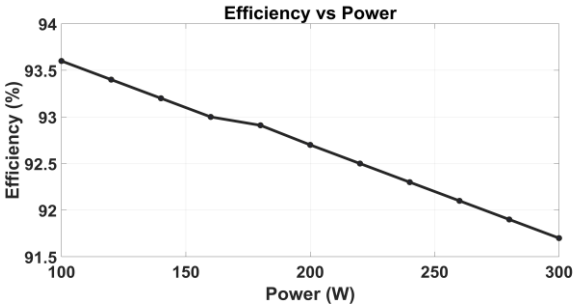


Fig 14. Simulated conversion efficiency as a function of delivered output power.

Figures 12 and 13 further show that all capacitor voltages are well balanced and that the output voltage settles at 315 V from a 15 V input with negligible steady-state error. Finally, Figure 14 demonstrates that the converter maintains 94–95 % efficiency over a 100–300 W load range, confirming that the clean switching and low device stress translate directly into practical energy savings.

8. Conclusion

In this study, a non-isolated high-gain DC–DC topology without a transformer is presented, developed specifically for photovoltaic applications. The architecture utilizes a hybrid energy-transfer mechanism that integrates switched-inductor paths with switched-capacitor stages in a symmetric three-branch layout, enabling a high step-up conversion ratio while preserving uniform current sharing among the branches. A detailed analytical investigation was carried out, including the converter's voltage-gain characteristics, efficiency performance, and the distribution of voltage stresses across all semiconductor devices. The system is designed to deliver a regulated 300-V output from a 15-V input at a power level of 250 W, operating entirely in continuous conduction mode (CCM). Simulation studies incorporating non-ideal component parameters confirm that the proposed converter sustains stable operation, high efficiency (94–95)% over a 100–300 W range), and consistent voltage boosting under realistic conditions. Moreover, the converter draws continuous, non-pulsating input current because the inductors never fully discharge, which reduces input capacitance and source-side ripple. All semiconductors experience uniformly low voltage stress—well below the output voltage—which simplifies device selection and improves reliability. The three identical branches naturally balance inductor currents without extra control loops, and the dual-duty modulation provides flexible gain adjustment using only standard PWM signals. The topology remains transformerless and magnetically uncoupled, avoiding leakage-inductance spikes, core saturation, and clamp circuits. With its compact structure, reduced component count compared to similar hybrid designs, and strong high-gain capability, the developed converter provides a robust, efficient, and EMI-compliant solution for photovoltaic and renewable-energy conversion systems.

References

[1] J. Ingilala and I. Vairavasundaram, "Investigation of high gain DC/DC converter for solar PV applications," *e-Prime - Advances in Electrical Engineering, Electronics and Energy*, vol. 5, 2023, doi: 10.1016/j.prime.2023.100264.

[2] K.-C. Tseng and C.-C. Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 3, pp. 1311–1319, March 2014 2014, doi: 10.1109/TIE.2013.2261036.

[3] V. F. Pires, A. Cordeiro, D. Foito, and J. F. A. Silva, "Dual Output and High Voltage Gain DC-DC Converter for PV and Fuel Cell Generators Connected to DC Bipolar Microgrids," *IEEE Access*, vol. 9, pp. 157124–157133, 2021, doi: 10.1109/access.2021.3122877.

[4] N. Tewari and V. T. Sreedevi, "A novel single switch dc-dc converter with high voltage gain capability for solar PV based power generation systems," *Solar Energy*, vol. 171, pp. 466–477, 2018, doi: 10.1016/j.solener.2018.06.081.

[5] B. Srinivas, R. Rao P, H. Nagendrappa, and B. Venkatesaperumal, "A Novel Cubic Boost Converter With Continuous Source Current for PV Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 12, pp. 5014–5018, 2024, doi: 10.1109/tcsii.2024.3434985.

[6] M. R. S. de Carvalho, E. A. O. Barbosa, F. Bradaschia, L. R. Limongi, and M. C. Cavalcanti, "Soft-Switching High Step-Up DC–DC Converter Based on Switched-Capacitor and Autotransformer Voltage Multiplier Cell for PV Systems," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 12, pp. 12886–12897, 2022, doi: 10.1109/tie.2022.3142432.

[7] S. Folmer and R. Stala, "DC-DC High Voltage Gain Switched Capacitor Converter With Multilevel Output Voltage and Zero-Voltage Switching," *IEEE Access*, vol. 9, pp. 129692–

129705, 2021, doi: 10.1109/access.2021.3111546.

[8] V. Karthikeyan, S. Kumaravel, and G. Gurukumar, "High Step-Up Gain DC–DC Converter With Switched Capacitor and Regenerative Boost Configuration for Solar PV Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 12, pp. 2022–2026, 2019, doi: 10.1109/tcsii.2019.2892144.

[9] R. Stala *et al.*, "High-Gain Switched-Capacitor DC-DC Converter With Low Count of Switches and Low Voltage Stress of Switches," *IEEE Access*, vol. 9, pp. 114267–114281, 2021, doi: 10.1109/access.2021.3104399.

[10] A. M. S. S. Andrade, L. Schuch, and M. L. da Silva Martins, "Analysis and Design of High-Efficiency Hybrid High Step-Up DC–DC Converter for Distributed PV Generation Systems," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3860–3868, 2019, doi: 10.1109/tie.2018.2840496.

[11] T. S. Bheemraj, Y. Anil Kumar, V. Karthikeyan, and S. Pragaspathy, "A Hybrid Structured High Step-Up DC–DC Converter for Integration of Energy Storage Systems in Military Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 4, pp. 1545–1549, 2023, doi: 10.1109/tcsii.2022.3225900.

[12] A. Andrade, T. Faistel, R. Guisso, and A. Toebe, "Hybrid High Voltage Gain Transformerless DC–DC Converter," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 3, pp. 2470–2479, 2022, doi: 10.1109/tie.2021.3066939.

[13] R. Rajesh, N. Prabaharan, and E. Hossain, "Design and Analysis of a New High Step-Up Converter Using Switched-Inductor-Capacitor Voltage Multiplier Cells for Photovoltaic Application," *IEEE Journal of the Electron Devices Society*, vol. 12, pp. 842–848, 2024, doi: 10.1109/jeds.2023.3337517.

[14] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti, and F. Blaabjerg, "High-Efficiency High Step-Up DC–DC Converter With Dual Coupled Inductors for Grid-Connected Photovoltaic Systems," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5967–5982, 2018, doi: 10.1109/tpel.2017.2746750.

[15] H. Liu, J. Wang, and Y. Ji, "A Novel High-Step-Up Coupled-Inductor DC–DC Converter With Reduced Power Device Voltage Stress," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1941–1948, 2019, doi: 10.1109/jestpe.2018.2868769.

[16] R. Rahimi, S. Habibi, P. Shamsi, and M. Ferdowsi, "A Three-Winding Coupled-Inductor-Based Dual-Switch High Step-Up DC–DC Converter for Photovoltaic Systems," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 3, no. 4, pp. 1106–1117, 2022, doi: 10.1109/jestie.2022.3151554.

[17] H. S. Gohari, S. Abbasian, N. A. Mardakheh, K. Abbaszadeh, and F. Blaabjerg, "Coupled Inductor-Based Current-Fed Ultra-High Step-Up DC-DC Converter Featuring Low Input Current Ripple," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 2, pp. 887–891, 2024, doi: 10.1109/tcsii.2022.3206231.

[18] M. Sarvi, R. Ebrahimnaz, and H. Zarei Zohdi, "A New High Gain DC–DC Converter for Solar System," *Journal of Solar Energy Research*, pp. 2115–2124, 2024, doi: 10.22059/jser.2025.382684.1468.

[19] R. Ebrahimnaz and M. Sarvi, "A new configuration of DC-DC converter with increased voltage gain for photovoltaic application," *International Journal of Electronics*, vol. 112, no. 11, pp. 2570–2590, 2025, doi: 10.1080/00207217.2025.2450744.

[20] R. Ebrahimnaza and M. Sarvi, "A Novel Interleaved DC–DC Converter with High Voltage Gain for Photovoltaic System Applications," *Journal of Solar Energy Research*, vol. 7, no. 2, pp. 1056–1066, 2022, doi: 10.22059/jser.2022.322284.1248.

[21] K. A. Singh, A. Prajapati, and K. Chaudhary, "High-Gain Compact Interleaved Boost Converter With Reduced Voltage Stress for PV Application," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 4, pp. 4763–4770, 2022, doi: 10.1109/jestpe.2021.3120802.

[22] A. Samadian *et al.*, "Analysis of High Step-Up Quasi-Z-Source-Based Converter With Low Input Current Ripple," *IEEE Open Journal of the Industrial Electronics Society*, vol. 5, pp. 632–650, 2024, doi: 10.1109/ojies.2024.3398250.

[23] A. Samadian, M. G. Marangalu, H. Tarzamni, S. H. Hosseini, M. Sabahi, and A. Mehrizi-Sani, "High Step-Up Common Grounded Switched Quasi Z-Source DC–DC Converter Using Coupled Inductor With Small Signal Analysis," *IEEE Access*, vol. 11, pp. 120516–120529, 2023, doi: 10.1109/access.2023.3327303.

[24] A. Torkan and M. Ehsani, "A Novel Nonisolated Z-Source DC–DC Converter for Photovoltaic Applications," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4574–4583, 2018, doi: 10.1109/tia.2018.2833821.

[25] A. A. A. Hafez, "Multi-level cascaded DC/DC converters for PV applications," *Alexandria Engineering Journal*, vol. 54, no. 4, pp. 1135–1146, 2015, doi: 10.1016/j.aej.2015.09.004.

[26] X. Hu, P. Ma, J. Wang, and G. Tan, "A Hybrid Cascaded DC–DC Boost Converter With Ripple Reduction and Large Conversion Ratio," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 761–770, 2020, doi: 10.1109/jestpe.2019.2895673.

[27] S. Xiong and S.-C. Tan, "Cascaded High-Voltage-Gain Bidirectional Switched-Capacitor DC–DC Converters for Distributed Energy Resources Applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1220–1231, 2017, doi: 10.1109/tpel.2016.2552380.

[28] R. M. Reddy and M. Das, "Reconfigurable Dual Output Resonant DC–DC Converter for Wide Output Voltage Applications," *IEEE Transactions on Transportation Electrification*, vol. 11, no. 1, pp. 1004–1014, 2025, doi: 10.1109/tte.2024.3399608.

[29] Y. Yue, G. Wang, and W. Guo, "A Wide-Input High Step-Up Resonant Converter With High-Ratio Transformer in High-Voltage Applications," *IEEE Transactions on Power Electronics*, vol. 40, no. 10, pp. 15583–15594, 2025, doi: 10.1109/tpel.2025.3579118.

[30] X. Hu, J. Jia, X. He, and Z. Xu, "An Extendable Transformer-Less Bidirectional DC–DC Converter With High Voltage Gain and Zero-Current Ripple," *IEEE Transactions on Power Electronics*, vol. 40, no. 3, pp. 4227–4243, 2025, doi: 10.1109/tpel.2024.3498320.

[31] Y. Wu, B. Xue, Y. Liu, M. Fu, and H. Wang, "Low Current Ripple High-Boost Ratio Resonant Converter for Vehicle-Integrated PV Modules," *IEEE Transactions on Power Electronics*, vol. 41, no. 1, pp. 983–993, 2026, doi: 10.1109/tpel.2025.3590880.

[32] S. Hasanpour and T. Nouri, "New Soft-Switched Three-Winding Built-In Transformer Step-Up DC/DC Converter With Low Voltage Stresses," *IEEE Transactions on Power Electronics*, vol. 41, no. 1, pp. 1137–1148, 2026, doi: 10.1109/tpel.2025.3608899.

[33] M. Elmi, M. R. Banaei, H. Afsharirad, and J. E. Valdez-Resendiz, "Study on a Trans-Inverse High Gain SEPIC-Based DC-DC Converter With ZCS Characteristics for Photovoltaic Applications," *International Transactions on Electrical Energy Systems*, vol. 2025, no. 1, 2025, doi: 10.1155/etep/3760078.

[34] R. K. Keshari and R. K. Singh, "LnC2n-2 Network-Based High-Gain Modular DC–DC Converter for PV Applications With MPPT," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 6, no. 2, pp. 677–686, 2025, doi: 10.1109/jestie.2024.3476942.

[35] T. Sakthiram, L. Yogesh, R. Srikanth, M. Prabhakar, and S. Angalaeswari, "Single-switch ultra-high step-Up DC-DC converter for PV applications," *Results in Engineering*, vol. 25, 2025, doi: 10.1016/j.rineng.2025.104050.

[36] S. V. K. Naresh, H. Shareef, and S. Peddapati, "An Ultra High Gain Quadratic Boost Converter with Low Electric Stress and Lower Inductor Currents for Photovoltaic Applications," presented at the 2024 Third International Conference on Power, Control and Computing Technologies (ICPC2T), 2024.

[37] M. F. Baba, A. V. Giridhar, and B. L. Narasimharaju, "Nonisolated high gain hybrid switched-inductor DC-DC converter with common switch grounding," *International Journal of Circuit Theory and Applications*, vol. 50, no. 8, pp. 2810–2828, 2022, doi: 10.1002/cta.3295.

[38] A. S. Mansour, A. H. Amer, E. E. El-Kholy, and M. S. Zaky, "High gain DC/DC converter with continuous input current for renewable energy applications," *Sci Rep*, vol. 12, no. 1, p. 12138, Jul 15 2022, doi: 10.1038/s41598-022-16246-8.

[39] G. G. Kumar, K. Sundaramoorthy, V. Karthikeyan, and E. Babaei, "Switched Capacitor–Inductor Network Based Ultra-Gain DC–DC Converter Using Single Switch," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 12, pp. 10274–10283, 2020, doi: 10.1109/tie.2019.2962406.

[40] E. Babaei, H. Mashinchi Maheri, M. Sabahi, and S. H. Hosseini, "Extendable Nonisolated High Gain DC–DC Converter Based on Active–Passive Inductor Cells," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 12, pp. 9478–9487, 2018, doi: 10.1109/tie.2018.2807367.

[41] M. Lakshmi and S. Hemamalini, "Nonisolated High Gain DC–DC Converter for DC Microgrids," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1205–1212, 2018, doi: 10.1109/tie.2017.2733463.

Biography

Seyed Moein Mortezaie is currently pursuing the M.Sc. degree in Power Electronics at Iran University of Science and Technology (IUST), Tehran, Iran. His research interests include high step-up DC–DC converters, fault diagnosis in DC–DC converters, resonant

converters, renewable energy systems, control of DC–DC converters, and electric vehicles.

Mohammad Sarvi received the M.Sc. and Ph.D. degrees in electrical engineering from Iran University of Science and Technology (IUST), Tehran, Iran.

He is currently an Associate Professor with the School of Electrical Engineering, Iran University of Science and Technology. His research interests include power electronics and the application of power electronics in wind and photovoltaic energy conversion systems.