Graphene Nano-Ribbon Field Effect Transistor under Different Ambient Temperatures

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Abstract: This paper is the first study on the impact of ambient temperature on the electrical characteristics and high frequency performances of double gate armchair graphene nanoribbon field effect transistor (GNRFET). The results illustrate that the GNRFET under high temperature (HT-GNRFET) has the highest cut-off frequency, lowest sub-threshold swing, lowest intrinsic delay and power delay product compared with low-temperature GNRFET (LT-GNRFET) and medium-temperature GNRFET (MT-GNRFET). Besides, the LT-GNRFET demonstrates the lowest off-state current and the highest ratios of Ion/Ioff, average velocity and mobile charge. In addition, the LT-GNRFET has the highest gate and quantum capacitances among three aforementioned GNRFETs.

Keywords: GNRFET; Ambient Temperature; Non-Equilibrium Green's Function (NEGF); High Frequency; Two-Dimensional FET Model.

1 Introduction

Graphene, a single atomic layer of graphite, is a huge material that experiences a new path in electronic applications. Due to its high carrier mobility and ultrathin body, graphene has attracted significant attention as a material for next-generation technologies that enhance the future high-speed Nano-electronic devices [1, 2].

Graphene is a tremendous candidate as a channel material for future high-speed field effect transistor (FET) performance beyond dimensional scaling. The band-gap of this material is zero. Nevertheless, when patterned into Nano-scale ribbons, a band-gap opens due to the lateral quantum confinement. The narrow stripes of graphene with width less than 100 nm, known as graphene Nano-ribbons (GNRs) have finite energy gaps. The GNRs display an impressive current-carrying capacity of more than 10^8 A/cm2 for the widths down to 16 nm. Furthermore, the breakdown voltage (BV) is estimated to be around 2.5 V for GNRs with widths of 22 nm [3-6].

The GNRs are used as the channel material on the transistors. Transistors made of GNRs are called Graphene-Nano-Ribbon Field Effect Transistors (GNRFETs), which are as potential alternatives to CMOS devices both experimentally and theoretically. One of the critical issues related to transistors is the ratio of ON-state current to OFF-state current (I_{on}/I_{off}) which is important parameter on switching performances of the device. Much of the attention has recently shifted to the use of graphene in RF transistors with large cut-off frequencies (f_T) [7-9].

Temperature is one of the device parameter with a major effect on the performance of GNRFET. In this paper we investigate the temperature effects on the electrical behaviour of GNRFET. The simulations are performed based on self-consistent solution of the Poisson- Schrödinger equations coupled with the Non-Equilibrium Green's Function (NEGF) method in mode space representation assuming the tight-binding Hamiltonian. Furthermore, we use a two dimensional "top-of-the-barrier" approach under ballistic transport in our study to extract some of the high-frequency characteristics of the GNRFET. All of the simulations are done under ballistic transport without any scattering and edge effects [10-12].

We have compared the performances of the low-temperature GNRFET (LT-GNRFET), medium-temperature GNRFET (MT-GNRFET) and the high-temperature GNRFET (HT-GNRFET). The results show that LT-GNRFET provides the high ratio of I_{on}/I_{off} which leads to the good switching performance of the device. Furthermore, the HT-GNRFET illustrates the better cut-off frequency and lower intrinsic delay and power delay product (PDP) in comparison with LT-GNRFET and MT-GNRFET.

2 Simulation and Modelling

Fig. 1 shows the representation of dual-gated GNRFET under study. A single layer of armchair Graphene Nano-Ribbon (A-GNR) with index of n = 12 is used as the channel material which is taken to be intrinsic. The index n, defines the number of dimmer

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carbon atom lines transverse to transport direction which is determined by the GNR width, W. The width and length of this GNR channel are assumed to be W = 1.35 nm and L = 12 nm, respectively. The insulating layers have 1 nm thickness and consist of the Sio_2 material with the dielectric constant of K = 3.9. The source and drain regions are assumed to be heavily doped GNR with doping concentration value of N_D = 2.86×10^8 m^{-1}.

The device characteristics are simulated by solving the ballistic transport equation using the Non-Equilibrium Green's Function (NEGF) formalism self-consistently with a 2-D Poisson's equation [13, 14]. In NEGF formalism the retarded Green's function of the device is defined as [8, 15],

$$G(E) = \left[(E + i0^+)I - H - U - \Sigma_S - \Sigma_D\right]^{-1} \quad (1)$$

where H is the device Hamiltonian. I is the identity matrix. $U = e\phi$ is on-site potential energy, where ϕ is the electrostatic potential which is obtained by solving 2-D Poisson equation. Σ_S and Σ_D are the self-energies of the source and drain, respectively.

The transmission probability of the carriers is [8],

$$T(E) = trace\left(\Gamma_S G \Gamma_D G^+\right) \quad (2)$$

where Γ is the contact broadening function extracted as [8],

$$\Gamma_{S(D)} = i(\Sigma_{S(D)} - \Sigma^+_{S(D)}) \quad (3)$$

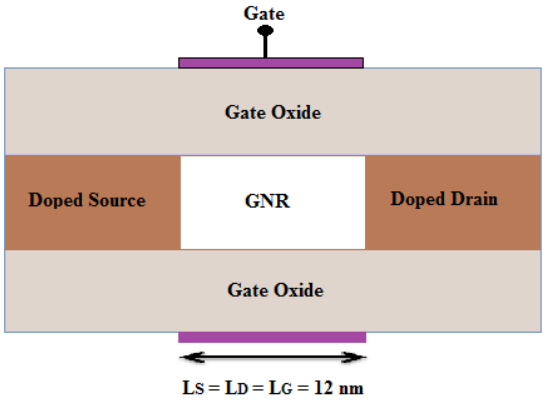


Fig. 1 Armchair GNRFET under study.

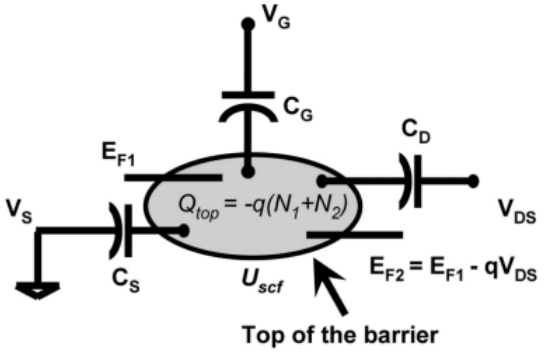


Fig. 2 Two-dimensional circuit model of MOSFET [12].

The local density are calculated using [8],

$$D_{S(D)} = G\Gamma_{S(D)}G^+ \quad (4)$$

The current–voltage characteristic is obtained as follows,

$$I = \frac{2q}{h}\int_{-\infty}^{+\infty} dE\, T(E)\{f(E,\mu_S) - f(E,\mu_D)\} \quad (5)$$

We have used a capacitance two-dimensional circuit model named "Top-of-the-barrier" model. It is an attempt to extract some of important characteristics of GNRFETs such as velocity, quantum and gate capacitances, mobile charge, intrinsic delay time, power delay product (PDP) and intrinsic cut-off frequency [12, 16].

In this model, the Poisson′s equation is solved at the top of the barrier through a capacitance model involving the gate insulator capacitance (C_G), drain capacitance (C_D), and source capacitance (C_S). The aforementioned capacitive model is illustrated in Fig. 2. The potential at the top of the barrier (U_{scf}) is controlled by the gate, source and drain potentials and by the location of two Fermi levels E_{f1} and E_{f2} [12, 16].

In the shaded region in Fig. 2, the amount of induced mobile charge at the top of the barrier is [12]:

$$Q_{top} = -q\left(N_1 + N_2\right) \quad (6)$$

where N_1 and N_2 are the density of positive velocity states filled by the source and the density of negative velocity states filled by the drain, respectively.

When the terminal biases are zero, the equilibrium electron density at the top of the barrier is N_0.

$$N_0 = \int_{-\infty}^{+\infty} D(E) f(E - E_f) dE \quad (7)$$

$$N_1 = \frac{1}{2}\int_{-\infty}^{+\infty} D\left(E - U_{scf}\right) f\left(E - E_{f_1}\right) dE \quad (8)$$

$$N_2 = \frac{1}{2}\int_{-\infty}^{+\infty} D\left(E - U_{scf}\right) f\left(E - E_{f_2}\right) dE \quad (9)$$

where $D(E)$ is the density of states at the top of the barrier, U_{scf} is the self-consistent voltage at the top of the barrier, E_f is the Fermi level and f is the equilibrium Fermi function. $E_{f1}=E_f$ and $E_{f2}= E_f - qV_{DS}$ are source and drain Fermi levels respectively.

The expression of the total potential U_{scf} becomes:

$$U_{scf} = U_L + U_P \quad (10)$$

where U_L is the Laplace potential and U_P is calculated using the linearized Poisson equation.

The equations of U_L and U_P are as follows:

$$U_L = -q\left(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S\right) \quad (11)$$

$$U_P = \frac{q^2}{C_\Sigma}\Delta N \quad (12)$$

where $\Delta N = (N_1+N_2)-N_0$ is the biased induced charge at the top of the barrier.

$$\alpha_G = \frac{C_G}{C_\Sigma}, \alpha_D = \frac{C_D}{C_\Sigma}, \alpha_S = \frac{C_S}{C_\Sigma} \quad (13)$$

where C_Σ is the parallel combination of the three capacitors shown in Fig. 2.

The current is given according to the following formula (14):

$$I_{DS} = \int_{-\infty}^{\infty} J(E - U_{scf})\left[f(E - E_{f_1}) - f(E - E_{f_2})\right] dE \quad (14)$$

where $J(E\text{-}U_{scf})$ is the "current density of states" which is expressed as:

$$J(E - U_{scf}) = \frac{1}{2} q \left(\frac{2}{\pi} \sqrt{\frac{2(E - U_{scf})}{m^*}} \right) D(E - U_{scf}) \quad (15)$$

3 Results and Discussions

In this section, the simulation results are presented along with the physical expressions. We study the performance of GNRFET under Three different ambient temperatures of T=200, 300 and 400 K. The GNRFET under the 200 ° K , 300 ° K and 400 ° K temperatures are called LT-GNRFET, MT-GNRFET and HT-GNRFET respectively.

Figs. 3(a) and 3(b) illustrate the simulated IDS-VGS characteristics and transconductance of the GNRFETs under three ambient temperature, respectively. As shown, LT-GNRFET has the lowest Off-state current and transconductance that are good features. This is due to the more thermal emission current stemming from strong control of the gate voltage on the channel near to source.

The transconductance is the ratio of current variation to the gate voltage variation at On-state and is given by [17]:

$$g_m = \frac{\partial I_D}{\partial V_G} \quad (16)$$

Fig. 4(a) depicts the Ion/Ioff ratio for GNRFET under different ambient temperatures. As it shown, the LT-GNRFET has the highest ratio of Ion/Ioff. The reason of this behaviour is described in the Fig. 3(a) where the LT-GNRFET experience the lowest Off-state current.

Fig. 4(b) represents the Sub-threshold Swing (SS) that is a key parameter to transistor miniaturization. Sub-threshold swing value at room temperature is defined with (17) in sub-threshold regime. A device with lower sub-threshold swing is more reliable. The smaller values of SS are desirable for low threshold voltage and low power operation when FETs scaled down to small sizes [18].

$$SS = \frac{dV_G}{d\left(\log(I_D)\right)} \quad (17)$$

The calculated I_{DS}-V_{DS} characteristics of the aforementioned GNRFETs are plotted in Fig. 5. We see that the HT-GNRFET has the highest delivering capability due to increase of thermal emission current in comparison with others.

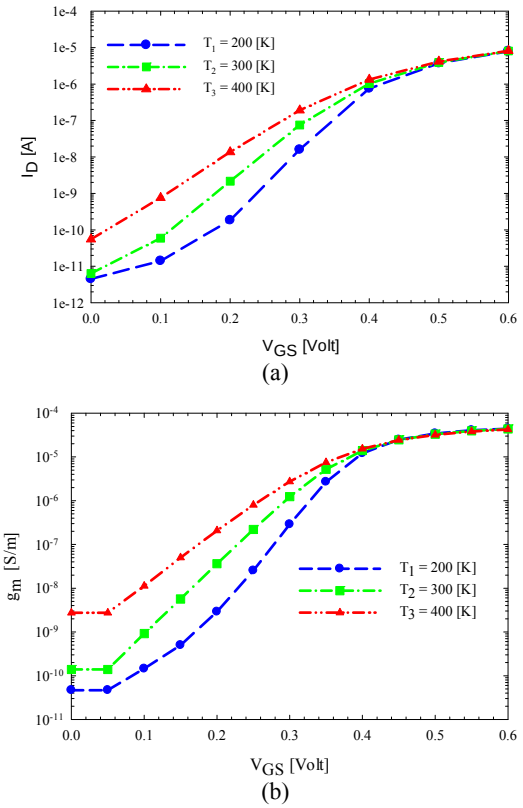


Fig. 3 (a) I_D-V_{GS} characteristic (b) Transconductance versus the gate voltage for LT-GNRFET, MT-GNRFET and HT-GNRFET at V_{DS} = 0.6 V.

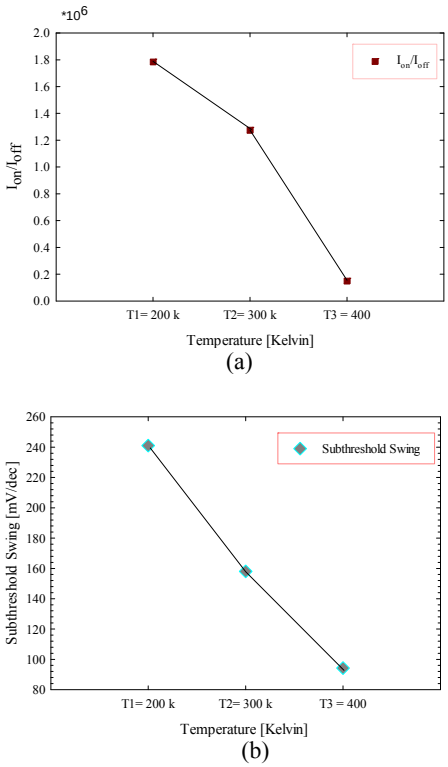


Fig. 4 (a) I_{on}/I_{off} ratio (b) Sub-threshold Swing (SS) versus the temperature for GNRFETs.

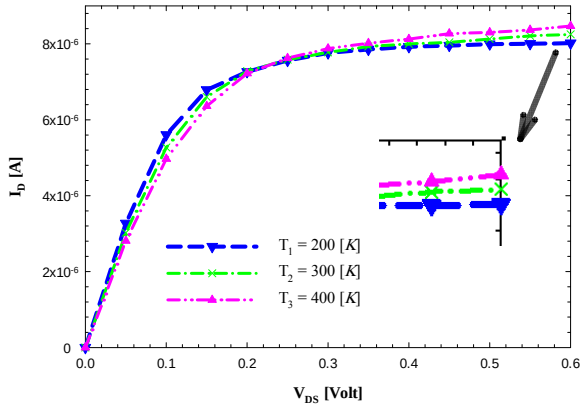


Fig. 5 Simulated current I_{DS} versus V_{DS} for GNRFETs under three different ambient temperatures.

Mobile charge is one of the important figures of merit for the transistors. Fig. 6 shows the variations of the mobile charge as a function of gate-source voltage for GNRFET under three different temperatures. The LT-GNRFET offers the highest mobile charge due to the strong effects of the gate voltage on the channel regions.

Now we discuss the average velocity behavior of carrier at the top of the barrier. This velocity is extracted in the linear region of sample FETs that is defined with [19],

$$\langle v \rangle = \frac{I_D(V_{GS}, V_{DS})}{-q\left[N_S(V_{GS}, V_{DS}) + N_D(V_{GS}, V_{DS})\right]} \tag{18}$$

Fig. 7 illustrates the average electron velocity at top of the barrier versus gate bias for aforementioned GNRFETs. As can be seen, the average electron velocity has the highest ratio for the LT-GNRFET and increases with V_{DS}.

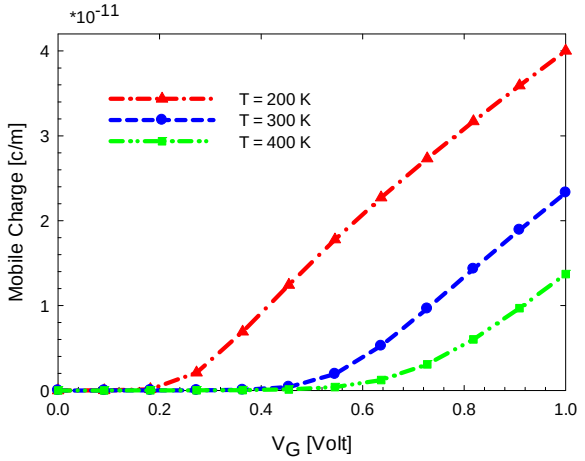


Fig. 6 Mobile charges versus gate voltage for LT-GNRFET, MT-GNRFET and HT-GNRFET at $V_{DS} = 0.6$ V.

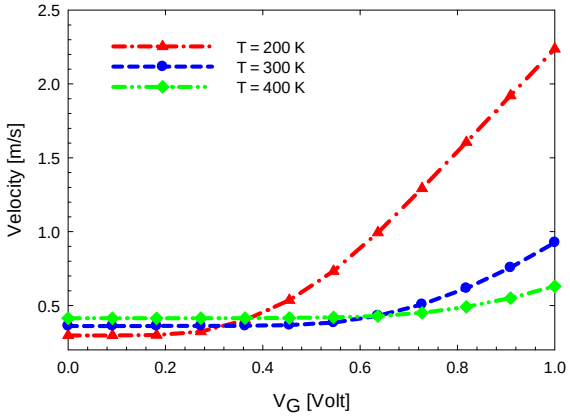


Fig. 7 Average electron velocity versus gate voltage for GNRFET under different ambient temperatures.

Now, we study the Gate and Quantum capacitances behaviours for GNRFET under different ambient temperatures. The gate capacitance (C_G) is modelled as a series combination of quantum capacitance (C_Q) and the insulator capacitance (C_{ins}) [8],

$$C_G = \frac{C_{ins} C_Q}{C_{ins} + C_Q} \tag{19}$$

where the quantum and gate-insulator capacitances are as follows,

$$C_Q = \frac{d(qN)}{d(-U_{scf}/q)} = q^2 \int_{-\infty}^{+\infty} D(E)\left(-\frac{\partial f(E - E_F)}{\partial E}\right) dE \tag{20}$$

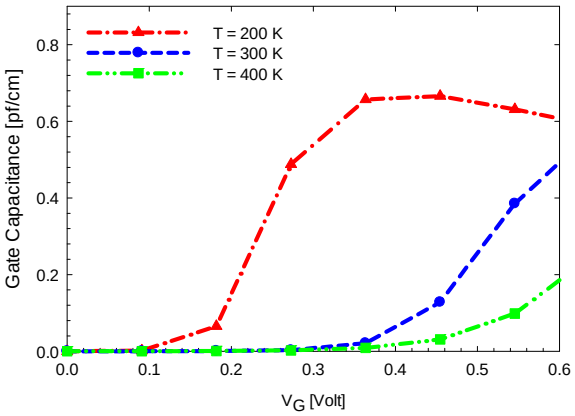
$$C_{ins} = N_G K \varepsilon_0 \left(\frac{W}{t_{ins}} + \alpha\right) \tag{21}$$

N_G is the number of gates, K is the relative dielectric constant of gate insulator, t_{ins} is the insulator thickness and α is a dimensionless fitting parameter.

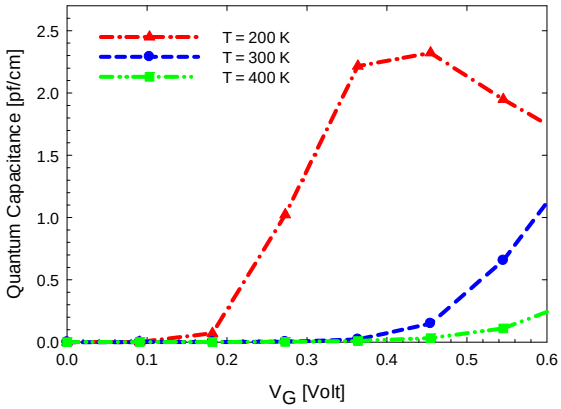
The Gate and Quantum capacitance as a function of gate voltage are shown in Figs. 8(a) and 8(b) respectively. We observe that the LT-GNRFET provides the highest gate capacitance which is a capacitance between gate and the channel region. And the HT-GNRFET offers the lowest quantum capacitance which is especially important for low-density-of-states systems.

When the gate voltage is high, the barrier height between the source and drain decreases, which increases the electron density in the channel, therefore the quantum capacitance increases.

Two important performance metrics that characterize the limitations on AC operation and switching behaviours of a transistor are intrinsic delay time (τ_s) and power-delay product (PDP). The PDP indicates the amount of energy consumed per switching event of the device. The values of intrinsic delay time and PDP can be obtained from Eqs. (22) and (23), respectively [20, 21].

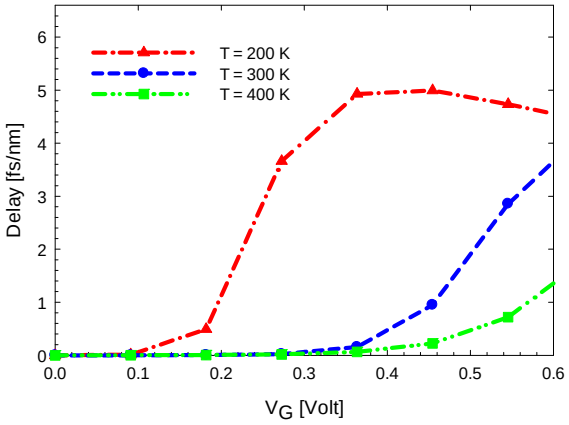


(a)

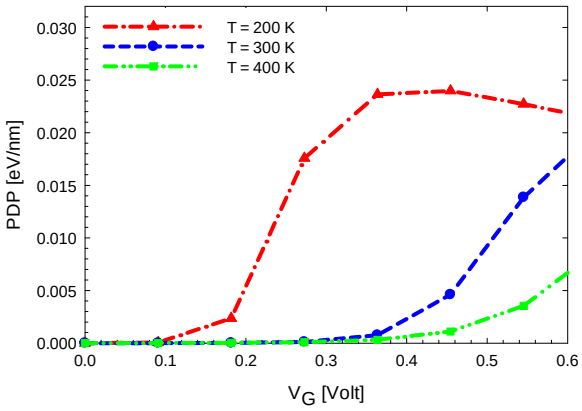


(b)

Fig. 8 (a) Gate capacitance, (b) Quantum capacitance versus gate bias for GNRFET under different ambient temperatures.



(a)



(b)

Fig. 9 (a) Switching delay time (b) Power-delay time product versus the gate voltage for GNRFET under different ambient temperatures.

$$\tau_s = \frac{C_G V_{DD}}{I_{ON}} \tag{22}$$

$$PDP = (I_{ON} V_{DD})\tau_s \tag{23}$$

where the On-state current is the drain current at $V_G = V_D = V_{DD} = 0.6$ V.

For GNRFETs operating at a given bias condition in linear or saturation regions, the intrinsic delay and PDP can be reduced by improving the material quality and using a better substrate. Here we examine the effects of ambient temperature on the performances of these parameters.

Figs. 9(a) and 9(b) illustrate the variations of switching delay time and PDP versus gate voltage for three aforementioned GNRFETs. We observe that the HT-GNRFET gives the lowest intrinsic delay time and PDP among three structures.

The intrinsic cut-off frequency (f_T) is an important parameter for high frequency and high speed performances of the transistors. It is the highest frequency, which a FET can support. The value of f_T can be obtained from the following equation [22],

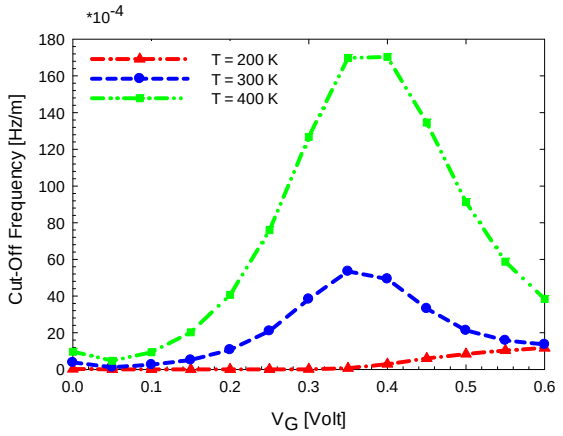


Fig. 10 Intrinsic cut-off frequency (f_T) versus gate bias for GNRFET under different ambient temperatures.

$$f_T = \frac{g_m}{2\pi C_g} \tag{24}$$

Fig. 10 presents the variations of the intrinsic cut-off frequency versus the gate bias voltage for GNRFETs under different ambient temperatures. As can be seen, this parameter increases with the gate voltage and sutures then decreases. The HT-GNRFET has the highest amount of f_T which means the best choice among these structures for the radio-frequency applications.

4 Conclusion

In this paper, we have studied the effects of different ambient temperatures on performances of Graphene Nano-Ribbon Filed-Effect transistors (GNRFETs). In order to extract the GNRFET characteristics, we applied the Non-Equilibrium Green's Function method to solve the Schrödinger equation self-consistently with 2-D Poisson equation. We have proposed three different ambient temperatures as 200, 300 and 400 kelvin that the GNRFETs with these temperatures are called LT-GNRFET, MT-GNRFET and HT-GNRFET respectively. We have used a double gate GNRFET with 12 nm channel length and source/drain doped reservoir. We have computed the characteristics of the device without the scattering and edge effects. We have investigated the current–voltage characteristics and switching parameters for three aforementioned structures of GNRFET. The results have shown that the LT-GNRFET has the lowest off-state current and the highest ratio of I_{on}/I_{off} among three aforesaid structures. The GNRFET under low ambient temperature demonstrates the best outputs of transconductance, mobile charge, gate capacitance and average electron velocity. Whereas The HT-GNRFET offers the lowest amount of sub-threshold swing, quantum capacitance, intrinsic delay time and Power delay product. Furthermore, the intrinsic cut-off frequency is calculated. Comparison among the LT-GNRFET, MT-GNRFET and HT-GNRFET revealed that the HT-GNRFET has the highest intrinsic cut-off frequency which is the best structure for the high frequency operations. And the MT-GNRFET offers the middle output characteristics during our discussions.

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