Iranian Journal of Electrical and Electronic Engineering

Journal Homepage: ijeee.iust.ac.ir

Research Paper

Modeling and Simulation of Common Mode Voltage in a Three-Phase Delta Connection STATCOM with Parasitic Capacitors

S. Shabani*, M. Asadi*(C.A), and A. Zakipour*

Abstract: In this paper, parasitic capacitors and common mode voltage (CMV) are modeled in a delta connection multilevel cascaded STATCOM. In high frequency and high voltage applications the parasitic capacitors play important role in common mode voltages. In this paper, parasitic capacitors and CMV are modeled in a multilevel cascaded STATCOM and also parasitic currents are calculated, then a method will be proposed to reduce the effects of the parasitic capacitors. The values of parasitic capacitors are calculated by finite element software. Finally, a delta connection 13-level cascaded STATCOM with parasitic capacitors will be simulated in MATLAB Simulink and then simulation results will be presented.

Keywords: STATCOM, Common Mode Voltage, Multilevel Inverters, Parasitic Capacitors.

Nomenclature

C_{gi}	The parasitic capacitors
C_{Ti}	The total parasitic capacitors
e_a	A-phase voltage of grid
e_b	B-phase voltage of grid
e_c	C-phase voltage of grid
i_a	A-phase line current of STATCOM
i_b	B-phase line current of STATCOM
i_c	C-phase line current of STATCOM
L	The number of levels
L_m	Inductance of each phase
N	The floating point of the STATCOM
P	The number of cells
R_m	Resistance of each phase
S_A	Switching state of A-phase in star connection
S_B	Switching state of B-phase in star connection
S_C	Switching state of C-phase in star connection
S_{AB}	Switching state of AB-phase in delta connection
S_{BC}	Switching state of BC-phase in delta connection
S_{CA}	Switching state of CA-phase in delta connection
V_{AN}	A-phase voltage of STATCOM
V_{BN}	B-phase voltage of STATCOM
V_{CN}	C-phase voltage of STATCOM
V_{dc}	DC link voltage of STATCOM
V_{nN}	The voltage between the floating point of the STATCOM and grid
V_{cm}	Common mode voltage
$\overrightarrow{V_s}$	The voltage vector of 3-phse

Iranian Journal of Electrical and Electronic Engineering, 2023. Paper first received 12 Sep 2021, revised 13 Dec 2022, and accepted 16 Dec 2022.
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https://doi.org/10.22068/IJEEE.19.1.2281

1 Introduction

TODAY power electronic converters are widely used in industrial applications. In the converter, the semiconductor switches are employed to generate pulse width modulation (PWM) waveforms. Increasing of the switching frequency can significantly reduce the total harmonic distortion (THD) of the output voltage. But increasing of the frequency causes problems. One of these problems is the production of undesirable voltages such as common mode voltage. The common mode voltage will cause problems, such as: leakage currents through the parasitic capacitors, conductive and radiation electromagnetic interference that affect the performance of the other electrical equipment. Therefore, the reduction of the common mode voltage should be considered in the design of power electronic systems.

Multilevel converters are suitable in the high voltage. One of the important applications of multilevel converters is STATCOM [1]. In the multilevel converters, the output voltage is close to sinusoidal waveform and the stress of dv/dt is low [2]-[4]. Diode clamped, Flying capacitor and cascaded are conventional multilevel converters. The Diode clamped and Flying capacitor topologies requires additional diodes and capacitors respectively. Whereas, the multilevel cascaded converters produce higher voltage levels by fewer elements. There are different ways to reduce EMI in two-level and multilevel inverters. The common mode voltage reduction techniques can be divided into three types: passive or active filters, control methods, modulation methods. One of these methods is using a transformer at the inverter output in order to isolated common mode currents. This method increases the weight, size and cost of the system and reduces the total efficiency [5]. Other methods use RLC filters including a series DM-inductor and capacitors and resistors (RC). Internal EMI filtering techniques create paths of common mode current within the converter. These filters can be designed in special structures to eliminate common mode and differential mode frequencies [6]-[10]. This method increases weight and costs of the system. Active EMI filters (AEF) can be used instead of passive filters. The AEFs use the active electronic circuits to cancel or eliminate the EMI. An AEF can be forward type or feedback type, or combination of them [11]. In [12], an Active common mode canceler (ACC) is proposed that can eliminate the common mode voltage produced by PWM. Control method can be employed to eliminate common mode voltage. In [13] a predictive control method is used, and common mode voltage is used as constraint of the objective function. The control law is adjusted to reduce the common mode voltage.

PWM and space vector modulation (SVM) can be used to reduce common mode voltage. In [14], a method proposed that the common mode voltage will be zero by adding suitable delays to the switches gate pulses. In [15], the switching states are selected to maintain the common mode voltage at a constant value. This method can reduce the common mode voltage transient states. Common mode voltage can produce common mode current through parasitic capacitors between converter elements and the ground. Therefore, the magnitude of these currents depends on the variation of the common mode voltage and the terminal voltage. In [16]-[18] the common mode voltage is eliminated by the modulation method. In the most modulation methods, the common mode voltage is eliminated by particular switching states.

In [19], a cost-effective nested five-level converter is presented that is composed of the three-level flying capacitor converter and dual T-type three-level circuits. The proposed converter is transformerless, so it suffers the CMI. The zero common-mode space vector modulation (ZCM-SVM) is proposed to reduce CMV. The mathematic calculations are reduced by the new procedure SVM. Complex equations have become simplified to find appropriate vectors in seven-level inverter to reduce CMV. In [20], the CMV is reduced using new proposed SVM in a multilevel cascaded that new proposed SVM reduces amount of mathematic calculation. In [21], a method is proposed that increase the linear modulation range without increasing of the DC bus voltage to eliminate CMV. In [22], an optimized topology is proposed that uses lower elements than the existing configurations to produce three-level voltages. The proposed structure used PWM strategy for the CMV elimination.

In most papers, modeling of parasitic capacitors has been discussed in the PV systems or between the phase node and ground, but it has not been investigated parasitic capacitors between the inverter elements and ground. In this paper, the modeling of the parasitic capacitors between the inverter elements and ground or protective wall is presented in a delta connection cascaded multi-level STATCOM. These capacitors are also calculated in the finite element software then their effects on CMV will be investigated. In most articles, the issue of CMV has been studied in star connection systems, while less attention has been paid to delta connection. In this paper, parasitic currents are calculated in terms of switching states. Then they reduce by space vector modulation. The effect of common mode current reduction on CMV will be investigated. This paper is organized as follows: Section 2 presents the mathematical model of the STATCOM and analyzes the CMV in STATCOM star and delta connection, and Section 3 presents modeling of the parasitic capacitances and calculation of their value in finite element software; Section 4 presents simulation results of the 13-level cascaded STATCOM delta connection; Section 5 draws the conclusion.

2 Common Mode Voltage in STATCOM

The STATCOM based on the voltage source inverter (VSI) is shunt connected to the grid through

a coupling inductance. The STATCOM can control magnitude, the phase angle and the frequency of the output voltage used to compensation of the reactive power. The electrical circuit is shown in Fig. 1. The mathematical equations of the STATCOM output voltages and currents [23]:

$$\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = -\frac{R}{L}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{1}{L}\begin{bmatrix} e_a - v_a \\ e_b - v_b \\ e_c - v_c \end{bmatrix} \quad (1)$$

Where $v_x(x = a, b, c)$ is produced by the inverter. This voltage contains harmonic and non-sinusoidal components. According to Fig. 1, phases (a, b, c) can be connected together to form a star connection. According to Fig. 2, these phases can also be connected together to form a delta connection. In STATCOM, the DC link must be set to certain values by the controller. In this paper, we assume a constant value for it. A schematic of STATCOM based on cascaded multilevel inverter is shown in Fig. 1, which consists of several cells (H-bridge inverter) which their number is P.

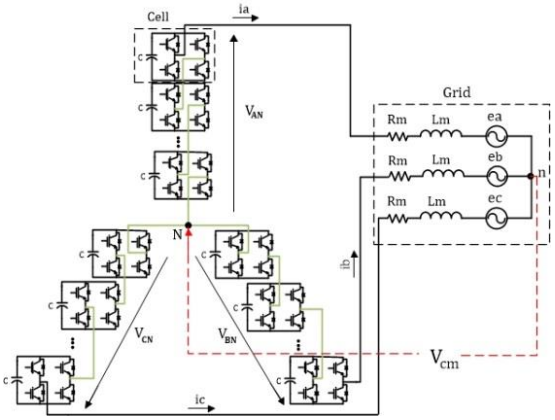


Fig. 1 The multilevel cascaded star connection STATCOM.

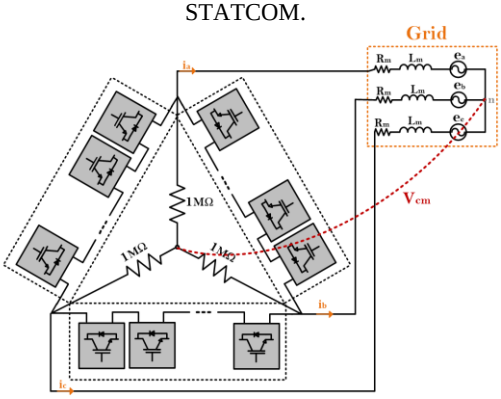


Fig. 2 The multilevel cascaded delta connection STATCOM.

According to Fig. 1, the output voltage of each phase relative to the floating point N in multilevel cascaded as follows:

$$V_{AN} = S_A V_{dc} \quad (2)$$

$$V_{BN} = S_B V_{dc} \quad (3)$$

$$V_{CN} = S_C V_{dc} \quad (4)$$

The switching states can be written as $0, \pm1, \pm2, \ldots, \pm\mathrm{P}$, and the number of levels will be explained as:

$$L = 2P + 1 \quad (5)$$

2.1 STATCOM Star Connection

Figure 1 shows a multilevel cascaded STATCOM with star connection. The output voltages relative to the neutral point n are:

$$V_{AN} = R_m i_a + L_m \frac{di_a}{dt} + e_a + V_{nN} \quad (6)$$

$$V_{BN} = R_m i_b + L_m \frac{di_b}{dt} + e_b + V_{nN} \quad (7)$$

$$V_{CN} = R_m i_c + L_m \frac{di_c}{dt} + e_c + V_{nN} \quad (8)$$

The voltage of V_{nN} is the same as CMV. The CMV in balanced condition will be:

$$V_{cm} = \frac{1}{3}(V_{AN} + V_{BN} + V_{CN}) \quad (9)$$

By inserting (2)-(4) in (9):

$$V_{cm} = \frac{V_{dc}}{3}(S_A + S_B + S_C) \quad (10)$$

This equation shows that value of the CMV is reduced by certain combinations of the switching states. These combinations can be applied by SVM.

Fig. 2 shows the delta connection multilevel cascaded STATCOM. According to Fig. 2, the floating point in this structure can be considered common point of three high resistances. In this type of connection, like the star connection, the equations related to the voltages and currents of the inverter can be obtained by (6)-(8), which V_{xN} $(x = a, b, c)$ is the voltage of each resistance. The vector diagram in Fig .3 can be used to calculate the voltage values of each phase of the delta connection multilevel cascaded inverter.

According to Fig. 3-(a), if v_x $(x = a, b, c)$ is considered the voltage of extra resistances, then the voltage of each phase of the inverter will be(v_{ab}, v_{bc}, v_{ca}). According to Fig. 3-(b), the voltage of extra resistances can be obtained through the inverter phase voltages:

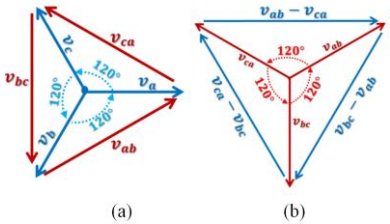


Fig. 3 Vector diagram for inverter voltages with delta connection: (a) inverter and the added resistances, (b) Inverter and voltage difference between them.

$$v_a = \frac{1}{3}(v_{ab} - v_{ca}) \quad (11)$$

$$v_b = \frac{1}{3}(v_{bc} - v_{ab}) \quad (12)$$

$$v_c = \frac{1}{3}(v_{ca} - v_{bc}) \quad (13)$$

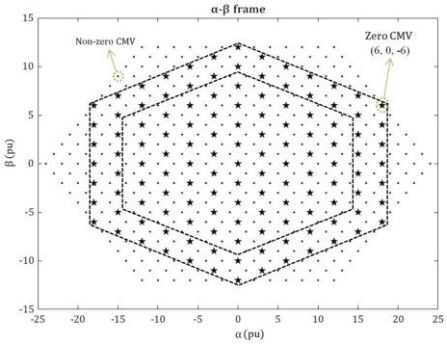
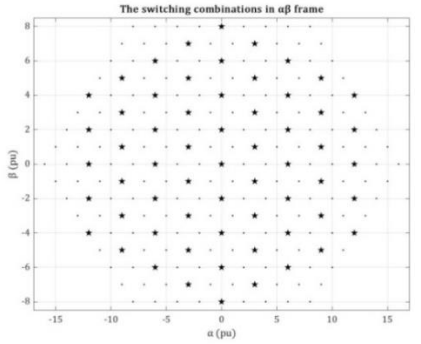
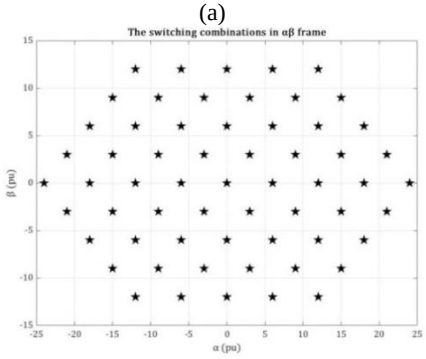


Fig. 4 The switching combinations in frame $\alpha\beta$ for 13-level cascaded STATCOM.



(a)



(b)

Fig. 5 The switching combinations in αβ frame: (a) 9-level cascaded star connection, (b) extended 17-level cascaded delta connection.

Fig. 4 shows all the switching combinations of the 13-level cascaded STATCOM. Star-shaped points are the switching combinations that make zero CMV. The voltage of extra resistances in the simulation should equal to (11)-(13) in zero CMV. In this paper, another method is proposed to eliminate the common mode voltage at the delta connection. In this method, the star connection multilevel cascaded is considered as the phase equivalent of the delta connection. Then, by the previous method, the combinations of switching are found to reduce the common mode voltage in this connection. Finally, these switching combinations in star connection are expanded to the delta states. As shown in Fig. 5-a and 5-b, the phase equivalent of a 17-level cascaded delta connection is a 9-level cascaded star connection that the number of star connection line voltage levels is 17-level. Because there is a phase difference of 30° between the delta and star connections, all the connections are rotated by 30°, as shown in Fig. 6.

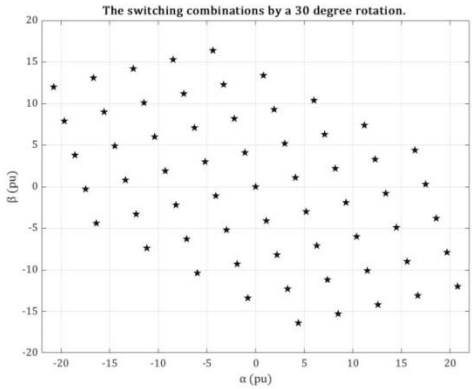


Fig. 6 The switching combinations by a 30 degree rotation.

3 Modeling of Parasitic Capacitors

In high-power inverters, there is often a protective wall around the IGBT valve. If this wall is connected to ground, then it will have zero voltage. In this paper, the ABB Company IGBT switch is used in IGBT valve that shown in Fig. 7 According to the collector blades shown in Fig. 7, if it is exposed to voltage then undesirable capacitors create between the collector blades and the protective wall.

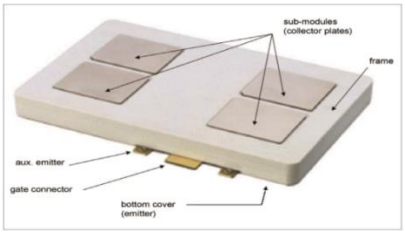


Fig. 7 IGBT press-pack modules [24].

As shown in Fig. 8, the parasitic capacitors (C_{gi}) will be created between the collector blades and the wall. The total parasitic capacitors (C_{Ti}) in the switch is:

$$C_{Ti} = \frac{C_{gi}}{n} \quad (14)$$

Where *n* is the number of sub-modules. If there is one parasitic capacitor in each cascaded inverter cell, it can be modeled as Fig. 8.

The output voltage of each cell is modeled as a voltage source as Fig. 9. These voltage sources are proportional to the switching state ($x = a, b, c$).

The current flows through parasitic capacitors:

$$i_{CTP} = C_{TP}\frac{dv_{xp}}{dt} \tag{15}$$

For each capacitor:

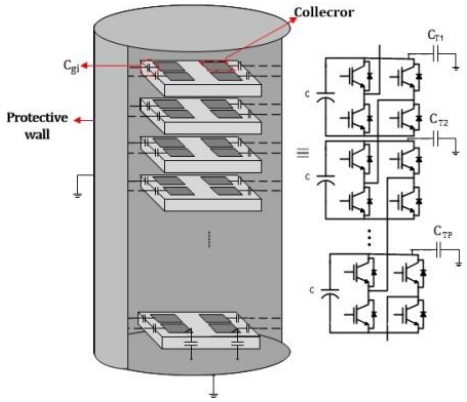


Fig. 8 Model of the parasitic capacitors.

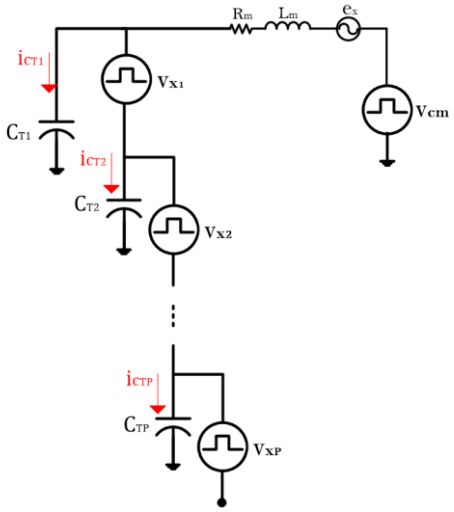


Fig. 9 Modeling of parasitic capacitors in an IGBT valve.

$$\begin{aligned} i_{CT1} &= C_{T1}\frac{dv_{xp}}{dt} \\ &= C_{T1}\frac{S_{a1}V_{dc} + S_{a2}V_{dc} + \cdots + S_{aP}V_{dc}}{T_s} \end{aligned} \tag{16}$$

$$\begin{aligned} i_{CT2} &= C_{T2}\frac{dv_{xp}}{dt} \\ &= C_{T2}\frac{S_{a2}V_{dc} + S_{a3}V_{dc} + \cdots + S_{aP}V_{dc}}{T_s} \end{aligned} \tag{17}$$

$$i_{CTP} = C_{TP}\frac{dv_{xp}}{dt} = C_{TP}\frac{S_{aP}V_{dc}}{T_s} \tag{18}$$

The sum of the above currents in a phase:

$$\begin{aligned} i_{CTa} = \sum_{i=1}^{P} i_{CTi} = V_{dc}f_s\{&C_{T1}(S_{a1} + S_{a2} \\ &+ \cdots + S_{aP}) \\ &+ C_{T2}(S_{a2} + \cdots + S_{aP}) \\ &+ \cdots + C_{TP}S_{aP}\} \end{aligned} \tag{19}$$

$$\begin{aligned} i_{CTb} = \sum_{i=1}^{P} i_{CTi} = V_{dc}f_s\{&C_{T1}(S_{b1} + S_{b2} \\ &+ \cdots + S_{bP}) \\ &+ C_{T2}(S_{b2} + \cdots + S_{bP}) \\ &+ \cdots + C_{TP}S_{bP}\} \end{aligned} \tag{20}$$

$$\begin{aligned} i_{CTc} = \sum_{i=1}^{P} i_{CTi} = V_{dc}f_s\{&C_{T1}(S_{c1} + S_{c2} \\ &+ \cdots + S_{cP}) \\ &+ C_{T2}(S_{c2} + \cdots + S_{cP}) \\ &+ \cdots + C_{TP}S_{cP}\} \end{aligned} \tag{21}$$

According to (10) for zero CMV:

$$S_A + S_B + S_C = 0 \tag{22}$$

$$S_A = S_{a1} + S_{a2} + \cdots + S_{aP} \tag{23}$$

$$S_B = S_{b1} + S_{b2} + \cdots + S_{bP} \tag{24}$$

$$S_C = S_{c1} + S_{c2} + \cdots + S_{cP} \tag{25}$$

So the sum of the currents of three-phase will be:

$$\begin{aligned} i_{CT} = \sum_{i=a.b.c} i_{CTi} = \\ V_{dc}f_s\begin{Bmatrix} C_{T1}(S_A + S_B + S_C) \\ +C_{T2}(S_A + S_B + S_C - S_{a1} - S_{b1} - S_{c1}) \\ + \cdots + C_{TP}(S_{aP} + S_{bP} + S_{cP}) \end{Bmatrix} \end{aligned} \tag{26}$$

The first part of the above equation is zero according to (22) then:

$$i_{CT} = V_{dc}f_s\begin{Bmatrix} -C_{T2}(S_{a1} + S_{b1} + S_{c1}) \\ -C_{T3}\begin{pmatrix} S_{a1} + S_{b1} + S_{c1} \\ +S_{a2} + S_{b2} + S_{c2} \end{pmatrix} \\ \ldots - C_{TP}(S_{a1} + S_{b1} + S_{c1} + \cdots \\ +S_{a(P-1)} + S_{b(P-1)} + S_{c(P-1)}) \end{Bmatrix} \tag{27}$$

By the suitable switching combinations, the current (i_{CT}) can be zeroed. According to (27), the switching combinations of three-phase cells will be zero step by step:

$$S_{a1} + S_{b1} + S_{c1} = 0 \tag{28}$$

$$S_{a2} + S_{b2} + S_{c2} = 0 \tag{29}$$

$$\vdots$$

$$S_{aP} + S_{bP} + S_{cP} = 0 \tag{30}$$

The amount of total parasitic current will be zero using the (22), (28)-(30), and CMV will also decrease.

4 Simulation Results

In section 4.1, parasitic capacitors are simulated in a finite element software. A sample of the distribution of the voltage, distribution of the energy and distribution of the electric field are presented to analyze. The values of the parasitic

capacitors are calculated by the finite element software. In the next sections, a multilevel cascaded STATCOM is simulated with the parasitic capacitors in the delta connections. The common mode voltage and the total current of the parasitic capacitors are reduced by vector space modulation by using the certain switching combination.

4.1 Calculation of Parasitic Capacitors

In this paper, the amount of parasitic capacitors is calculated in the finite element software. First, the dimensions and material are determined in an IGBT valve (by selecting ABB press pack switches), as shown in Fig. 10. To calculate the value of each capacitor, the metal blades of the collector are exposed to voltage, and the boundary conditions are determined for protective wall and ground.

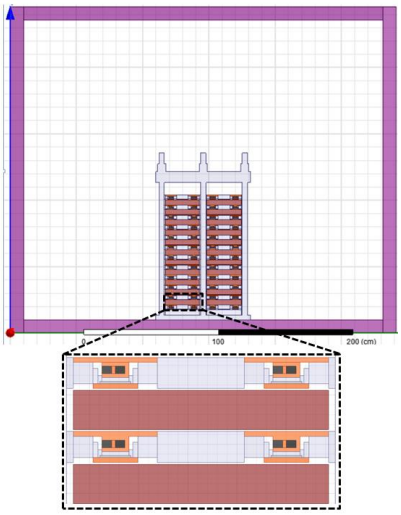
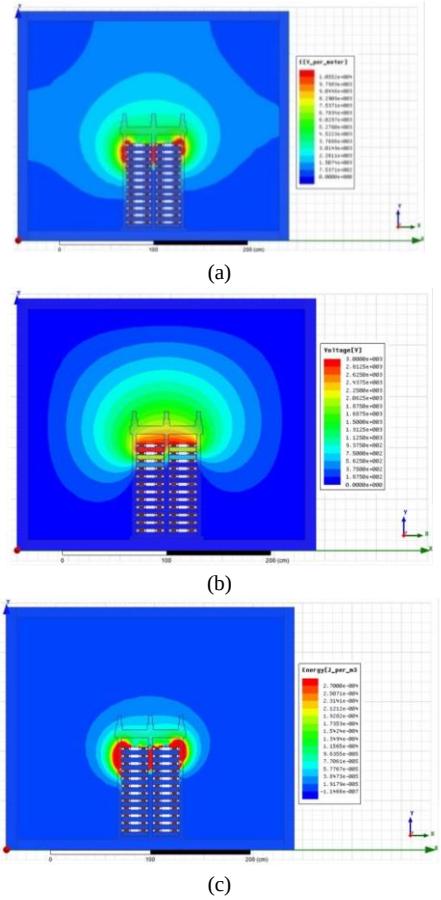


Fig. 10 The IGBT-valve simulation in the finite element software.

Fig. 11 shows the simulation results in finite element software, which includes: voltage distribution and electric field distribution around the first cell exposed to voltage. As shown in Fig. 11, if the collector blade of each switch is exposed to voltage during switching, then electric fields will form around it. This electric field will be suitable space to create parasitic capacitors. The values of the capacitors are calculated by finite element software.

Table. 1 shows the calculated parasitic capacitor values for a STATCOM based 13-level cascaded inverter. The parasitic capacitor values decrease from the upper cell (C_{T1}) to the lower cell (C_{T6}) respectively because the distance between ground and collector blades are reduced. In other words, the lower cells are closer to the ground. The materials and dimensions of the devices have also a significant impact on the value of the parasitic capacitors.



(a)

(b)

(c)

Fig. 11 Distribution of: (a) electric field, (b) voltage, (c) energy in around of the IGBT valve.

Table 1 Parasitic capacitors values.

C_{Ti}	C_{T1}	C_{T2}	C_{T3}	C_{T4}	C_{T5}	C_{T6}
Value (PF)	57.425	63.24	70.22	77.86	87.51	102.39

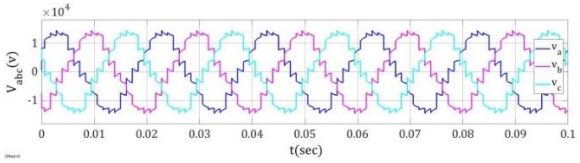
4.2 Simulation Results for the Delta Connection STATCOM

In this section, a delta connection 13-level cascaded STATCOM is simulated with the parasitic capacitors calculated in Section 3. The MATLAB simulation was performed once by applying the parasitic currents elimination method and once without applying the parasitic currents elimination method. The simulation parameters are presented in Table. 2.

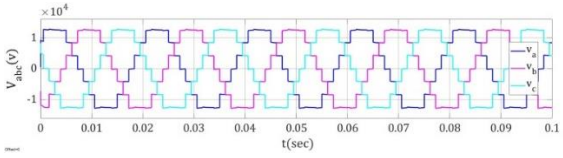
Table 2 The simulation parameter.

Parameters	Value
Line Voltage $V_{L-L}(kv)$	20
DC Link Voltage for the delta connection V_{dc}(kv)	4.2
Inductive Coupling for the delta connection L_m (mH)	3.6
Line frequency f (Hz)	50
Line resistance R_m (Ω)	0
Added resistance ($M\Omega$)	1

Fig. 12 shows the output phase voltage of the STATCOM. As can be seen, the voltage waveform has less distortion by the proposed method. Figures 13 and 14 show the parasitic currents and the CMV, respectively. As can be seen, the parasitic current, despite having a small value range, has a great effect on the CMV. The CMV is reduced from 2 kV to less than 200 V by the elimination parasitic currents by the proposed method, is shown in Fig. 14.

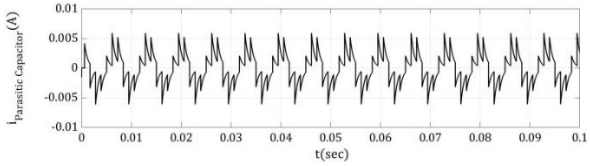


(a)

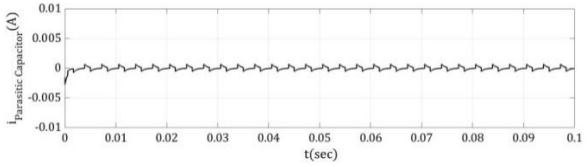


(b)

Fig. 12 STATCOM output voltages: (a) without parasitic current reduction conditions, (b) With parasitic current reduction conditions.

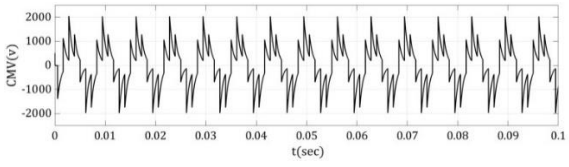


(a)

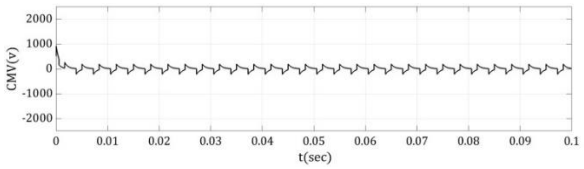


(b)

Fig. 13 Parasitic current: (a) without parasitic current reduction conditions, (b) With parasitic current reduction conditions.



(a)



(b)

Fig. 14 CMV: (a) without parasitic current reduction conditions, (b) With parasitic current reduction conditions.

Fig. 15 shows the STATCOM output current. Fig. 16 shows the effect of switching on the amount of parasitic capacitor currents in a multilevel cell. As shown, the increase stress of the dv/dt of each multilevel cell is directly related to the capacitors current, which confirms the correctness of the proposed modeling. If the switching frequency increases, then the number of parasitic current spikes increases. As a result, the STATCOM phase voltage distortion also increases. This topic shows the effect of multilevel inverter in reduction of the number of parasitic current spikes.

5 Conclusion

In this paper, parasitic capacitors are modeled around the IGBT valve. The parasitic currents flow through undesirable capacitors due to the switching. The materials and dimensions of the devices have a significant impact on the value of the parasitic capacitor. The waveforms show that the parasitic currents depend on the switching states. The amplitude of this currents depend on the value of the capacitors. As shown in the simulation results, parasitic currents have a large effect on the amount of CMV. As a result, modeling and using a suitable method to eliminate parasitic current and CMV is very important. The simulation results confirm the validation of the modeling and the validation of the proposed method to reduce CMV.

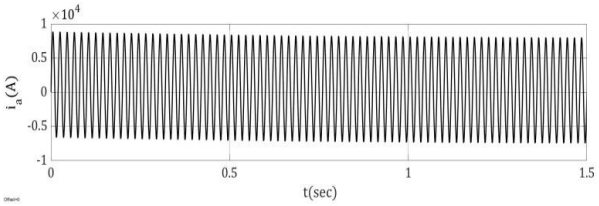


Fig. 15 STATCOM output current.

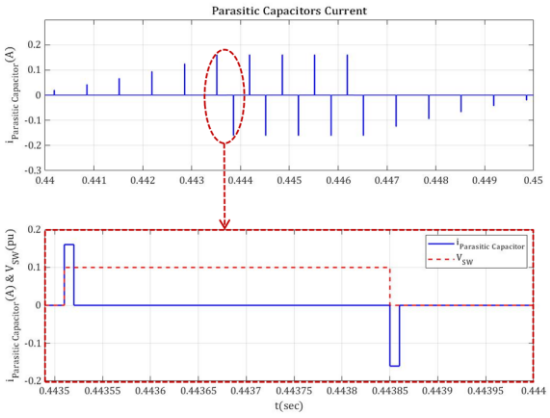


Fig. 16 variation of parasitic current by switching.

Intellectual Property

The authors confirm that they have given due consideration to the protection of intellectual property associated with this work and that there are no impediments to publication, including the timing to publication, with respect to intellectual property.

Funding

No funding was received for this work.

CRediT Authorship Contribution Statement

S. Shabani: Software and Simulation, Research & Investigation. **M. Asadi:** Supervision, Project Administration, Idea & Conceptualization, Revise & Editing. **A. Zakipour:** Research & Investigation, Revise & Editing.

Declaration of Competing Interest

The authors hereby confirm that the submitted manuscript is an original work and has not been published so far, is not under consideration for publication by any other journal and will not be submitted to any other journal until the decision will be made by this journal. All authors have approved the manuscript and agree with its submission to "Iranian Journal of Electrical and Electronic Engineering".

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