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An Electronically Tunable Floating Meminductor Emulator Based on VDDDA and Its Application

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Abstract: This paper introduces a floating flux-controlled meminductor emulator, implemented using two voltage differencing differential difference amplifier (VDDDA) along with a memristor and capacitor. Grounded and floating configurations are simulated with TSMC 0.18 µm level-49 BSIM3 CMOS process parameters in LTspice, showcasing the performance of the proposed circuits. The circuit features electronic tunability, allowing for the adjustment of nonlinear flux through the tuning of bias voltage. Simulation results validate the frequency-dependent current-flux dynamics of the proposed meminductor emulator. The simulation results, which involve frequency-dependent pinched hysteresis loops, transient analysis, non-volatility, and Monte Carlo analysis of the proposed meminductor, affirm the functionality and adequacy of the proposed design. A Chua's oscillator is realized using proposed VDDDA-based meminductor as non-linear element.

Keywords: Chua's Circuit, Electronically Adjustable Emulator, Hysteresis Loop, Memristor, Meminductor, Mem-element, Oscillator, VDDDA

1 Introduction

BEFORE 1971, only three traditional circuit elements were recognized: resistors, capacitors, and inductors. However, in 1971, Professor Leon Chua introduced a groundbreaking addition to this list – the memristor [1]. Chua's discovery was rooted in the realization that fundamental quantities like charge, flux, current, and voltage possessed well-established relationships with each other. Five out of six of these fundamental relationships were well-defined, with one missing link: the connection between charge and flux as shown in Fig. 1. This gap in the understanding led to the invention of the memristor, an element that uniquely bridges charge and flux [2]. A memristor resembles conventional passive components but exhibits a critical nonlinearity; it can remember previous states. This memory-like property has generated substantial excitement among researchers worldwide. The first physical realization of Chua's memristor concept came in 2008 from HP Labs [3], utilizing TiO2 sandwiched between layers of Platinum (Pt). This development reignited global interest in memristors, leading to the emergence of new elements, including memcapacitors and meminductors, collectively known as mem-elements [4].

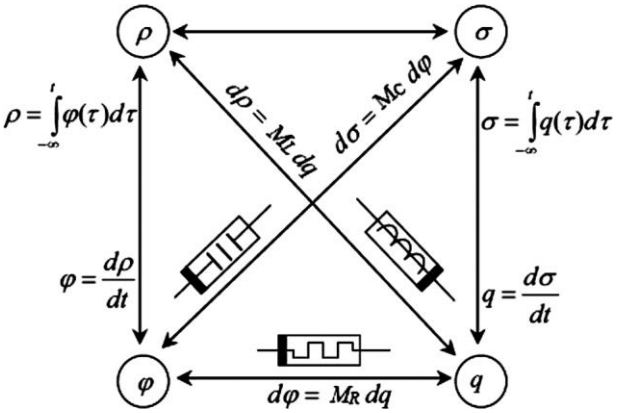

Fig. 1 Relationship among fundamental elements

The term mem-elements is aptly chosen because these components share the ability to store and retain past

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data, much like conventional memory devices [5]. This characteristic represents a significant step forward in fields such as neural networks, communications, and the electronics industry, offering the potential to redesign cumbersome circuits with fewer components, occupying less space and consuming less power, ultimately leading to more compact and efficient circuit designs.

Mem-elements serve as a source of inspiration for creating circuits capable of storing previous data, facilitating future result processing, predicting patterns, and enabling machines in machine learning to learn regressively over time. These benefits are harnessed by exploiting the nonlinear characteristics of mem-elements [6]. In diverse domains, the memristor has been applied in various capacities, including chaotic circuits [7], non-volatile memories [8], neural networks [9], programmable analog circuits [10], and adaptive filters [11].

Consequently, the non-linear relationship between charge and flux has emerged as a new research frontier, enabling the modelling of innovative circuits with numerous advantages over traditional counterparts. Until now, the physical realization of these mem-elements remained elusive in our everyday world, leading to the proposal of multiple emulator circuits to identify the most suitable one. Additionally, the literature presented in this context introduces a meminductor emulator achieved with a few components, incorporating VDDDA as an active building block (ABBs), resulting in a compact circuit well-suited for a broad frequency range.

The journey of emulating meminductors commenced in 2009 [12] when the first emulator was introduced. Following this, the SPICE model [13] for mem-elements was unveiled in 2012, and in 2014, an emulator based on the AD844 was introduced. These circuits integrated various components, including current conveyor-II (CCIIs), adders, resistors, operational amplifiers (OPAMPs), dependent current sources, capacitors, modulator and demodulator ICs, switches, and inductors [14]. An alternative floating meminductor emulator was developed in 2014 using two OPAMPs, a multiplier, four second-generation current conveyors (AD844), two conventional OPAMPs (TL084), a multiplier (AD633), and several resistors and capacitors [15].

A significant development in 2016 involved the introduction of a flux-controlled meminductor emulator. However, from 2020 onwards, there has been a shift towards designing meminductors with memristors, resulting in reduced complexity and fewer components. For instance, one circuit employed various components such as operational transconductance amplifier (OTA), multiplier, CCIIs, current feedback operational amplifier, resistors, and capacitors, working in both floating and grounded configurations [16]. Another circuit employed meminductor based on Antoniou's circuit utilized multiple resistors and OPAMPs only [17].

Starting from 2021, meminductor emulators were developed with fewer elements, such as two voltage difference transconductance amplifier (VDTA) without analog multipliers, a resistor-less grounded meminductor emulator using a VDTA and one OTA as ABB [18], and an electronically tunable high-frequency meminductor based on single output OTA and differential voltage current conveyor, two capacitors, and a resistor [19]. Memristor-less meminductor emulators were proposed using VDTA, current differencing buffered amplifier (CDBA), and a grounded capacitor, working in both floating and grounded meminductor configurations [20].

Another proposed design included voltage differencing buffered amplifier (VDBA), a memristor, and a capacitor [21], while a different circuit utilized two OPAMPs, resistors, a memristor, and a capacitor [22] in 2022.

The latest developments from 2023 featured meminductor emulators utilizing VDBA, CDBA, a resistor, and two grounded capacitors, offering an easily adjustable design for grounded/floating decremental to incremental configurations [23]. A floating decremental/incremental meminductor emulator circuit used a voltage differencing gain amplifier with a current differencing buffered amplifier and two grounded capacitors [24]. Another realization involved an OTA, CCII, resistor, and capacitor [25]. A circuit using two operational transconductance amplifiers and two capacitors was also introduced [26]. Additionally, a current differencing transconductance amplifier (CDTA) based grounded meminductor emulator circuit was proposed, comprising only a single type of active block (CDTA) and simple circuitry with two grounded capacitors, eliminating the need for an analog multiplier, adder, memristor, or any other complex circuit [27].

In contrast to traditional methods involving multipliers, adders, subtractors, and other analog circuits that result in complex and bulky circuitry. This paper proposes a novel approach to designing a meminductor emulator using a simple circuit comprising two VDDDA ABBs, a memristor, and a grounded capacitor as a solution to the challenge.

This approach yields a compact and straightforward meminductor design, making it well-suited for low-voltage applications with satisfactory performance across a wide range of frequencies, from 750 Hz to 5.5 kHz. Additionally, the emulator can be electronically tunable, offering the flexibility to adjust the nonlinear flux control by tuning the bias current through the circuit.

The paper aims to create a lossless meminductor

emulator circuit that mimics the behaviour of meminductor. Furthermore, the newly designed meminductor is applied in the development of a chaotic oscillator to assess the emulator's performance. Simulation results were obtained using the LTspice tool, which confirmed the presence of a pinched hysteresis loop and validated the proposed concept.

This paper is structured as follows: Sect.1. introduction, Sect.2. offers review of mem-elements. Sect.3. VDDDA and its properties are discussed, followed by Sect.4. which presents the design and analysis of the proposed meminductor. Sect.5. includes the simulation results of the proposed meminductor, covering meminductive behaviour, non-volatility, capacitive tuning, supply and bias voltage variations, temperature variations, and Monte Carlo analysis. Sect.6. offers a detailed comparison of the proposed meminductor with emulators in the literature. In Sect.7. a chaotic oscillator is designed using the proposed floating meminductor to demonstrate the performance of the meminductor circuit. Finally, Sect.8. draws conclusions.

2 Basic Review of Mem-elements

The memristor, memcapacitor, and meminductor fall within the category of mem-elements. Memristor provides a relation between flux (ϕ) and charge (q), where flux is the time integral of the applied voltage $V(t)$, whereas charge, q, is the time integral of the current $I(t)$ that can be represented as:

$$M(q) = \frac{\frac{d\phi}{dt}}{\frac{dq}{dt}} = \frac{V(t)}{I(t)} \quad (1)$$

which can be rewritten as

$$V(t) = M_R \cdot I(t) \quad (2)$$

Similar to memristor, the non-linear relationship of meminductor and memcapacitor can be shown as:

$$L(q) = \frac{d\rho(q)}{dq} \quad (3)$$

which can be rewritten as

$$\rho(t) = \int_{-\infty}^{t} \varphi(t)\, dt \quad (4)$$

$$d\rho = M_L \cdot dq \quad (5)$$

where M_L is the meminductance of the system. And for memcapacitor:

$$C(\emptyset) = \frac{d\sigma(\emptyset)}{d\emptyset} \quad (6)$$

which can be rewritten as

$$\sigma(t) = \int_{-\infty}^{t} q(t)\, dt \quad (7)$$

$$d\sigma = M_c \,.\, d\phi \quad (8)$$

where M_C is the memcapacitance of the system.

Therefore, pinched hysteresis curves for mem-elements can be obtained between the fundamental quantities, i.e., flux (ϕ), charge (q), voltage (v), and current (i). Hence, the distinctive memory characteristic associated with memristive systems can now be readily inferred in capacitive and inductive systems, rendering them inherently memcapacitive and meminductive [28].

3 VDDDA and Its Properties

The voltage differencing differential difference amplifier (VDDDA) is described as a six-terminal analog ABB, as elucidated in [29]. Comprising an OTA cascaded with a voltage differential difference amplifier (DDA), the VDDDA emerges as a crucial active element for designing analog voltage-mode circuits. Its unique construction obviates the need for additional voltage addition or subtraction components. The VDDDA-based circuits exhibit high impedance at input voltage terminals and low impedance at the output voltage terminal, enabling seamless cascading without requiring supplementary voltage buffers, as expounded in [30].

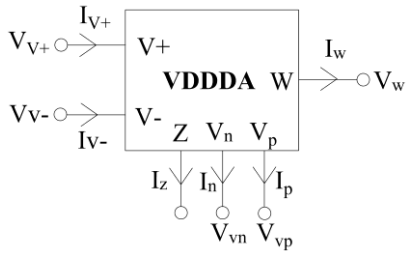


Fig. 2 Symbolic notation of VDDDA

Fig. 2 and Fig. 3 illustrates the schematic symbol and equivalent CMOS circuit of the VDDDA respectively.

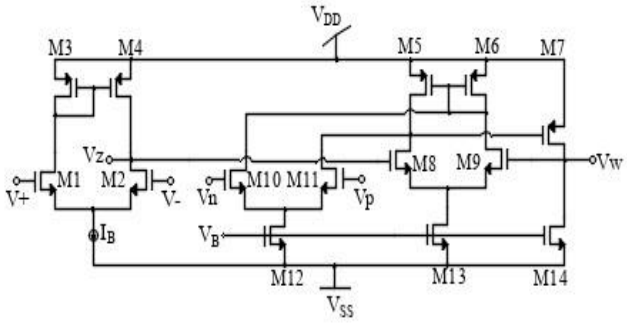


Fig. 3 CMOS implementation of VDDDA

In its ideal state, the VDDDA demonstrates no input current at the input voltage terminals V_{v+}, V_{v-}, V_{vn}, and V_{vp}, indicating high impedance at these nodes. The disparity in the inverting input voltage transforms into output current at the high-impedance z terminal through transconductance gain (gm). Typically, the transconductance gain is modulated by an external DC bias voltage (V_B). The voltage at the low-impedance w terminal reflects the difference and addition of the voltages at terminals z, vn, and vp.

The ideal and non-ideal electrical relationships between the input and output terminals of the VDDDA are elucidated by the hybrid matrix, detailed below.

$$\begin{bmatrix} Iv+ \\ Iv- \\ Iz \\ In \\ Ip \\ Vw \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ gm & -gm & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} Vv+ \\ Vv- \\ Vz \\ Vvn \\ Vvp \\ Iw \end{bmatrix}$$

In this design, the terminal voltages are constrained to ±200mV for the OTA and -0.50V to +0.25V for the differential difference stage, with V_{DD} and V_{SS} set at 0.9V and -0.9V respectively, and V_B = −0.35V. The transistors in the design are modelled using the TSMC 0.18μm level-49 CMOS process, with specific parameters (VTH_n = 0.3725327V, μ_n = 259.5304 cm2/(V.s), VTH_p = −0.3823437V, μ_p = 109.4682 cm2/(V.s), T_{ox} = 4.1nm). The updated designed VDDDA aspect ratios are provided in Table 1.

Table 1 Aspect ratios of MOSFETs used in the design of VDDDA

NMOS transistors	W(µm)/L(µm)
M1,M2	9/1.08
M8-M11	0.72/1.08
M12-M14	2.16/1.08
PMOS transistors	W(µm)/L(µm)
M3,M4	3.96/1.08
M5-M7	3.6/0.18

4 Proposed Meminductor Emulator

The meminductor emulator circuit proposed in this study comprises two cascaded VDDDA ABBs, a memristor, and a grounded capacitor, as illustrated in Fig. 4.

The difference in the inverted input voltage is transformed into an output current at the high impedance z terminal through transconductance gain (gm). Both VDDDA's exhibit the same transconductance, gm. Consequently, the magnitudes of currents at the first port (I_{z1}) and second port (I_{z2}) are equal but flow in opposite directions. The meminductor's two input ports are designated as V_1 and V_2. Applying voltages to both terminals transform the circuit into a floating meminductor while applying voltage to one terminal and grounding the other results in a grounded meminductor. This circuit offers the capability to simulate floating meminductor with electronic controllability.

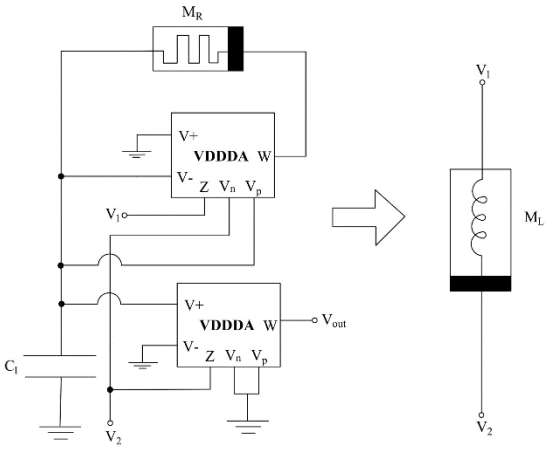


Fig. 4 Proposed Floating Meminductor

In the proposed design, a capacitor is utilized alongside a memristor.

This adjustment is particularly advantageous for the applications in integrated circuits, contributing to the overall compactness of the circuit due to the small size of the memristor. Additionally, the suggested floating meminductor has the capability to retain its state, allowing it to function as a mem-element, providing flexibility for use in devices that require both memory and a compact design.

4.1 Analysis of the Proposed Meminductor Emulator

The meminductor emulator circuit (Fig. 4) routine analysis yields the following equations:

$$I_1 = g_m (V_{v+} - V_{v-}) \quad (9)$$

$$I_1 = g_m (0 - V_{v-}) \quad (10)$$

We know, that the current I_1 at the port is determined by the product of the transconductance, gm, and the voltage difference across the ports.

$$V_{v-} = (V_w - V_{v-}) \frac{1}{sCM_R} \quad (11)$$

$$V_{v-} = \frac{1}{sCM_R} (V_z - V_{vn} + V_{vp} - V_{v-}) \quad (12)$$

$$V_{v-} = \frac{1}{SCM_R} (V_1 - V_2) \quad (13)$$

also, from the circuit, the voltage V_w can be represented as

$$V_w = V_z - V_{vn} + V_{vp} \quad (14)$$

From (10) and (13),

$$\phi(t) = \frac{CM_R I_1}{g_m} \quad (15)$$

We know that the mem-inductance equation is:

$$\phi_L(t) = M_L \cdot I(t) \quad (16)$$

Comparing (15) and (16),

$$\phi_L(t) = \frac{CM_R}{g_m} \cdot I_1 \quad (17)$$

where, meminductance M_L is deduced as:

$$L_{eq} = \frac{CM_R}{g_m} \quad (18)$$

Further analyses using SPICE model of HP memristor. The memristance of the HP memristor is given as:

$$M_R = R_{ON} \cdot x(t) + R_{OFF} \cdot (1 - x(t)) \quad (19)$$

where R_{OFF} and R_{ON} are the equivalent resistances of the HP memristor when it is undoped and doped, respectively

$$M_L = \frac{C_1 \cdot R_{OFF}}{gm} + \frac{C_1 \cdot (R_{ON} - R_{OFF}) \cdot x(t)}{g_m} \quad (20)$$

From Eq. (20), it is inferred that the meminductance of the proposed meminductor emulator, designed utilizing HP memristor, can be partitioned into two components: fixed and variable. The fixed component is contingent upon the capacitor's value (C_1) and the off-resistance of the memristor (R_{OFF}). Conversely, the variable component is influenced by both the internal state, denoted as x(t), and the on-resistance and off-resistance (R_{ON} and R_{OFF}) of the HP memristor.

5 Simulated Results of Proposed Meminductor Emulator

The floating meminductor emulator illustrated in Fig. 4 underwent simulation in the LTspice tool, utilizing the SPICE model of an HP memristor. The CMOS-based VDDDA, depicted in Fig. 3, was employed and simulated using 180nm CMOS technology parameters. Table 1 provides details on the aspect ratios of MOSFETs utilized in the circuit diagrams of VDDDA. The emulator, implemented with two VDDDA, a 0.5nF capacitor, and a memristor, operated with a power supply set at ±0.9V, with aspect ratios detailed in Table 1.

Careful consideration should be given to the selection of Rinitial, Ron, and Roff values for the memristor to ensure accurate and predictable behaviour. In this context, the chosen values for Rinit, Ron, and Roff in the memristor are 13K, 100K, and 16K respectively.

The proposed meminductor offers an inductance value of 29.5mH, enhancing the compactness and reliability of the circuit, especially significant in analog circuitry, where the performance, sizing, and flexibility of each element play vital roles. The simulation analysis indicates a power consumption of 76.369uW.

This significance is particularly pronounced when dealing with complex analog circuitry, especially in the development of integrated circuits tailored for low-power applications.

5.1 Non-volatility Test

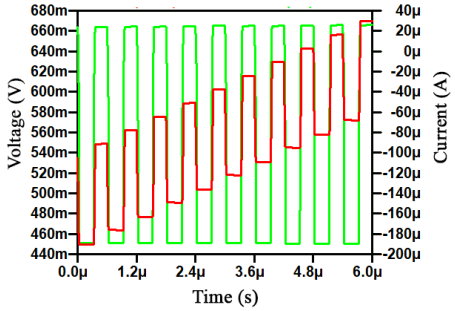


Fig. 5 Non-volatile behaviour of proposed meminductor emulator

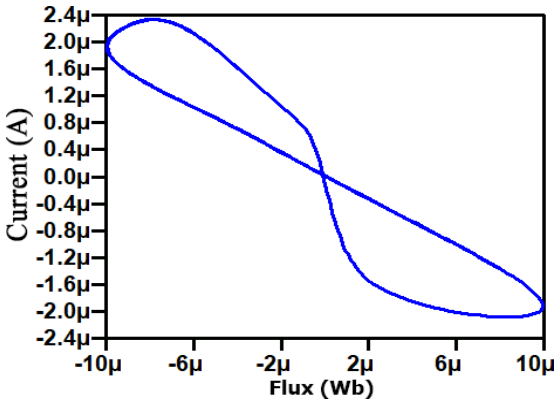
The non-volatility test demonstrates the mem-elements ability to retain its previous value, even when in the off state, making it suitable for use as a memory-based device. To confirm this property in the proposed meminductor emulator, the voltage across the memristor is monitored during input current application using the SPICE model of the HP memristor.

In this test, a pulse signal with a 1.5V amplitude and 300 ns "ON" time, operating at a total period of 600 ns (equivalent to a frequency of 1.6 MHz), is applied. Rin and Roff are set at 1K and 11K, respectively. The flux ($\phi = \int V_{in} dt$) was measured at the input terminal, and meminductance is obtained by dividing the flux (ϕ) by the input current (I_{in}). Fig. 5 illustrates simulation plots showing both meminductance and the pulse input (V_{in}), confirming the successful verification of non-volatility.

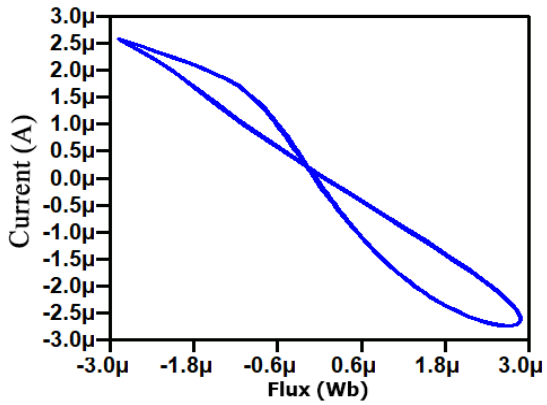
Fig. 5 also demonstrates memory persistence, where the meminductance value recorded during the "on" phase of the input pulse is maintained throughout the corresponding "off" phase. It starts to increase again from the retained level at the beginning of the next "on" phase until the end of the subsequent "off" phase, affirming the memory retention characteristic of the proposed meminductor emulator.

5.2 Meminductive Behaviour

The upcoming section will explore the behaviour of the proposed meminductor model across the frequency ranges where it operates effectively, as well as the limiting frequency beyond which its performance degrades. This analysis will shed light on the operational boundaries of the meminductor in both floating and grounded configurations.



(a) Frequency at 1.6kHz



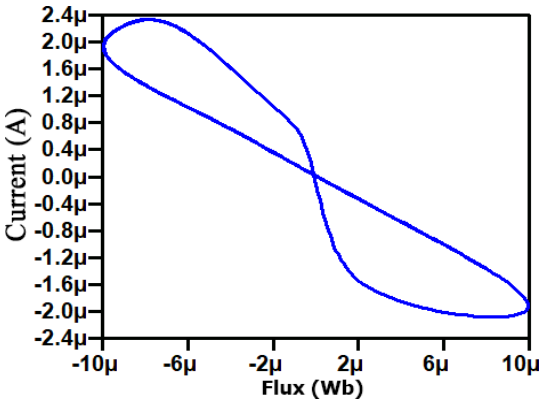
(b) Frequency at 5.5kHz

Fig. 6 Pinched hysteresis loops for proposed meminductor emulator (a)1.6 kHz and (b)5.5 kHz

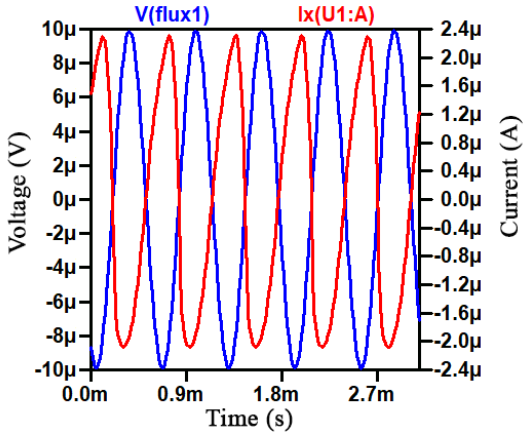
Fig. 6(a) and 6(b) provide simulation results for frequencies of 1.6kHz, and 5.5kHz respectively. The bandwidth of the proposed meminductor emulator closely approaches 5.5kHz, as illustrated in the frequency curves in Fig. 6. The pinched hysteresis loop diminishes as the frequency increases. Beyond 5.5kHz, pinched hysteresis loops were not obtained, and at 6kHz, it becomes evident that the circuit no longer functions as a meminductive circuit.

For the proposed meminductor emulator, the pinched hysteresis loop was observed at a frequency of 1.6kHz. Fig. 7 and Fig. 8 present the pinched hysteresis loops and transient response for the proposed meminductor emulator in floating and grounded configurations respectively.

Pinched hysteresis curves between flux and current are portrayed in Fig. 7(a) and 8(a), while sinusoidal waveforms of flux and input current are showcased over time in Fig. 7(b) and 8(b) for the proposed meminductor emulator circuit illustrated in Fig. 4, where the voltage leads the current waveform, showcasing a 90-degree phase shift, thereby indicating that the proposed emulator effectively emulates the functionality of a traditional inductor.



(a) Pinched hysteresis loop for Proposed meminductor inductor emulator in floating configuration



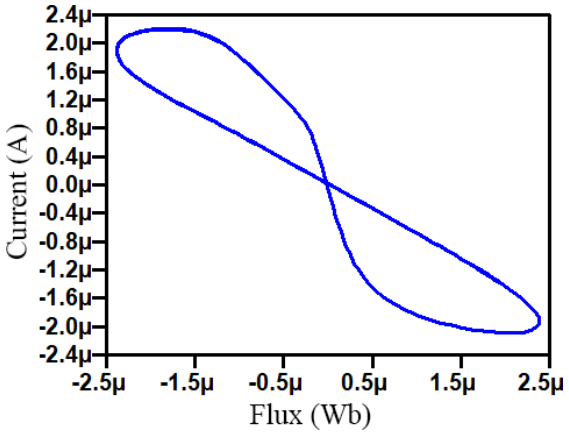
(b) Transient analysis for Proposed meminductor inductor emulator in floating configuration

Fig. 7 Proposed floating meminductor emulator analysis

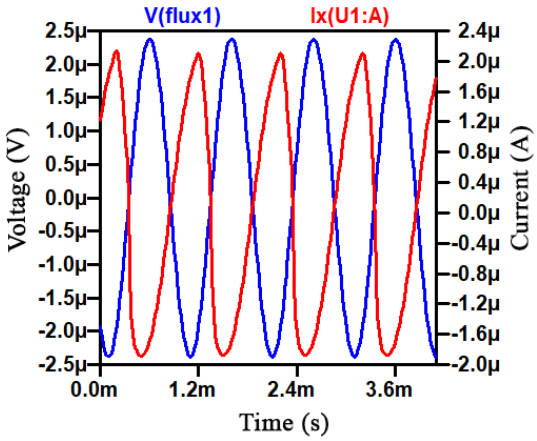
The acquired pinched hysteresis loops further validate the robustness of our design.

Simulations of the proposed meminductor, designed using VDDDA, included applying sinusoidal voltages with amplitudes of 75mV and 100mV at V_1 and V_2, respectively, in a floating configuration.

In grounded configurations, there may be a difference in amplitudes of approximately 64mV between V_1 and V_2, respectively, at a frequency of 1.6 kHz. The pinched hysteresis loop was plotted between voltages (V_1) and (V_2) and the current (I_{MR}) with varying frequencies from hertz to several hundreds of kilohertz, confirming the satisfactory performance of the proposed meminductor emulator across a range of frequencies.



(a) Pinched hysteresis loop for Proposed meminductor emulator in grounded configuration



(b) Transient analysis for Proposed meminductor emulator in grounded configuration

Fig. 8 Grounded meminductor emulator analysis, when V_1 is grounded

5.3 Capacitive Tuning

The desired characteristic for applications involving capacitive tuning lies in the variations of the phase response of the meminductor corresponding to different capacitance values. To explore the impact of varying capacitor values, simulations were conducted on the proposed meminductor emulator using sinusoidal signals with a variation of 25mV at 1.6 kHz.

The pinched hysteresis loop curves were observed for C_1 across the range of 1pF to 10nF, as illustrated in Fig.

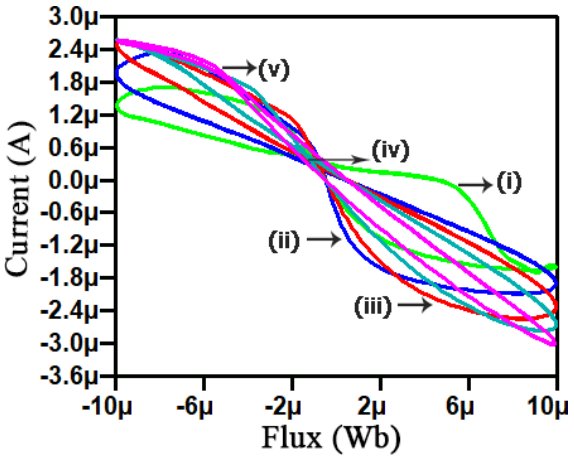


Fig. 9 Pinched hysteresis loop curves of proposed meminductor emulator with C1 varying (i) 1pF (ii) 10pF (iii) 0.5nF (iv) 1nF (v) 10nF

9 from (i) to (v) for values of 1pF, 10pF, 0.5nF, 1nF, and 10nF, respectively.

The subtle changes in the pinched hysteresis loop curves serve as confirmation of the capacitive tuning feature inherent in the suggested meminductor, showcasing its performance variability.

Analysing the plotted graph reveals that as capacitance values increase, the graph contracts, resulting in a reduction of the phase loop area. Concurrently, the current range associated with each loop expands, enhancing the reliability of the system by providing a broader operating current range.

The observed pattern in the pinched hysteresis loop curves illustrates how the circuit's characteristics vary and depend on the capacitance employed in the proposed meminductor emulator.

5.4 Voltage Supply variation analysis

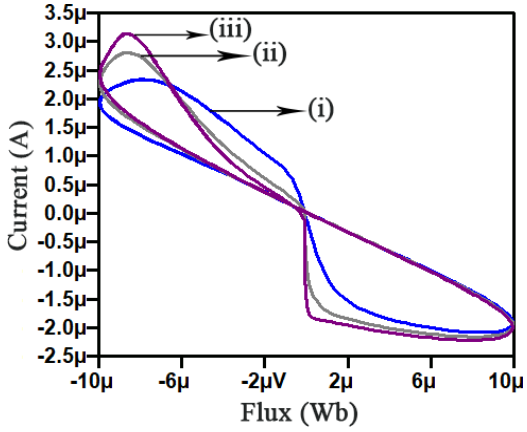


Fig. 10 Pinched hysteresis loop curves of proposed meminductor emulator with supply varying (i) 0.9V (ii) 0.95V (iii) 1V

As the voltage supplied increases, the hysteresis loops exhibit greater uniformity and systematic characteristics

contrasting with lower supply voltages where the loops tend to be more asymmetrical in shape, as illustrated in Fig. 10.

Consequently, opting for a moderate power supply allows for the attainment of symmetrical loops, providing a desirable foundation for our design work. This choice facilitates the creation of designs suitable for low-voltage power applications, ensuring effective functionality.

5.5 Varying bias voltage

In order to examine the pinched hysteresis loops under varying bias voltages, we adjusted the bias voltage within the range of -0.5V to 0.3V. As the bias voltage increases from -0.5V to 0.3V, the current peaks diminish, as depicted in Fig. 11 (i)-(v) sequentially.

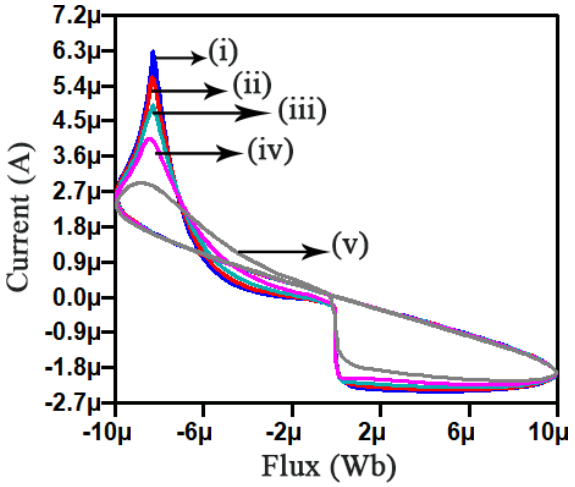


Fig. 11 Pinched hysteresis loop curves of proposed meminductor emulator with a varying bias voltage (i) -0.5V (ii) -0.3V (iii) -0.1V (iv) 0.1V (v) 0.3V

This demonstrates the adaptable characteristic of the proposed meminductor emulator, showcasing its responsiveness to externally controlled bias voltage variations.

The resulting pinched hysteresis loops confirm the electronic tunable capability of the proposed meminductor emulators. Fig. 11 clearly illustrates the variation in pinched hysteresis loops while maintaining their appropriate shapes and pinched points across different bias voltages.

5.6 Temperature variation analysis

As temperature decreases, hysteresis loops display reduced uniformity and systematic characteristics, unlike at room temperature, where the loops tend to be more symmetrical in shape, as depicted in Fig. 12.

Therefore, maintaining a moderate room temperature enables the achievement of symmetrical loops, offering a favourable basis for our design. This decision facilitates the development of designs adaptable to temperature fluctuations, ensuring reliable functionality despite varying environmental conditions, thus ensuring stable operation of the circuit in extreme environments.

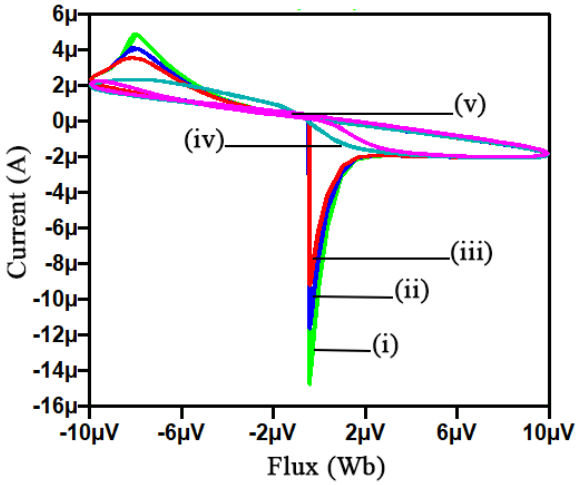


Fig. 12 Pinched hysteresis loop curves of proposed meminductor emulator with temperature variations (i) -25°C (ii) -10°C (iii) 0°C (iv) 27°C (v) 35°C

5.7 Monte Carlo analysis

Depicted in Fig. 13, the Monte Carlo analysis comprises 200 iterations, considering a 10 percent tolerance in capacitance, which directly impacts the pinched hysteresis loop. The proposed meminductor's design sensitivity relies on capacitor values within this specified range.

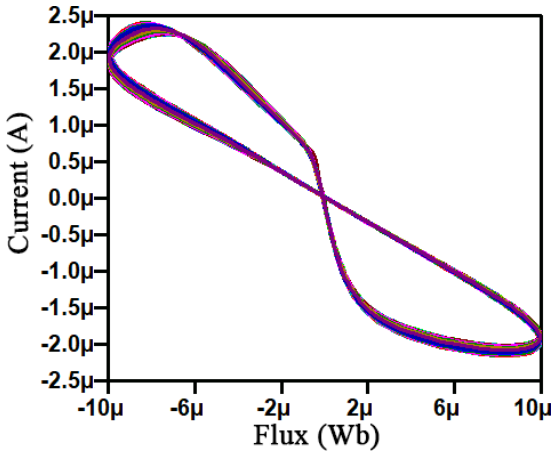


Fig. 13 Monte Carlo analysis of proposed meminductor emulator

The pinched hysteresis loop is intricately shaped by this range of capacitance. This analysis serves to confirm the system's tolerance across a spectrum of values, demonstrating consistency through the alignment and tracing of the initial pinched hysteresis loop of the proposed meminductor, as initially presented in Fig. 7(a).

6 Comparison of Proposed Emulator with Reported Emulators in the Literature

Table 2 presents a comparative analysis between the newly proposed meminductor and previously existing meminductor emulators. This comparison aims to assess the superior performance of the proposed meminductor emulator in several aspects, including operating frequency, maximum frequency range, the count of active and passive components, grounded and floating configurations, electronic tunability as well as the presence or absence of a memristor component.

1. The meminductor emulator circuit proposed in this paper has been observed to operate within the frequency range of 700Hz to 5.5kHz. In contrast, meminductor emulator circuits described in the literature [2,9,16.31-36] predominantly function within the lower frequency range of Hz to kHz.

2. While the meminductor emulators found in the literature [2,9,16,32,34-35,37] utilize a more extensive array of active and passive components, the emulator model introduced in this paper relies solely on two active VDDDA blocks along with two passive components, namely a memristor and a capacitor.

3. The meminductor emulator circuit proposed in this paper has been designed using two VDDDA blocks, a memristor, and a single capacitor. In contrast, emulator circuits in the literature [2,9,16,34] employ multiple resistors, capacitors, and current conveyors, contributing to their bulkiness and high cost in practical implementation.

4. The meminductor emulator presented in this paper distinguishes itself by avoiding the use of analog multipliers and adders, resulting in a simpler design with fewer components. In contrast, emulators reported in the literature [2,916,32,34-35,37] incorporate multipliers and adders [9,31], leading to increased circuit complexity and practical challenges.

5. The meminductor emulator presented in this work operates in both floating and grounded inductor configurations. In contrast, the designs detailed in the literature function solely as grounded [2,9,31-33] or floating inductors [34-37] with no flexibility to switch between the two.

6. The proposed meminductor is electronically tunable, allowing for easy adjustment of inductance without the need to alter the circuit topology when adapting to different inductance requirements. On the other hand, emulators featured in the literature [35] lack electronic tunability, restricting their utility to specific frequency ranges and applications, limiting their versatility.

7 Application of Proposed Meminductor Emulator in Chua's Oscillator Circuit

The configuration of the chaotic oscillator, as illustrated in Fig. 14, incorporates the proposed meminductor emulator from Fig. 4. Chua's oscillator is recognized as a straightforward circuit for generating chaotic waveforms [38].

Fig. 14 illustrates a simplified version of Chua's oscillator, featuring the proposed meminductor M_L, two resistors (R, Ro), two capacitors (C_1, C_2), and an inductor (L).

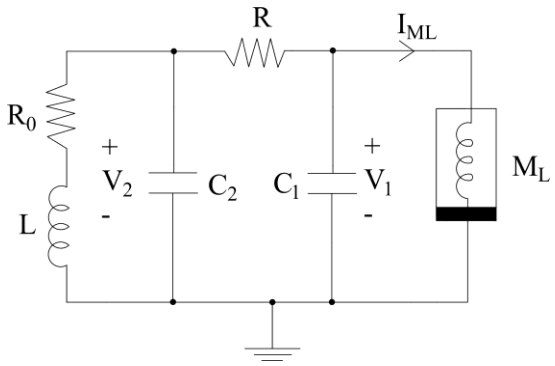


Fig. 14 Chaotic oscillator circuit using proposed meminductor

Addressing the sensitivity of the chaotic oscillator to changes in circuit element values, various projection plots can be generated for different sets of circuit element values. An active element is crucial to infuse energy into an otherwise dissipative system, facilitating self-excited oscillations—a role fulfilled by the proposed meminductor emulator.

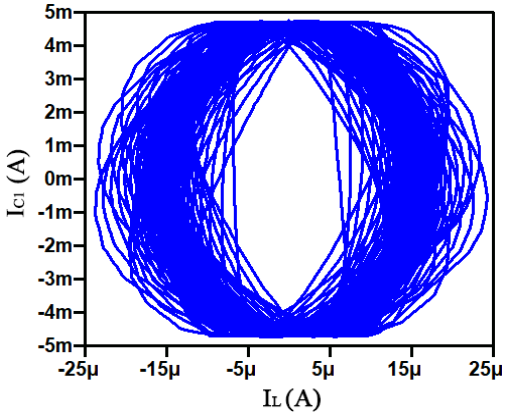
The parameters for the chaotic oscillator, Fig. 14, constructed using grounded meminductor configurations depicted from Fig. 4, are selected as follows: Ro = 651 $\mu\Omega$, R = 12 kΩ, L =7.5 μH, C_1 = 10 nF, C_2 = 2 nF and illustrated in Fig. 15.

In contrast, the values for the chaotic oscillator created with the suggested floating meminductor are as follows: Ro = 651 $\mu\Omega$, R = 1 kΩ, L =7.5 μH, C_1 = 0.06 nF, C_2 = 10 nF with their respective two-dimension plots presented in Fig. 16.

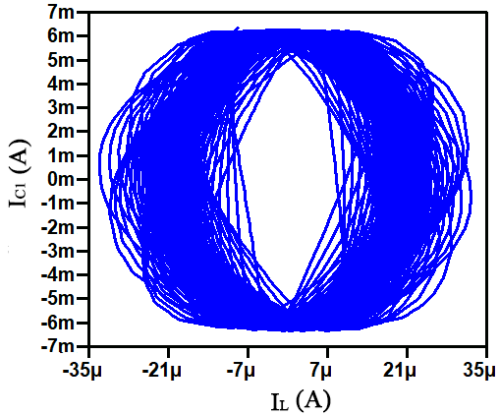
The compact nature of a memristor, operating at the nanoscale level, is a significant advantage, prompting the exploitation of this property. The chaotic oscillator designed with the proposed meminductor circuit with Chua's configuration finds application in encrypted communication, random generation, and spike generation.

Table 2 Comparison between the proposed emulator and already existing emulator. Abbreviations used are: OTA: Operational Transconductance Amplifier, MO-OTA: Multi-Output Operational Transconductance Amplifier, CFOA: Current Feedback Operational Amplifier, CCII: Current Conveyor-II, CBTA: Current Backward Transconductance Amplifier, OP-AMP: Operational Amplifier, MR: Memristor, VDDDA: Voltage Differencing Differential Difference Amplifier, R: Resistor, C: Capacitor.

Reference	Active Elements	Passive Elements	Power Supply	Operating Frequency	Floating /Grounded	Memristor-less	Electronically Tunable
[2]	4OP-AMP, 2CCII, 1Multiplier	2C,7R	±5V	800 Hz	Grounded	No	Yes
[9]	3CCII, 1Multiplier, 1 Adder	2C,3R	±5V	10 Hz	Grounded	Yes	Yes
[16]	1OTA,1 Multiplier, 2CCII, 1CFOA	2C,7R	±15V	5 kHz	Both	Yes	Yes
[31]	1Subtractor, 1 Adder	1C,1R	±1.25 V	40 Hz	Grounded	No	Yes
[32]	5OP-AMP, 1Multiplier	10R, 2C	-	70 Hz	Grounded	No	Yes
[33]	1OTA, 1voltage reference	1L, 1R, 1C	-	500 Hz	Grounded	Yes	Yes
[34]	2CCII or 1 CCII and 1OTA, 1Multiplier	1R, 3C or 3C	±20V	2 kHz	Floating	Yes	Yes
[35]	9OP-AMPs, 11 Multipliers	26R	-	140 Hz	Floating	Yes	No
[36]	1CBTA	1C	-	200 Hz	Floating	No	Yes
[37]	1OTA, 1MO-OTA, 1Multiplier	1R, 2C	±1.25V	1 MHz	Floating	Yes	Yes
Proposed	**2VDDDA**	**1C, 1M_R**	**±0.9V**	**750 Hz - 5.5 KHz**	**Both**	**No**	**Yes**



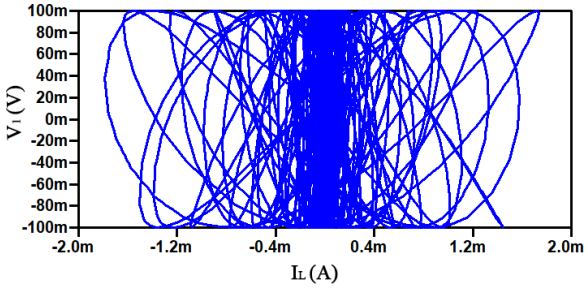
(a) When supply at V_z



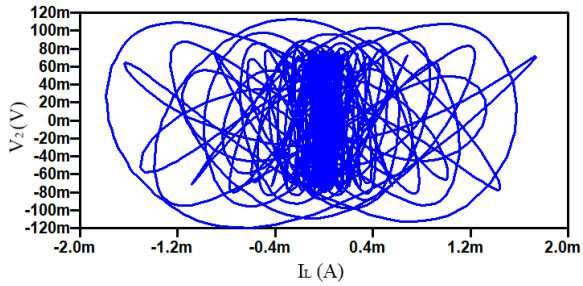
(b) When supply at V_{z2}

Fig. 15 I_L vs I_{C2} plots of chaotic oscillator generated from grounded meminductor configurations

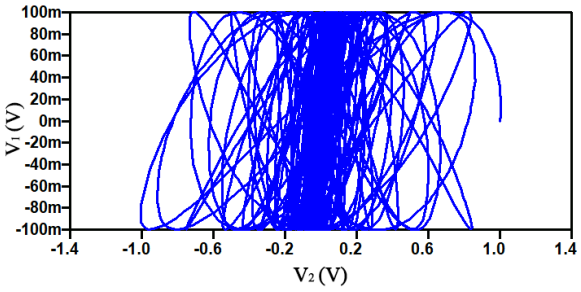
Two-dimensional projection plots between inductor and capacitor current in Fig. 15, also plots between voltages across C_1 and C_2 and inductor current I_L presented in Fig. 16 prove the circuit's chaotic nature. The observed randomness in these curves substantiates the circuit's suitability for applications prioritizing encryption, randomness, and unpredictability.



(a) I_L vs V_1



(b) I_L vs V_2



(c) V_1 vs V_2

Fig. 16 Graphs generated by the chaotic oscillator across various variables

8 Conclusion

In this study, we have introduced a meminductor emulator, available in both grounded and floating configurations, crafted using two VDDDA blocks, a memristor, and a capacitor. Comprehensive comparative evaluations with various previously reported emulators underscore the distinctive qualities of our proposed design. The proposed meminductor emulator have demonstrated robust performance, effectively supporting frequencies up to 5.5 kHz. The incorporation of CMOS technology in the internal structure of the introduced active block renders it well-suited for applications requiring electronic control.

The advantages of our proposed emulator include a straightforward design and adaptability for both grounded and floating configurations. Key benefits encompass simplicity, versatility, a reduced number of active and passive components, support for both grounded and floating modes, an extended operating frequency range in the kHz range, electrical tunability via bias voltage, and the ability to fine-tune pinched hysteresis loop by adjusting the transconductance (gm) parameter of the voltage differencing gain amplifier. Additionally, the emulator is suitable for monolithic IC fabrication. The uncomplicated circuitry enables seamless integration with other systems, potentially expanding the application possibilities in the future. Simulation analyses have been provided to elucidate the underlying operational principles and confirm the satisfactory performance of our proposed meminductor

emulator. To further validate its effectiveness, the designed emulator has been practically applied in chaotic oscillator applications, providing real-world validation of their performance.

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

First Author's Name: Chhaya Belwal

1) Data Curation
2) Software and Simulation
3) Original Draft Preparation

Second Author's Name: Kunwar Singh

1) Methodology

Third Author's Name: Shireesh Kumar Rai

1) Idea & Conceptualization
2) Revision & Editing

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Informed Consent Statement

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