

Cancellation of Series-Loss Resistance in UWB Active Inductors using RC Feedback

M. Rafei* and M. R. Mosavi*

Abstract: One of the most important features of the Active Inductors (AIs) is their input equivalent resistance, namely series-loss resistance, which should be low enough to have a high Quality Factor (QF). Most of the previous methods by this goal did not yield a high enough QF. This paper presents a new method, namely applying an RC feedback, to cancel series-loss resistance entirely. As the RC feedback cancels series-loss resistance, it enhances the Self-Resonant Frequency (SRF) as well. The SRF of the AI has a range as high as 0.25-12.5 GHz. Compared to the previous reports, the QF has been improved by applying the RC feedback. The structure is such that the QF can be adjusted independent of the SRF. For example, a very high quality factor of 13159 at the frequency of 6.6 GHz with a 2.2 nH inductance is obtained, while noise voltage and power dissipation are less than 4.6 nV/ $\sqrt{\text{Hz}}$ and 4 mW, respectively. The AI is designed and simulated using 90 nm CMOS process and 1.2 V power supply. To the best of authors' knowledge, this is the first time an RC feedback has been implemented to cancel series-loss resistance.

Keywords: Active Inductor, High Quality Factor, Low Power Consumption, RC Feedback, Single-Ended, Zero Series-loss Resistance.

1 Introduction

In 2002, Federal Communications Commission (FCC) approved unlicensed use of Ultra-Wideband (UWB) spectrum in the range of 3.1 GHz to 10.6 GHz. Therefore, UWB range attracted attention of many researchers especially to wireless systems. Most analog Radio Frequency (RF) designers make use of on-chip Passive Inductors (PIs) in their circuits. PIs exhibit low Quality Factor (QF) and dominate the die area of the chip [1]. In contrast, some others benefit from Active Inductors (AIs) that have higher inductances and QFs with less required chip area. However, AIs introduce higher noise and consume more power than PIs [2, 3].

AIs are categorized into two major structures: Single-Ended AIs (SEAIs) and Differential AIs (DAIs). SEAIs are utilized in applications such as filters and amplifiers, and DAIs in oscillators [4-6]. In comparison with on-chip PIs that have a fixed Self-Resonant Frequency (SRF), AIs benefit from a tunable SRF. To the best of authors' knowledge, the best-reported SRF Range (SRFR) is 10.7 GHz with the QF of 3000,

however the designed circuit suffers from power consumption [7]. Therefore, the main issues in the design of the AIs that one might encounters are high power consumption [7], low QF [3], and SRFR typically lower than 5 GHz [8, 9].

Some AIs benefit from cross-coupled structure. Due to the negative equivalent resistance at the output of this structure, equivalent series-loss resistance at the input node of such AIs decreases [2, 3, 10]. Recently, to increase the inductance of the AI, a feedback resistor has been used in both SEAI and DAI [3, 8]. However, these structures do not give a high quality factor since the addition of the feedback resistance does not result in a low series-loss resistance. In addition, in these works the SRFR is actually less than 5 GHz.

In this paper, we apply an RC feedback to the well-known cascode structure. As a result, a negative term is added to the series-loss resistance equation, and hence results in the cancellation of its effect. The AI circuit is designed and simulated with the TSMC 90 nm 1P9M RF CMOS process. The utilized simulator is HSPICE. The second section describes the circuit structure, which is a single-ended one. Relations governing the circuit are extracted in each part and simulation results confirm these relations. Finally, the third section will be devoted to the conclusion.

Iranian Journal of Electrical & Electronic Engineering, 2012.

Paper first received 21 Nov. 2011 and in revised from 22 Feb. 2012.

*The Authors are with the Department of Electrical Engineering, Iran University of Science and Technology, Narmak, Tehran 16846-13114, Iran.

E-mails: rafei@elec.iust.ac.ir, m_mosavi@iust.ac.ir.

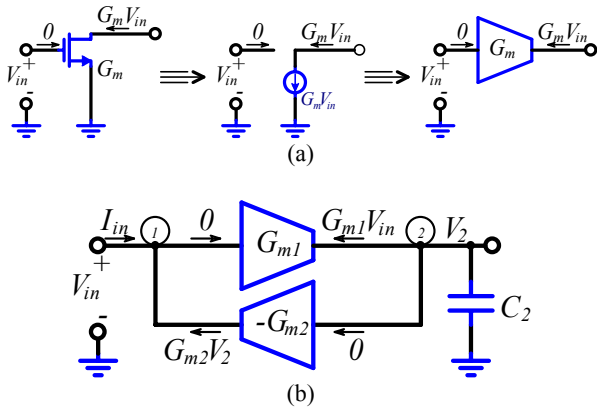


Fig. 1 (a) NMOS as an OTA, (b) Gyrator-C basic idea with ideal OTAs.

2 Investigation of the Active Inductor Structure

In this section, after the explanation of the basic theory of the AI, we will discuss the new series-loss resistance cancelling method, i.e. applying the local RC feedback.

2.1 Basic Concepts

The main idea of the AI, known as gyrator-C, has been depicted in Fig. 1 [11]. As can be seen, gyrator-C is based on Operational Transconductance Amplifiers (OTAs) whose electrical characteristics emulate a voltage controlled current source. The NMOS as an OTA is shown in Fig. 1(a) schematically. In the gyrator-C of Fig. 1(b), transconductance of the forward path is G_{m1} and the transconductance of the backward path is $-G_{m2}$, which is in the opposite sign of G_{m1} and maybe different in value. Assume that ideal OTAs are applied, the following analysis proves the main gyrator-C idea:

$$\begin{cases} V_2 = -G_{m1} V_{in} \frac{1}{sC_2} \\ I_{in} = -G_{m2} V_2 \end{cases} \quad (1)$$

Therefore, input impedance can be derived as:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sC_2}{G_{m1} \cdot G_{m2}} \Rightarrow L_{eq} = \frac{C_2}{G_{m1} \cdot G_{m2}} \quad (2)$$

To have a pure inductance at the input node, the phase of the input node's impedance should be exactly 90 degrees. However, in practice, resistance at the second node is limited and causes the reduction of the input impedance phase. Accordingly, if we can somehow adjust the phase, then we will be able to set the input resistance to zero. According to [11] the condition for stability of the circuit is $G_{m1} > G_{m2}$.

2.2 Proposed Active Inductor

Fig. 2 shows the proposed cascode structure of the AI with local RC feedback. Transistors M_1 and M_2 create G_{m1} of Fig. 1(b) and transistor M_3 creates G_{m2} of Fig. 1(b). Transistors M_{B1} to M_{B4} provide bias currents.

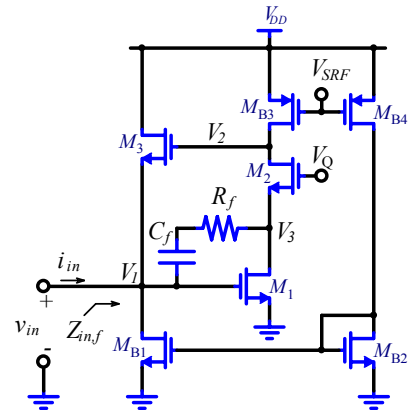


Fig. 2 Schematic of the proposed AI circuit.

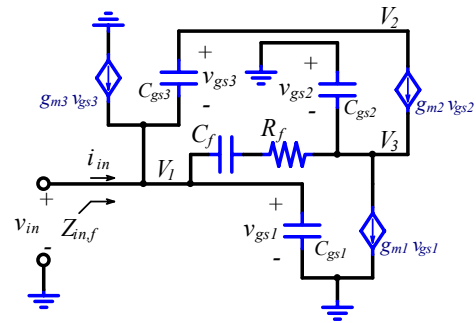


Fig. 3 Small-signal equivalent circuit of the proposed AI.

To verify the input impedance, Fig. 3 has depicted simplified small-signal model of the proposed AI. In this figure, C_{gsi} and g_{mi} are gate-source capacitance and transconductance of the i -th transistor, respectively. Gate-source capacitance C_{gsi} of the non-bias transistors is in the order of some tens of femtofarads and the transconductance g_{mi} is in the order of some millisiemens. Therefore, the term $C_{gs}\omega$ is very smaller than g_m in the frequency range of 0.25-12.5 GHz. As a result, in the extraction of any relation from the proposed circuit, the terms consist of $C_{gs}\omega$ can be neglected in contrast to those consist of g_m . For example, the term $C_{gs2}C_{gs3}s^2 + g_{m2}C_{gs3}s$ is equal to $g_{m2}C_{gs3}s$, since the term $C_{gs2}C_{gs3}s^2$ is very smaller than the term $g_{m2}C_{gs3}s$. By considering this note, input admittance of the circuit of Fig. 3, regardless of R_f and C_f , are obtained as follows:

$$Y_{in} = \frac{1}{Z_{in}} = \frac{g_{m1}g_{m3}}{C_{gs3}s} + g_{m1} + C_{gs1}s \quad (3)$$

The derivation of the Eq. (3) is described in details in the Appendix. Eq. (3) shows that the equivalent circuit of Fig. 2 without RC feedback is a parallel combination of an inductor, a capacitor, and a resistor, as seen in Fig. 4(a). The relations of these elements are as follows:

$$L_p = \frac{C_{gs3}}{g_{m1}g_{m3}}; R_p = \frac{1}{g_{m1}}; C_p = C_{gs1} \quad (4)$$

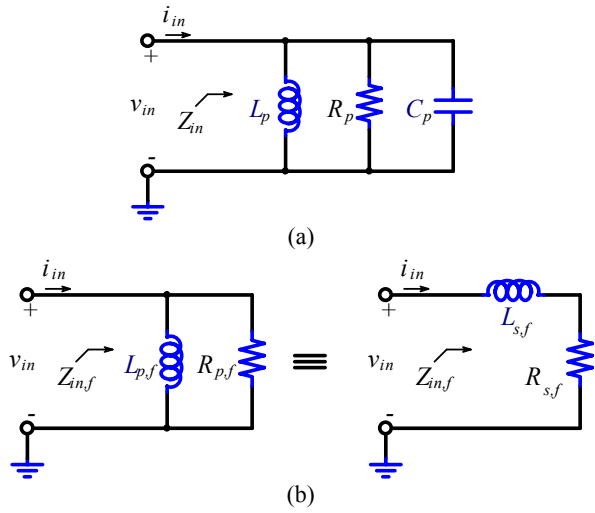


Fig. 4 Models of the proposed AI, (a) without RC feedback, (b) with RC feedback.

For the parallel RLC combination, if the condition $L_p C_p \omega^2 < 1$ is met, the phase of the input impedance will be between zero and 90 degrees. Therefore, following relation guarantees the inductance effect at the input node:

$$\frac{C_{gs3}}{g_{m1}g_{m3}} C_{gs1} \omega^2 < 1 \longrightarrow \omega^2 < \frac{g_{m1}g_{m3}}{C_{gs1}C_{gs3}} \quad (5)$$

The SRF, the frequency in which imaginary part of the input impedance or admittance becomes zero, in radian is as follows:

$$\omega_{osc} = \sqrt{\frac{g_{m1}g_{m3}}{C_{gs1}C_{gs3}}} \quad (6)$$

In practice, parasitic capacitances in nodes 1, 2, and 3 cause to increase of the value of C_{gs1} and C_{gs3} . To reduce input series-loss resistance and increase input inductance, the resistance and capacitance values in parallel combination model must be large and small, respectively. To adjust the phase of the input impedance, we apply a local RC feedback in the forward open loop including M_1 and M_2 . Considering the effect of local RC feedback, a good approximation of the input impedance for frequencies lower than the SRF, which is given in Eq. (6), is a parallel combination of a resistor and an inductor, which are calculated as follows:

$$Y_{in,f} = \frac{1}{Z_{in,f}} = \frac{C_{gs3}g_{m1} - C_f g_{m3}}{C_{gs3}} + \frac{g_{m1}g_{m3}}{C_{gs3}s} \quad (7)$$

$$= \frac{1}{R_{p,f}} + \frac{1}{jL_{p,f}\omega}$$

where subscript ‘‘f’’ denotes the circuit with local RC feedback and ‘‘p’’ denotes the parallel equivalent structure. The extraction of the Eq. (7) can be found in

the Appendix in details. This relation is established for small amounts of R_f of less than about 10 Ω . Therefore, the resistance R_f is not appeared in Eq. (7). Furthermore, the noise contribution of R_f in this range is negligible. As is specified in Eq. (7), the equivalent parallel resistance $R_{p,f}$ can be easily increased by adjusting $C_{gs3}g_{m1}$ close to $C_f g_{m3}$. As is shown in Fig. 4(b), the equivalent circuit of the AI with RC feedback is a parallel RL or a series RL model. Hence, Eq. (7) can be rewritten as:

$$Z_{in,f} = R_{s,f} + jX_{s,f} = \left(\frac{R_{p,f}L_{p,f}\omega}{R_{p,f}^2 + L_{p,f}^2\omega^2} \right) (L_{p,f}\omega + jR_{p,f}) \quad (8)$$

where

$$R_{s,f} = \left(\frac{R_{p,f}L_{p,f}\omega}{R_{p,f}^2 + L_{p,f}^2\omega^2} \right) (L_{p,f}\omega) = \frac{C_{gs3}\omega^2 (C_{gs3}g_{m1} - C_f g_{m3})}{(C_{gs3}g_{m1} - C_f g_{m3})^2 \omega^2 + (g_{m1}g_{m3})^2} \quad (9)$$

$$L_{s,f} = \left(\frac{R_{p,f}L_{p,f}\omega}{R_{p,f}^2 + L_{p,f}^2\omega^2} \right) (R_{p,f}) = \frac{C_{gs3}g_{m1}g_{m3}\omega}{(C_{gs3}g_{m1} - C_f g_{m3})^2 \omega^2 + (g_{m1}g_{m3})^2} \quad (10)$$

Adjusting g_{m1} and g_{m3} , and selecting C_f close to C_{gs3} , one can set input resistance to zero while maintaining stability, i.e. $g_{m1} + g_{m2} > g_{m3}$. In contrast to Eq. (3), local RC feedback has added a negative term to the input series-loss resistance that is $R_{s,f}$. The term $(g_{m1}g_{m3})^2$ in the denominator of the Eqs. (9) and (10) prevents it to become zero.

Equivalent series inductance and resistance at the input node in high frequencies are shown in Fig. 5, for both with and without RC feedback. The transistors sizes and bias voltages are the same in both cases and have been listed in Table 1. By applying the local RC feedback, the input resistance would be obviously zero and the inductance increases.

The QF of the circuit with the local RC feedback by definition is achieved from the following relation:

$$Q_f = \frac{X_{s,f}}{R_{s,f}} = \frac{R_{p,f}}{L_{p,f}\omega} = \frac{g_{m1}g_{m3}}{(C_{gs3}g_{m1} - C_f g_{m3})\omega} \quad (11)$$

Therefore, as the condition $C_{gs3}g_{m1} = C_f g_{m3}$ is established, the QF in frequencies lower than the SRF, which is given in Eq. (6), can be large enough. The bias voltage V_{SRF} is for adjusting g_{m1} and g_{m3} , and hence adjusting SRF. In contrast, V_Q is for adjusting g_{m1} and hence adjusting the quality of the AI in the whole UWB range.

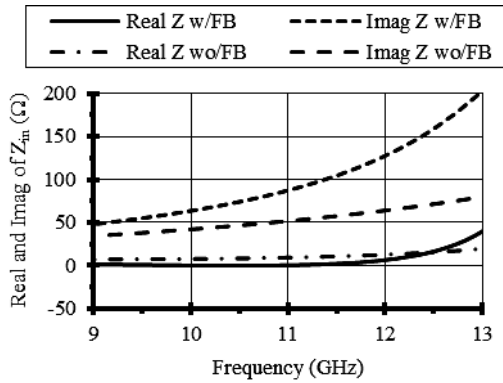


Fig. 5 Input impedance Z_{in} in high frequencies, with and without local feedback.

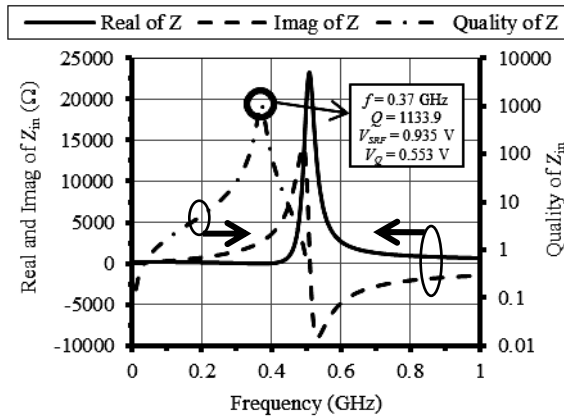


Fig. 6 Z_{in} and its QF in low frequencies.

Transconductances g_{m1} and g_{m3} , and also the SRF will increase by reducing V_{SRF} . Almost independent of g_{m3} , changing of V_Q will change g_{m1} and hence adjusts the QF of the AI. Figs. 6 and 7 show the effect of changing V_{SRF} for low and medium SRFs in UWB range. As is shown in Fig. 6, for frequencies higher than 250 MHz the QF of the active inductor is higher than 10. The effect of changing V_Q has been depicted in Fig. 8. As can be seen from Fig. 8, the QF is still more than 10 for frequencies up to 12.5 GHz. Since the input resistance could be easily zero, the QF could be increased almost independent of the inductance and SRF values.

3 Investigation of the Proposed Active Inductor Performance

In this section, in order to evaluate the relations governing the proposed circuit, results of the simulation will be given for each performance.

3.1 Input Referred Noise

In order to investigate the thermal noise characteristics of the circuit, each MOS transistor should be replaced with its noise model. Fig. 9 shows noise model of the circuit of Fig. 2 where it is obtained by using equivalent MOS noise model presented in [12]. In this figure, I_{ngi} and I_{ndi} are gate and drain channel

Table 1 Circuit parameters.

Element	Value
M_1	44/0.1 ($\mu\text{m}/\mu\text{m}$)
M_2	6/0.1 ($\mu\text{m}/\mu\text{m}$)
M_3	13/0.1 ($\mu\text{m}/\mu\text{m}$)
M_{B1}	14/0.1 ($\mu\text{m}/\mu\text{m}$)
M_{B2}	20/0.1 ($\mu\text{m}/\mu\text{m}$)
M_{B3}	5/0.1 ($\mu\text{m}/\mu\text{m}$)
M_{B4}	15/0.1 ($\mu\text{m}/\mu\text{m}$)
R_f	5 (Ω)
C_f	6 (fF)

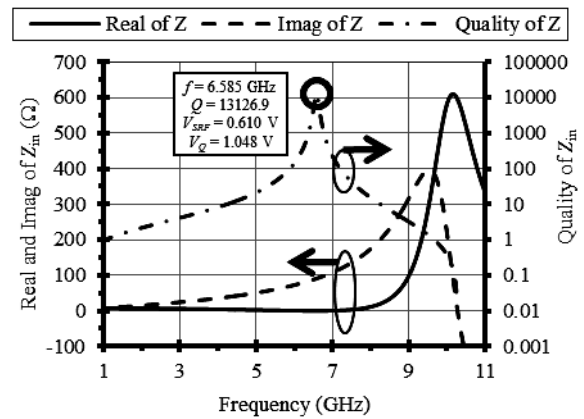


Fig. 7 Z_{in} and its QF in medium frequencies.

current noises, respectively. They are defined as follows:

$$\begin{cases} \overline{I_{ndi}^2} = 4K_B T \frac{\gamma}{\alpha_i} g_{mi} \\ \overline{I_{ngi}^2} = 4K_B T \delta g_{gi} \end{cases}, i = 1, \dots, 5. \quad (12)$$

in which

$$\begin{cases} \alpha_i = \frac{g_{mi}}{g_{d0i}} \\ g_{gi} = \frac{\omega^2 C_{gsi}^2}{5g_{d0i}} \end{cases} \quad (13)$$

where K_B is the Boltzmann constant, T the absolute temperature, Δf the frequency bandwidth, g_{d0i} the output conductance of the i -th transistor at zero drain bias (i.e., $V_{DS} = 0$), and γ the channel bias-dependent noise parameter. To obtain the output noise density, we ignore the noise of the gate and substrate series resistance and the noise of the low resistance of the local RC feedback. Let $V_{in,ngi} = N_{gi} I_{ngi}$ and $V_{in,ndi} = N_{di} I_{ndi}$ be the output noise voltage relative to the gate and drain noise currents of the i -th transistor, respectively. In this case, the noise coefficients N_{gi} and N_{di} , with respect to Fig. 9, are obtained as follows:

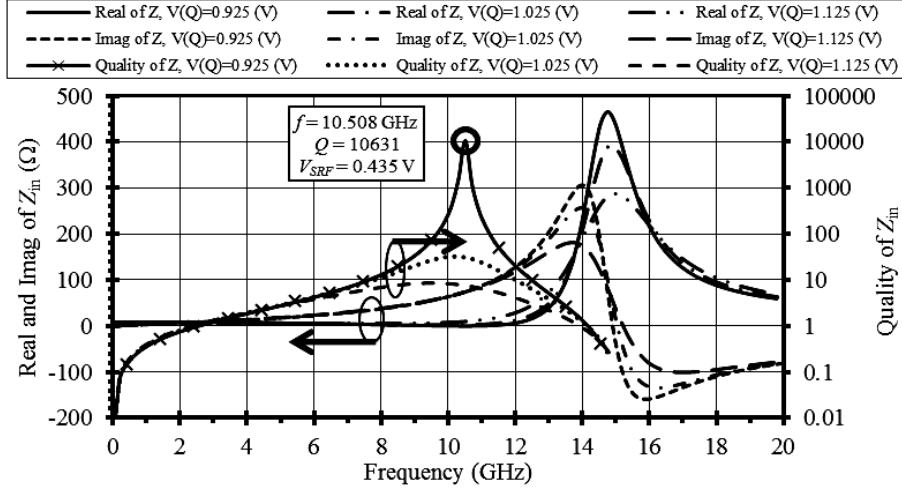


Fig. 8 Effect of variation of V_Q on Z_{in} in high frequencies (V_{SRF} is the same for all of the curves and equal to 0.435V).

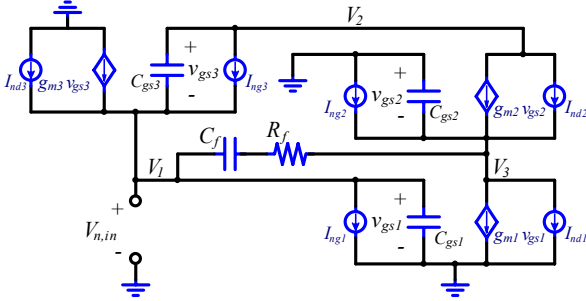


Fig. 9 Small-signal noise model for the AI structure of Fig. 2.

$$\begin{cases}
 N_{g1} = ((g_{m2}C_{gs3})s + (C_{gs2}C_{gs3} + C_fC_{gs3})s^2) / \text{Den} \\
 N_{d1} = (g_{m2}g_{m3} + (g_{m2}C_{gs3})s + (C_fC_{gs3})s^2) / \text{Den} \\
 N_{g2} = N_{d1} \\
 N_{d2} = ((g_{m3}C_{gs2} + g_{m3}C_f)s + (C_{gs2}C_{gs3})s^2) / \text{Den} \\
 N_{g3} = (g_{m2}g_{m3} + (g_{m3}C_{gs2} + g_{m3}C_f)s) / \text{Den} \\
 N_{d3} = N_{g1}
 \end{cases} \quad (14)$$

where:

$$\begin{aligned}
 \text{Den} = & g_{m1}g_{m2}g_{m3} + (g_{m1}g_{m2}C_{gs3} - g_{m2}g_{m3}C_f)s \\
 & + (g_{m2}C_{gs1}C_{gs3} + g_{m1}C_fC_{gs3})s^2
 \end{aligned} \quad (15)$$

Eqs. (14) and (15) show the dependency of the circuit parameters on the output noise voltage. Therefore, the overall output noise voltage spectral density of the AI is achieved as follows:

$$\overline{V_{in,n}^2} = \sum_{i=1}^3 (N_{gi}^2 \overline{I_{ngi}^2} + N_{di}^2 \overline{I_{ndi}^2}) \quad (16)$$

To reduce the noise voltage, according to Eqs. (14), (15), and (16), it is seen that g_{m1} should be increased. Nevertheless, increasing of g_{m1} leads to an increase in the power consumption. This addresses the trade-off between power and noise. On the other hand, according to Eqs. (9) and (10), to increase inductance and decrease series-loss resistance, g_{m1} and g_{m3} should be increased. Hence, the noise and series-loss resistance (which should be small) are placed against power (which should be small).

Simulation result of the input referred noise voltage is shown in Fig. 10. With respect to this figure, the noise increases by decreasing the SRF. Noise at the frequencies greater than 1 GHz is less than $10 \text{ nV}/\sqrt{\text{Hz}}$, which compares favorably with many of the reported AIs. As can be seen, when the QF is at its maximum, the noise is less than $10 \text{ nV}/\sqrt{\text{Hz}}$.

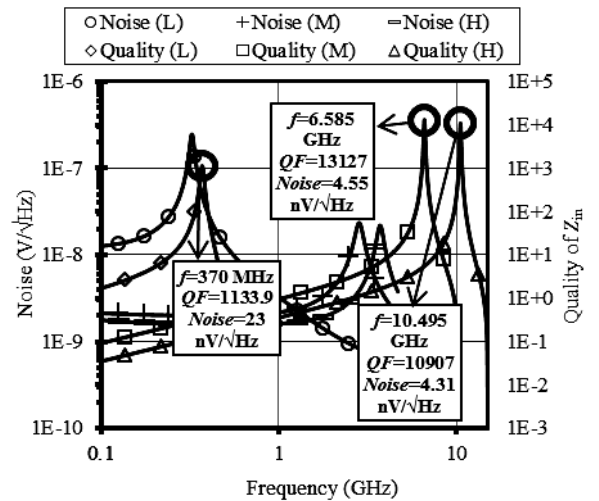


Fig. 10 Noise and QF of the AI.

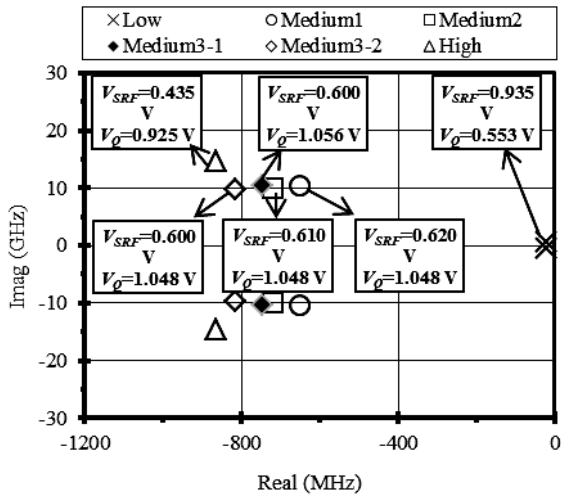


Fig. 11 S-plane to show dominant poles.

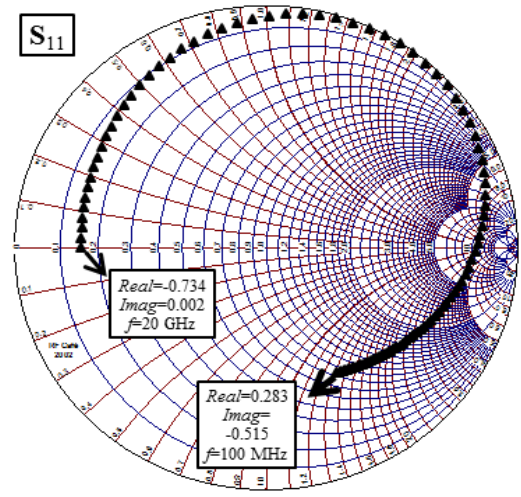


Fig. 12 S-parameter of the AI for medium frequencies.

Table 2 Special specifications of the proposed AI.

SRF (GHz)	Max of Imag (Ω) @ F (GHz)	Min of Real (Ω) @ F (GHz)	Max of Phase (degree)	Max of Quality	Noise (nV/\sqrt{Hz}) @ Q_{max}	P_{diss} (mW)
0.517	10436 @ 0.5	2.3 @ 0.370	89.950	1153	34.600	0.055
10.268	273 @ 9.4	6.9×10^{-3} @ 6.585	89.996	12395	5.500	5.200
14.874	250 @ 13.9	6.8×10^{-3} @ 10.490	89.995	10897	4.313	4.033

3.2 Stability of the Proposed AI

As was presented in [11], the stability condition of the AI is $G_{m1} > G_{m2}$, which is true in the designed circuit, i.e. $g_{m1} + g_{m2} > g_{m3}$. In addition, checking the location of zeros and poles of the input impedance is useful in examining the stability of the circuit. Fig. 11 depicts the position of the dominant imaginary poles of the AI. This figure is obtained by using the dimensions of the transistors, the feedback capacitor and resistor values given in Table 1. Zeros are real and negative in all cases, and we omit them, as well as the poles, which are negative and very far from the origin. In Fig. 11, input resistance at the point with hollow diamond marker is negative and not desired. By increasing V_Q and maintaining V_{SRF} fixed, the point with hollow diamond marker moves to the location of the point with filled diamond marker. The size of the imaginary part in the filled diamond marker is greater than that of hollow diamond one, which leads to a small reduction in its real value and QF will be improved. As long as the poles and zeros are in the left side of the imaginary axis in s-plane, the AI will be stable. When we set V_Q value much smaller than the optimal value (for zero input resistance), the real part of the input impedance will be large and negative value, and poles will move to the right side of the imaginary axis. This leads to loss of stability. Fig. 12 shows S_{11} , the input return loss, curve for medium frequencies. Size of S_{11} is smaller than one; hence, as it is known, input impedance is never out of the stable region. Table 2 summarizes the main

characteristics of the circuit at the SRFs of low, medium, and high. As is evidenced in this table, the dissipation power gradually increases by increasing SRF.

3.3 Nonlinearity of the Proposed AI

Linearity investigation of the UWB circuits always has a great importance. In UWB range, input power can extend to a value as high as 10 dBm and causes nonlinearity of the circuit characteristics [13]. Therefore, it is helpful to depict inductance variations versus input power sweep. Fig. 13 shows AI inductance versus input current amplitude in SRF of 6.585 GHz. As can be seen, the inductor reaches its 1-dB compression point at the input current amplitude of 480 μA . This is equivalent to the input voltage amplitude equal to 55.66 mV, which is a very large input. Table 3 is provided for the comparison of the proposed AI characteristics with the other reports. Layout of the proposed AI is depicted in Fig. 14. The size of the circuit without pads is 20 $\mu m \times 12.3 \mu m$ or equivalently 246 μm^2 .

4 Conclusion

In this paper, a new method, which is the applying of the RC feedback in the AIs, has been presented to cancel the series-loss resistance. By adding an RC feedback to the forward path of the AI, a negative term is added to the series-loss resistance, and hence, it is simply canceled. Inductive bandwidth of the proposed

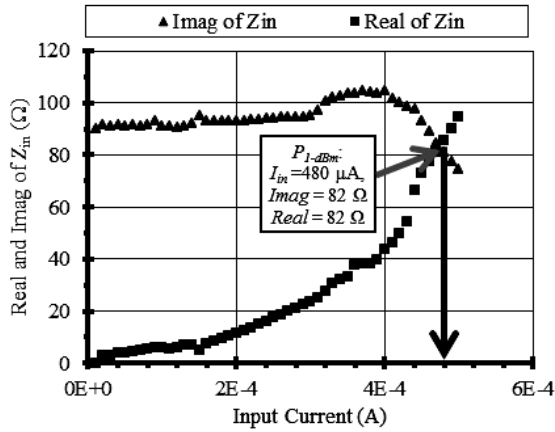


Fig. 13 Linearity of the AI at 6.585 GHz.

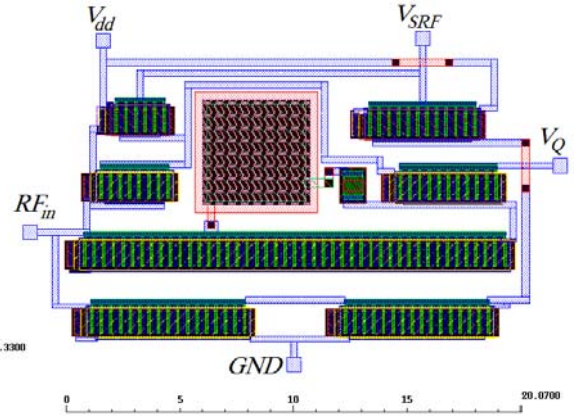


Fig. 14 Layout of the proposed AI.

Table 3 Performance comparison of the proposed UWB AI with the reported AIs.

Ref.	Tech. ($\mu\text{m}/\text{V}$)	IBW ¹ (GHz)	Q_{max} @ F (GHz)	L_{max} (nH) @ F (GHz)	MIVS ² (mV)	Noise (nV/ $\sqrt{\text{Hz}}$) @ Q_{max}	P_{diss} (mW)	Fab/Sim ³
[3]	0.18/n.a.	n.a. ⁴	68 @ 3.6	33 @ 4	n.a.	n.a.	3.6	Fab
[7]	0.13/1.6	0.5-10.2	3000 @ 3.7	14.5 @ 5.5	n.a.	2	13.6	Fab
[8]	0.18/1.8	n.a.	28 @ 1	27 @ 1.5	n.a.	n.a.	4	Fab
[10]	0.13/1.2	n.a.	38.8 @ 6.8	6.4 @ 7.5	n.a.	n.a.	6.4	Fab
[14]	0.13/1.2	0.3-7.32	3900 @ 5.75	144 @ 6.4	18	3.1	1	Sim
[15]	90nm/1.2	0.6-3.8	120 @ 3	530 @ n.a.	n.a.	43.4	1.2	Sim
This Work	90nm/1.2	0.25-12.50	† 1153 ‡ 10970	†† 1141 ‡‡ 1.124	55.7	†34.6 ‡4.6	†0.055 ‡4	Sim

† @ 0.370GHz †† @ 0.570GHz ‡ @ 10490GHz ‡‡ @ 14874GHz

¹Inductive Bandwidth; ²Max. Input Voltage Swing; ³Fabrication/ Simulation; ⁴Not assigned.

circuit is as high as 12.25 GHz. A QF of 10970 with an inductance of 1.124 nH at the frequency of 10.5 GHz has been obtained. In addition, a QF of 13159 with an inductance of 2.2 nH at the frequency 6.6 GHz has been achieved. In the low frequency of 370 MHz, a very high inductance of 1141 nH was resulted. The features mentioned in the report are more favorable compared with many other reports. The features are as completely UWB range coverage, very high quality factors, low noise, low power, and high linearity.

Appendix: The Derivation of Eqs. (3) and (7)

For the derivation of Eqs. (3) and (7), firstly, the originals of the both Eqs. (3) and (7) should be extracted from the small-signal model of the AI, which is depicted in Fig. 3. Since the original equations provide little insight about the relation between them and simulation results, both should be simplified with the same degree of approximation. In the followings, first, the original equations will be expressed and then by some admissible approximations the simplified ones will be derived.

Input admittance for the small-signal equivalent circuit of Fig. 3, without RC feedback and any approximations, is as follows:

$$Y_{\text{in}} = \frac{g_{m1}g_{m2}g_{m3}}{g_{m2}C_{gs3}S + C_{gs2}C_{gs3}S^2} + \frac{g_{m1}g_{m2}C_{gs3}S}{g_{m2}C_{gs3}S + C_{gs2}C_{gs3}S^2} + \frac{g_{m2}C_{gs1}C_{gs3}S^2}{g_{m2}C_{gs3}S + C_{gs2}C_{gs3}S^2} + \frac{C_{gs1}C_{gs2}C_{gs3}S^3}{g_{m2}C_{gs3}S + C_{gs2}C_{gs3}S^2} \quad (17)$$

For the 90 nm technology, gate-source capacitance C_{gsi} of the non-bias transistors is in the order of some tens of femtofarads and the transconductance g_{mi} is in the order of some millisiemens. Therefore, the term $C_{gs}\omega$ is very smaller than g_m in the frequency range of 0.25-12.5 GHz. As a result, considering the terms with the same order, those consist of $C_{gs}\omega$ are very small compared to those consist of g_m . Therefore, the former can be neglected in the extraction of any relation from the proposed circuit. For instance, the term $C_{gs2}C_{gs3}S^2 + g_{m2}C_{gs3}S$ is equal to $g_{m2}C_{gs3}S$, since the term $C_{gs2}C_{gs3}S^2$ is very smaller than the term $g_{m2}C_{gs3}S$. Accordingly, Y_{in} can be rewritten as:

$$Y_{in} = \frac{g_{m1}g_{m2}g_{m3}}{g_{m2}C_{gs3}s} + \frac{g_{m1}g_{m2}C_{gs3}s}{g_{m2}C_{gs3}s} + \frac{g_{m2}C_{gs1}C_{gs3}s^2}{g_{m2}C_{gs3}s} + \frac{C_{gs1}C_{gs2}C_{gs3}s^3}{g_{m2}C_{gs3}s} \quad (18)$$

After some mathematics, the result is:

$$Y_{in} = \frac{1}{Z_{in}} = \frac{g_{m1}g_{m3}}{C_{gs3}s} + g_{m1} + C_{gs1}s + \frac{C_{gs1}C_{gs2}s^2}{g_{m2}} = \frac{g_{m1}g_{m3}}{C_{gs3}s} + \frac{g_{m1}g_{m2} - C_{gs1}C_{gs2}\omega^2}{g_{m2}} + C_{gs1}s \quad (19)$$

Finally

$$Y_{in} = \frac{1}{Z_{in}} = \frac{g_{m1}g_{m3}}{C_{gs3}s} + g_{m1} + C_{gs1}s \quad (20)$$

This equation is mentioned as Eq. (3) in the text. Indeed, for the circuit with RC feedback, input admittance of its small-signal equivalent circuit without any approximation is derived as follows:

$$Y_{in,f} = \frac{1}{Z_{in,f}} = \frac{Num}{Den} \quad (21)$$

where

$$Num = g_{m1}g_{m2}g_{m3} + (g_{m1}g_{m2}C_{gs3} + g_{m1}g_{m2}g_{m3}C_fR_f - g_{m2}g_{m3}C_f)s - (g_{m2}C_{gs1}C_{gs3} + g_{m1}g_{m2}C_{gs3}C_fR_f + g_{m1}C_{gs3}C_f)\omega^2 - (C_{gs1}C_{gs2}C_{gs3} + g_{m2}C_{gs1}C_{gs3}C_fR_f + C_{gs1}C_{gs3}C_f + C_{gs2}C_{gs3}C_f)\omega^2 + (C_{gs1}C_{gs2}C_{gs3}C_fR_f)\omega^4 \quad (22)$$

and

$$Den = (g_{m2}C_{gs3})s - (C_{gs2}C_{gs3} + g_{m2}C_{gs3}C_fR_f + C_{gs3}C_f)\omega^2 - (C_{gs2}C_{gs3}C_fR_f)\omega^2s \quad (23)$$

By the same approximations considered in the derivation of Eq. (3), the last equations can be written as:

$$Num = g_{m1}g_{m2}g_{m3} + (g_{m1}g_{m2}C_{gs3} - g_{m2}g_{m3}C_f)s - (g_{m2}C_{gs1}C_{gs3} + g_{m1}C_{gs3}C_f)\omega^2 - (C_{gs1}C_{gs2}C_{gs3} + C_{gs1}C_{gs3}C_f + C_{gs2}C_{gs3}C_f)\omega^2s + (C_{gs1}C_{gs2}C_{gs3}C_fR_f)\omega^4 \quad (24)$$

and

$$Den = (g_{m2}C_{gs3})s - (C_{gs2}C_{gs3} + C_{gs3}C_f)\omega^2 - (C_{gs2}C_{gs3}C_fR_f)\omega^2s \quad (25)$$

Again, for simplicity purposes, we can rewrite the last equations as:

$$Num = g_{m1}g_{m2}g_{m3} + (g_{m1}g_{m2}C_{gs3} - g_{m2}g_{m3}C_f)s - (C_{gs1}C_{gs2}C_{gs3} + C_{gs1}C_{gs3}C_f + C_{gs2}C_{gs3}C_f)\omega^2s \quad (26)$$

and

$$Den = (g_{m2}C_{gs3})s - (C_{gs2}C_{gs3} + C_{gs3}C_f)\omega^2 \quad (27)$$

The final derivation for the input admittance of the small-signal model of the circuit with the RC feedback is as follows:

$$Y_{in,f} = \frac{1}{Z_{in,f}} = \frac{Num}{Den} = \frac{g_{m1}g_{m2}g_{m3} + (g_{m1}g_{m2}C_{gs3} - g_{m2}g_{m3}C_f)s}{(g_{m2}C_{gs3})s} = \frac{g_{m1}g_{m3}}{C_{gs3}s} + \frac{g_{m1}C_{gs3} - g_{m3}C_f}{C_{gs3}} \quad (28)$$

This equation is mentioned as Eq. (7) in the literature. The equation shows that series-loss resistance can be set to zero by adjusting the term $g_{m3}C_f$ close to the term $g_{m1}C_{gs3}$.

References

- [1] Chirala M. K., Guan X., and Nguyen C., "Integrated multilayered on-chip inductors for compact CMOS RFICs and their use in a miniature distributed low-noise-amplifier design for ultra-wideband applications," *IEEE Trans. on Microwave Theory Tech.*, Vol. 56, No. 8, pp. 1783-1789, Aug. 2008.
- [2] Zito D., Fonte A. and Pepe D., "Microwave active inductors," *IEEE Microwave and Wireless Components Letters*, Vol. 19, No. 7, pp. 461-463, July 2009.
- [3] Lai Q. and Mao J., "A new floating active inductor using resistive feedback technique," *IEEE Int. Microwave Symp.*, pp. 23-28, May 2010.
- [4] Reja M., Moez K. and Filanovsky I., "A wide frequency range CMOS active inductor for UWB bandpass filters," *IEEE Int. Microwave Symp.*, pp. 1055-1058, Aug. 2009.
- [5] Reja M., Filanovsky I. and Moez K., "A CMOS 2.0-11.2 GHz UWB LNA using active inductor circuit," *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 2266-2269, June 2008.
- [6] Lu L. H., Hsieh H. H. and Liao Y. T., "A wide tuning-range CMOS VCO with a differential tunable active inductor," *IEEE Trans. on Microwave Theory Tech.*, Vol. 54, No. 9, pp. 3462-3468, Sep. 2006.
- [7] Li C., Gong F. and Wang P., "Analysis and design of a high-Q differential active inductor with wide tuning range," *IET Circuits Devices & Systems*, Vol. 4, No. 6, pp. 486-495, Nov. 2010.
- [8] Hwang K. S., Cho C. S., Lee J. W. and J. Kim, "High quality-factor and inductance of symmetric differential-pair structure active inductor using a feedback resistance design," *IEEE Int. Microwave Symp.*, pp. 1059-1062, June 2008.

- [9] Hsiao C. C., Kuo C. W. and Y. J. Chan, "Improved quality-factor of 0.18- μ m CMOS active inductor by a feedback resistance design," *IEEE Microwave and Wireless Components Letters*, Vol. 12, No. 12, pp. 467-469, Dec. 2002.
- [10] Ahmed A. and Wight J., "6.7 GHz high-Q active inductor design using parasitic cancellation with process variation control," *IEEE Electronics Letters*, Vol. 46, No. 7, pp. 486-487, Apr. 2010.
- [11] Bakken T. and Choma J., "Gyrator-based synthesis of active on-chip inductances," *Int. Journal of Analog Integrated Circuits and Signal Processing*, Vol. 34, pp. 171-181, Mar. 2003.
- [12] Ziel A. V. D., "Noise in solid state devices and circuits," John Wiley & Sons Inc., 1986.
- [13] Lo C. C., Yang Y. L., Tsai C. L., Lee C. S. and Yang C. L., "Novel wireless impulsive power transmission to enhance the conversion efficiency for low input power," *IEEE Microwave Workshop Series on Innovative Wireless Power Transmission: Technologies, Systems, and Applications*, pp. 55-58, June 2011.
- [14] Uyanik H. U. and Tarim N., "Compact low voltage high-Q CMOS active inductor suitable for RF applications," *Int. Journal of Analog Integrated Circuits and Signal Processing*, Vol. 51, No. 3, pp. 191-194, June 2007.
- [15] Krishnamurthy S. V., El-Sankary K. and El-Masry E., "Noise-cancelling CMOS active inductor and its application in RF band-pass filter design," *Int. Journal of Microwave Science and Technology*, Vol. 2010, Feb. 2010.



Majid Rafei was born in Tehran, Iran, in 1984. He received the B.S. degree in electronics engineering from Tarbiat Moealem University, Sabzevar, Iran, in 2010, and is currently working toward M.S. degree in electronics engineering at Iran University of Science and Technology, Tehran, Iran. His research interests include the Design of Radio Frequency Integrated Circuits (RFICs), Optimization using Evolutionary Algorithms (EAs), and Modeling and Optimization by means of Artificial Neural Networks (ANNs).



Mohammad Reza Mosavi received his B.S., M.S. and Ph.D. degrees in Electronic Engineering from Iran University of Science and Technology (IUST), Tehran, Iran in 1997, 1998 and 2004, respectively. He is currently faculty member of Department of Electrical Engineering of IUST as associate professor. He is the author of about 140 scientific publications on journals and international conferences. His research interests include circuits and systems design.