Design of a Resonant Suspended Gate MOSFET with Retrograde Channel Doping

M. Fathipour*, M. H. Refan** and S. M. Ebrahimi**

Abstract High Q frequency reference devices are essential components in many Integrated circuits. This paper will focus on the Resonant Suspended Gate (RSG) MOSFET. The gate in this structure has been designed to resonate at 38.4MHz. The MOSFET in this device has a retrograde channel to achieve high output current. For this purpose, abrupt retrograde channel and Gaussian retrograde channels have been investigated.

Keywords: Natural Frequencies, Pull-in Voltage, Retrograde Channel, Resonant Suspended Gate (RSG) MOSFET.

1 Introduction 1

Resonant Gate Transistor (RGT) was first introduced in 1967 by Nathanson and coworkers [1]. However this device had a Q factor approximately equal to 100 due to it's low mass. Packaging was another hurdle to the fabrication of this device. Since then optimization of RGT and use of new designs, has resulted in enhanced quality factor for this device. Rapid development of MOS technology during last few years has provided new schemes for optimization of this device [2], [3]. To increase the Q factor of Resonant Suspended Gate (RSG) MOSEFET, large mass and use of vacuum packaging is essential. For example by replacing beam with a disk, mass, and therefore Q is increased. Other parameters of interest include low power consumption as well as small size [4]. This is infact the case for the radio frequency (RF) MEMS component such as antennas, low-noise tunable oscillators, tunable filters, and tunable matching networks for wideband (or multiband) radios [5]. Another goal in the design of such circuits is to integrate all of the elements on one chip. This has proved to be a difficult task. The bottleneck is not the fabrication of inductors or resonators, but the achieving high quality factors needed for such application . Using RF MEMS devices (switches, varactors, and high-Q planar inductors), it may be possible to eliminate the off-chip inductor in the oscillator circuit or to integrate a tunable filter on the silicon chip (or on the glass or ceramic carrier). In this paper we present a procedure for the design of a resonator using MOS technology. This paper is organized as follows: In Section 2 the Resonator architecture is presented. In Section 3 we design the Gate Geometry to achieve a desired resonant frequency**.** In section 4 we get Air gap distance for the RSG MOSFET structure. In section 5 we investigate abrupt retrograde channel and Gaussian retrograde channel design for the RSG MOSFET. Finally in section 6 we provide a conclusion.

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2 Resonator Architecture

2.1 Structure

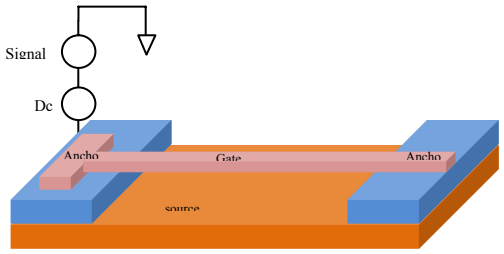
The resonator discussed in this section, is built in MOS technology and essentially consists of a beam which is suspended over the channel of the MOSFET. This structure is thus referred to as Resonant Suspended Gate MOSFET or RSG-MOSFET. A schematic of the RSG MOSFET and it's Electrical equivalent circuit is presented in Fig. 1 where gap, inversion and depletion capacitances (C_{gap} , C_{ox} , C_{dep} , and C_{inv}) are capacitively divide the applied gate voltage V_G [6].

$$V_{G\,int} = \frac{V_G}{\left(1+\frac{C_{gc}}{C_{gap}}\right)} \tag{1}$$

$$C_{gc}(V_{G\,int}) = \frac{C_{ox}C_{inv}}{C_{ox}+C_{inv}+C_d} \tag{2}$$

2.1 Description of the Pull-in Phenomena

An appropriate DC bias as well as a sinusoidally varying signal is applied to the gate. This scheme results



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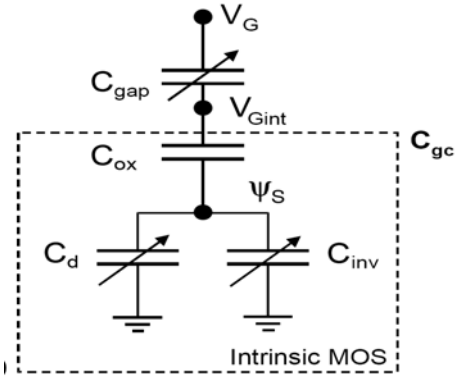


(b)

Fig. 1 a) Schematic of the RSG MOSFET b) Electrical equivalent circuit of the RSG-MOSFET showing the capacitive divider.

in an electrostatic force, that is proportional to gap capacitance, C_{gap}, and the voltage that is applied. This force causes the beam to deflect towards the channel, therefore the current in the channel can be modulated in accordance to applied voltage. Increasing V_G, increases the deflection until the stiffness of the system reaches zero. Further increase in V_G, causes the gate to touch the channel. For two plates with distance d, this voltage is known as pull-in voltage. This voltage is expressed as [1]:

$$V_{pi} = \sqrt{\frac{8}{27}\frac{kd^3}{\varepsilon_0 A}} \tag{3}$$

where ε_0 is dielectric constant of air, A is the plate area, d is the distance between two plates and k is rigidity of the plate that is calculated from its geometry and dimensions as:

$$k = \frac{192EI}{L^3} \tag{4}$$

$$I = \frac{WH^3}{12} + \frac{HW^3}{12} \tag{5}$$

where I is the bending moment of inertia of the rectangular shape, E is young's modulus and H, L, W are respectively the beam thickness, length and width.

The pull-in voltage for the RSG-MOSFET deduced from Eq. (1) and Eq. (3) as [7]:

$$V_{pi} = \sqrt{\frac{8}{27}\frac{k_{gate}d^3}{\varepsilon_0 A_{gate}}\left(1+\frac{C_{gap}}{C_{gc}}\right)} \tag{6}$$

Fig. 2 shows down-state for voltages greater than pull-in voltage and the up-state for voltages smaller than pull-in voltage.

In linear applications such as resonator or filter design V_G must be less than V_{pi} such that [1]:

$$\left(\frac{V_G}{V_{pi}}\right)^2 \approx .5 \tag{7}$$

The natural frequencies of a beam with length L, height H and Width W, is given by [5]

$$f_n = \frac{(k_{nl})^2}{2\pi l^2}\left(\frac{EI}{\rho A}\right)^{\frac{1}{2}} \tag{8}$$

where ρ is density of the suspended gate and K_{nl} is given by [5] as $K_{1l} = 4.73$, $K_{2l} = 7.85$, $K_{3l} = 10.99$ and $K_{4l} = 14.14$.

High mode shape resonance can be used to achieve higher frequency operation, however the first mode is easier to actuate with a single actuation electrode and allows larger amplitude of displacement which is of benefits to the output current level, furthermore for high frequency resonators, the frequency sensitivity to dimensions, related to the lithographical step, can severely shift the frequency from the expected value. As an example, a variation of 10nm in length on a 6.5 μm long and 1 μm thick polysilicon beam induces a frequency shift of 800 kHz at 200 MHz (51 kHz for a 38.4 MHz resonator with similar thickness and 15.1 μm length). Thus from Eqs. (5) and (8) with selecting the first mode, the first natural frequency for the clamped-clamped beam is expressed as [8]:

$$f_R \approx 1.03\sqrt{\frac{E}{\rho}\frac{H}{L^2}} \tag{9}$$

From above equation, the resonant frequency Increases when the beam stiffness is increased [9]. Dimensions of the gate are important parameters in determining the resonant frequency. As resonator length is reduced resonant frequency increases. From Eq. (9) resonant frequency is independent of width but is a function of length and height of the gate.

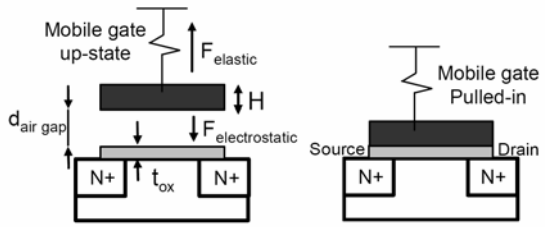


Fig. 2 Schematic of the RSG-MOSFET in the up-state and down-state.

3 Design of the Gate Geometry

In this section we provide the design guideline for a MEMS resonator to replace the quartz crystal with an oscillation frequency equal to 38.4 MHz. ANSYS was used for simulation analysis. We used SOLID45 for structural field modeling. SOLID45 is used for the 3-D modeling of solid structures. This element is defined by eight nodes and has three degrees of freedom at each node: translations in the nodal x, y and z directions. Gate material can be selected whether polysilicon or AlSi1%, that leads to the different processes. In this paper our material assumed to be AlSi1% whose Young's modulus and density are E=48e3 μN/(μm)^2 and ρ=2700e-18 kg/(μm)^3 respectively. By applying Eq. (9) we obtain L=8.22 μm and H=0.6 μm.

Fig. 3 shows the first natural frequency of this clamped-clamped beam.

4 Air Gap Design for the RSG MOSFET Structure

The application of the RSG in resonator mode is linear, i.e. suspended gate should not touch the channel surface, while it is vibrating around it's equilibrium position with small amplitudes, Therefore upon applying a signal, displacement of the gate and therefore change of current in the channel is small and linear. For the RSG-MOSFET modeling, especially for pull-in voltages prediction, the notion of electrical air-gap is introduced. It represents the electric field between the gate and the channel, more relevant than physical air-gap. For the AlSi1% gate the equivalent gap thickness (EGT) of the RSG-MOSFET from Eq. (10) is obtained. In this design we chose the pull-in voltage to be 40v, therefore from Eq. (3) and use of gate geometry obtained in previous section, gap distance is found to be equal to 95 nm. This gap distance is effective gap distance and is sum of the air gap distance and also the gate oxide thickness [9].

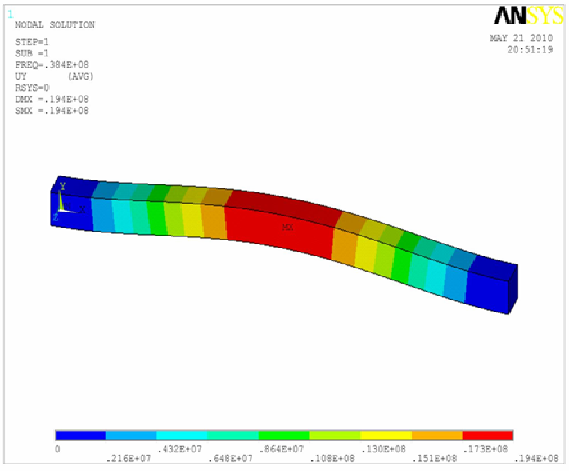


Fig. 3 FEM modal simulation of a clamped–clamped beam dimensions: length 8.22 μm, width 0.5μm, height 0.6 μm, ANSYS 38.4 MHz, analytic 38.4 MHz.

$$EGT = d_{gap0} + \frac{t_{ox}}{\varepsilon_{rox}} \qquad (10)$$

where d_{gap0} is the air gap between the electrode and the conductive suspended gate, t_{ox} is the gate oxide thickness and ε_{rox} is the relative permittivity of the oxide.

Already the pull-in voltage for RSG MOSFET is given by Eq. (6) but it is easier to use Eq. (3) with d given by EGT in Eq. (10). When the gate oxide thickness is increased, the pull-in voltage is also increased. Fig. 4 shows deflection of the gate as a function of gate voltage.

5 MOSFET Optimization for RSG MOSFET

In today's MOSFETs, because of scaling, substrate's doping must be increased. On the other hand this heavy doping for our RSG-MOSFET is not good and causes threshold voltage increase and therefore reduces drain current. Thus for better control of the threshold voltage and current the body is generally not doped uniformly. A common doping profile in modern MOSFETs is a retrograde profile with a lightly doped surface layer on a relatively heavy doped substrate. The lower surface doping concentration defines the threshold voltage. It also increases the effective mobility by reducing the Coulomb scattering. The incorporation of a retrograde doping profile at the substrate's surface, leads to a parallel shift of the I–V characteristics along the gate voltage as compared to a similar MOSFET with a uniformly doped body. By using retrograde channel one can maximize the current of the MOSFET [11].

In this paper, we investigate abrupt retrograde channel and Gaussian retrograde channel. The abrupt model assumes an ideal retrograde doping profile with an abrupt boundary between the surface layer and the uniformly, heavily doped substrate. This doping profile is shown in Fig. 5. For Gaussian retrograde channel we also assumes a Gaussian boundary between the surface

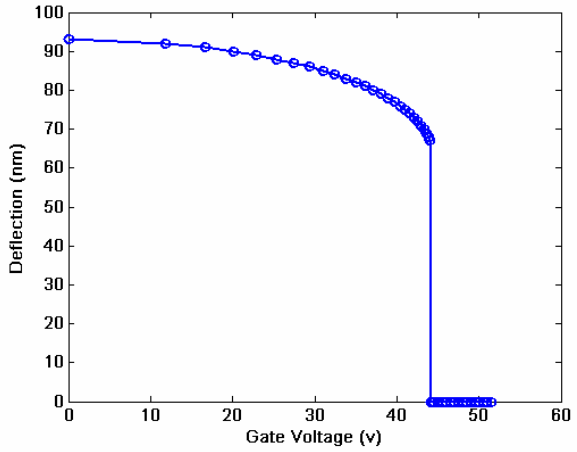


Fig. 4 Deflection of gate for voltages (V) that smaller than pull-in.

layer and the uniformly, heavily doped substrate. This doping profile is shown in Fig. 6.

It is interesting to note that in standard MOSFETs, the drain current in the subthreshold regime increases exponentially with the gate voltage. In the case of the movable gate MOSFET, the increase of V_G induces the air-gap reduction and increases the gate capacitance. The drain current increases super-exponentially in weak inversion when the gate voltage is approaching the pull-in region. A commercial software has been used for this purpose. Fig. 7 shows drain current versus gate voltage for two cases of abrupt retrograde and Gaussian retrograde channel profiles and compares uniform lightly doped 4×10^{15} (Atom/cm3) [7] and uniform heavy doped doping 1×10^{18} (Atom/cm3) for substrate. It is found that the uniform lightly doped channel, has good current and channel with heavy doped, approximately has zero current. This is due to large threshold voltage of approximately 43v. The abrupt retrograde profile and Gaussian retrograde channel lowers threshold voltage and consequently results in a higher drain current.

6 Process

The fabrication process is very similar to that given by [7] with a minor modification. It uses five masks and includes one CMP step. In first step a wet oxidation is used to grow a 30nm silicon dioxide layer then a 60nm silicon nitride layer is deposited by LPCVD. Because stress in this structure must be low, silicon dioxide is used to decrease stress between the substrate and silicon nitride layer. Active zones are then dry etched through the SiO2-Si3N4 isolation bi-layer (Fig. 8-a). The height of isolation layer will define the air-gap of the suspended-gate. After this stage a thermal gate oxide is grown in the active zones. Thickness of this layer is 10nm. This oxide layer is the same as gate oxide layer

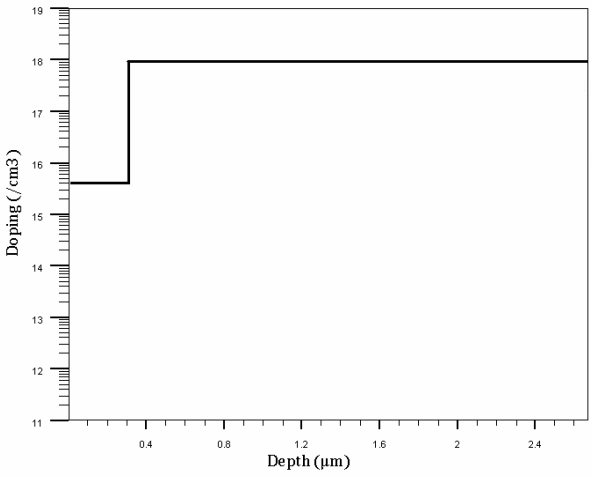


Fig. 5 Abrupt retrograde channel.

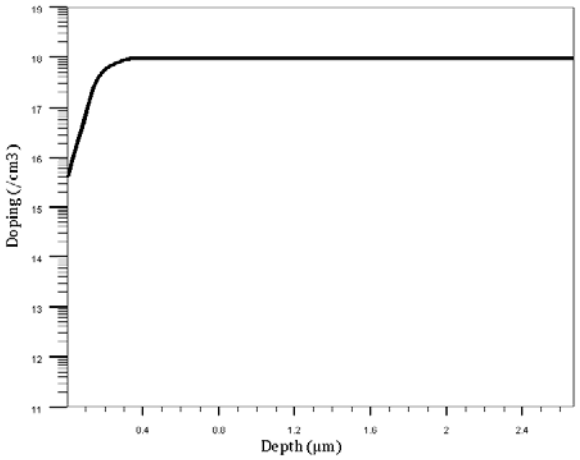


Fig. 6 Gaussian retrograde channel.

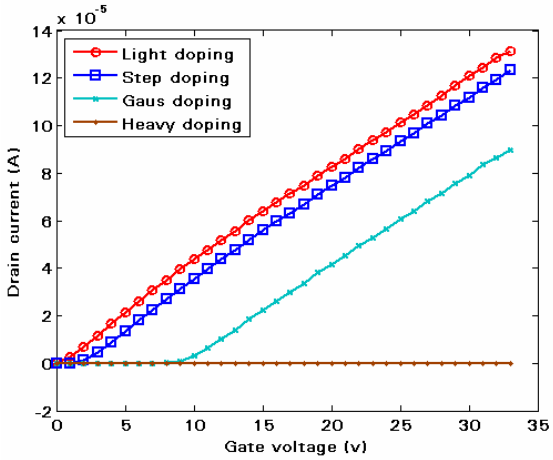
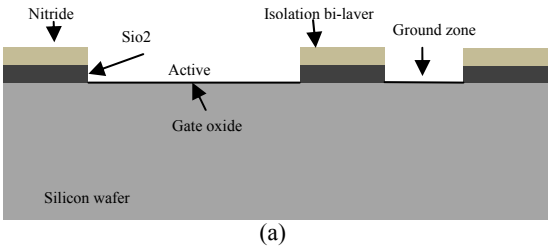


Fig. 7 Simulation I_d versus V_G for voltages (V) smaller than pull-in.

in MOS structure. Source and drain were photolithographically defined and a thick photoresist mask is used to implant through the thin gate oxide. A second masking step is used to implant Boron to define the ground contact. Diffusion annealing rearranges the atomic structure of the silicon (Fig. 8-b). Third mask used to define doping of the channel (Fig. 8-c)**.** A critical step on this process is to precisely control the gap between the gate and the channel, which is achieved by controlling the sacrificial thickness and uniformity on the wafer. A 600 nm LPCVD polysilicon layer was deposited followed by a Low Temperature Oxide (LTO). This LTO used to avoid dishing in the sacrificial layer (Fig. 8-d). Chemical Mechanical Polishing (CMP) step is critical to flatten the sacrificial layer in order to have a flat resonator structure and limit the energy loss through thermo-elastic dissipation due to stress concentration in the non-flat parts of the resonator. This CMP in two steps is done (Fig. 8-d). To define the electrical contacts, the polysilicon was patterned by a mixed C_4F_8 and SF_6 plasma followed by a C_4F_8



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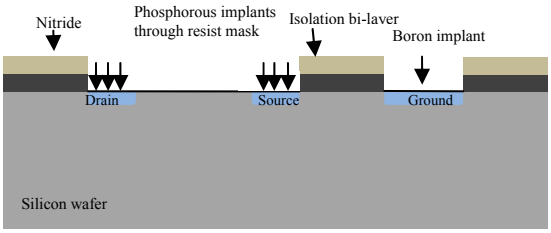

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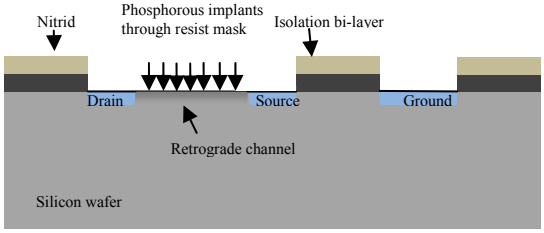

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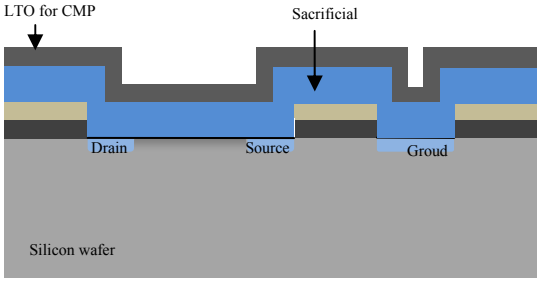

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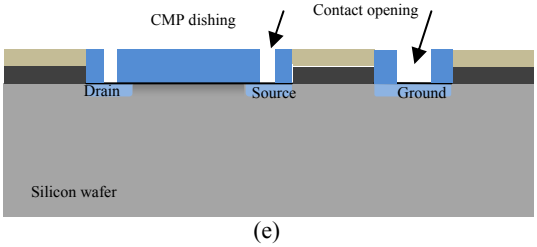

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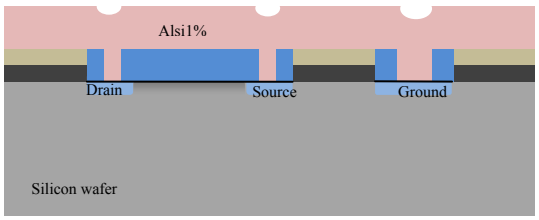

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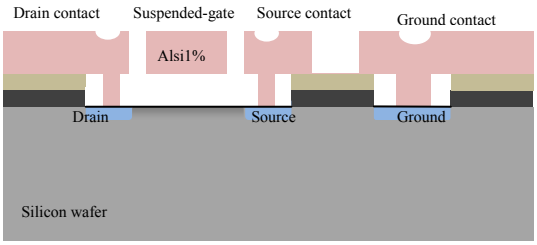

(g)

Fig. 8 Schematic of the fabrication process steps of a metallic RSG-MOSFET.

plasma to etch the thermal gate oxide. A 0.6 µm aluminum-silicon film alloy (AlSi 1%) is sputtered under high vacuum and used as structural material (Fig. 8-f). In final stage the 0.6µm aluminum-silicon film alloy (AlSi 1%) is etched through the pure isotropic SF_6 plasma (Fig. 8-d).

6 Conclusion

For integrating RF element, such as on chip frequency reference oscillators, RSG-MOSFET resonator can play an important role due to high Q, but output current in this device may be small. In this paper we have shown that use of retrograde profile for the MOSFET channel, the output current of the device may be enhanced.

Appendix I

Pull-in Voltage in Electrostatic Microactuators

In this appendix, we cover the pull-in effect in electrostatic MEMS devices. Fig. 8 shows the schematic of an electrostatic actuator that could be used for example as a tunable RF capacitor. When voltage is applied over the capacitance, electrostatic force will work to reduce the plate separation d-x. At small voltages, the electrostatic voltage is countered by the spring force $F_k = kx$ but as voltage is increased the plates will eventually snap together. Estimating this pull-in voltage V_{pi} and the plate travel distance X before pull-in effect is required for the successful design of electrostatic actuators, switches, varactors and sensors.

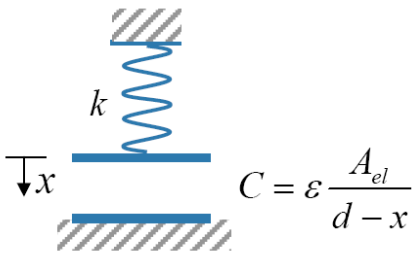

Fig. 8 Schematic of an electrostatic actuator. The plate is attached to a spring k. The capacitor capacitance C depends on the plate area A_{elec} and gap d-x.

To derive the expression for pull-in, we start by writing the total potential energy in the system:

$$E = -\frac{1}{2}\frac{\varepsilon A_{el}}{d-x}V_{pi}^2 + \frac{1}{2}kx^2 \quad (A1)$$

where the first term is the electrostatic potential of the deformable capacitor and of the voltage source and the second term is due to the mechanical energy stored in the spring. The force acting on the movable plate is obtained by deriving Eq. (A1):

$$F = -\frac{\partial E}{\partial x} = \frac{1}{2}\frac{\varepsilon A_{el}}{(d-x)^2}V_{pi}^2 - kx \quad (A2)$$

At equilibrium, the electrostatic force and spring force cancels (F = 0) and Equation (A2) gives:

$$kx = \frac{1}{2}\frac{\varepsilon A_{el}}{(d-x)^2}V_{pi}^2 \quad (A3)$$

A simple expression for the pull-in point is obtained by deriving Eq. (A2) to obtain the stiffness of the system:

$$\frac{\partial F}{\partial x} = \frac{\varepsilon A_{el}}{(d-x)^3}V_{pi}^2 - k \quad (A4)$$

Substituting Eq. (A3) gives the stiffness around the equilibrium point:

$$\frac{\partial F}{\partial x} = \frac{2kx}{(d-x)} - k \quad (A5)$$

With no applied voltage Eq. (A5) is simplified to $\frac{\partial F}{\partial x} = -k$; a small positive movement δx result in negative restoring force $\frac{\partial F}{\partial x}\delta x = -k\delta x$. Increasing the bias voltage V makes the stiffness less negative. The unstable point is given by $\frac{\partial F}{\partial x} = 0$ giving

$$x = \frac{1}{3}d \quad (A6)$$

Substituting Eq. (A6) to Eq. (A3) gives the pull-in voltage at which the system becomes unstable

$$V_{pi} = \sqrt{\frac{8}{27}\frac{kd^3}{\varepsilon_0 A_{el}}} \quad (A7)$$

Acknowledgment

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